RISC-V IS CHANGING THE EMBEDDED PROCESSOR WORLD
Codasip Is Leading The Way

ENHANCED TOOLS FOR RISC-V PROCESSOR DEVELOPMENT
Codasip is the leading provider of RISC-V processor IP

Codasip Bk: A portfolio of RISC-V processors
Uniquely providing design automation tools that allow users to easily modify RISC-V processors

- Performance/power efficiency and low cost
- Algorithm accelerators (DSP, security, audio, video, etc.)
- Profiling of embedded SW for tailoring processor IP

Codasip introduced its first RISC-V processor in November 2015
CODASIP’S 2018 RISC-V PORTFOLIO

Selection of low-power, high-performance options for any design

- **Broad portfolio** of processor cores
- **Micro-architectural choices:**
  - Bk1 – zero pipeline stage
  - Bk3 – balanced performance/power
  - Bk5 – optional caches and jump predictor
  - Bk5-64 – adds 64-bit addressing to Bk5
  - Bk7 – Linux capable, 7-stage with branch prediction
- All fully **compliant** with the RISC-V specification
- All fully **configurable**
- All fully **customizable**

Differentiates & gives competitive advantage
CONFIGURE RISC-V AS YOU NEED

1. Select an implementation to start with (Bk1, Bk3, Bk5, Bk7)

2. Enable only the modules that you need for optimal result

ISA modules:
- I/E – Base integer
- M – Multiply and divide
- C – Compact ISA
- F – Single precision floating point
- and more...

Codasip modules:
- Jump predictor
- I/D cache
- AHB/AXI interconnect
- Type of multiplier/divider
- and more...

IP

Settings for IP.

Configuration

Configuration Value

| UARCH_NAME       | (bk1|bk3|bk5|bk7) |
|------------------|-------|
| DELIMITER        | -     |
| XLEN             | (32|64) |
| EXTENSION_E      | (I|E)  |
| EXTENSION_M      | [M]   |
CUSTOMIZE RISC-V AS YOU NEED

Codasip Studio:
- Introduced in 2014
- Silicon-proven by major vendors
- Allows for fast & easy customization of base instruction set:
  - Single cycle MAC
  - Floating point
  - Custom crypto functions
  - Non-standard data types
  - ... and many others

✓ Set the best ratio of power consumption and performance
✓ Easily add optional subsets and features
✓ Fine-tune the processor for intended application
✓ Differentiate and gain competitive advantage!

Codasip Studio
Integrated processor development environment

CodAL
Processor description language

element i_mac {
  use reg as dst, src1, src2;
  assembler { "mac" dst"," src1"," src2 }; assembler { "DP_MAC" dst src1 src2 0 }; assembler { rf(dst) = rf(src1) * rf(src2) };}

SDK Automation
Standards based tools & models

Verification Automation
VSP and processor validation

RTL Automation
Powerful High level Syntheses

Verilog 
VHDL
STRONG VERIFICATION METHODOLOGY

- Consistency checker
- Random assembler program generator
- UVM Verification Environment
  - Checking if RTL corresponds to specification which in our case is IA model definition
  - Environment in SystemVerilog generated automatically from Codasip Studio

Diagram:
- Instruction-accurate CodAL Processor Model
- Cycle-accurate CodAL Processor Model
- Test Cases
- Reference Model
- Synthesizable RTL
CODASIP STUDIO 7

Codasip Studio automatically generates all processor IP design kits and verifies for RISC-V compliance

✓ Prototype a core for a specific application domain
✓ Fast design space exploration
✓ Develop custom extensions

New in Studio 7:
✓ Support for LLVM 5.0
✓ Native AMBA interfaces
✓ Two-wire JTAG
✓ On-chip trace
SOFTWARE DEVELOPMENT: CODESPACE

SDK management
You can change the SDK for a software project with a few clicks

Profiler perspective
Integration with profiler tools directly in editors

Enhanced debugging perspective
You can view ports, signals, or pipeline

On-chip debugging
You can move a project from ISS to on-chip debugging within the same environment
WHY CODASIP

**Automation** allows for faster development

- Thanks to customization, Codasip can **create new RISC-V processor variants faster** than the competition, including modular ISA options
- Pre-verified software and hardware are **generated simultaneously**

**Optimization** allows for differentiation

- Customers can **add their own intellectual property** to RISC-V processors, tailoring it to their proprietary software
- **No other RISC-V vendor** offers this feature

**Innovation** allows for technology leadership

- R&D based in **Brno, Czech Republic**, a leading research and university region of Central Europe, providing top engineering talent