

S3S full day shortcourse on FDSOI design

San Francisco, Hyatt Regency on Oct 18th, 2018

Major Topics:

- FDSOI Fundamentals
- SRAM
- Body Bias Techniques
- FDSOI High performance
- Power management IPs
- Low Power SoC
- Automotive
- IoT
- EDA
- Analog, RF and ThZ

Abstract:

S3S is organizing a full day shortcourse about FDSOI intended for chip designers, technologists and new comers in the field. The tutorials will provide a wide overview of the advantages of FDSOI technology and how to efficiently design innovative circuits for key markets such as automotive and IoT. The lectures will be given by world renown experts from academia and industry. In each field, FDSOI state of the art design techniques and methodologies enabling the development of new and innovative IPs or products will be presented.

The tutorial day will be held in SF Airport, Hyatt Regency on Oct 18th, beginning at 8am and running until 6pm. Here's a quick preview at what each speaker will be addressing during the FDSOI Shortcourse. In addition to the following lectures, EDA vendors, IP vendors and foundry technologists will be available for in-depth discussions during break-outs."

Agenda:

08:00 – 08:20: Welcome & Registration

08:20 – 08:30: Short course introduction

- *Philippe Flatresse*

08:30 – 09:15: FD-SOI: how material & design innovations enable new market opportunities

- *Manuel Sellier, PhD, SOITEC*

09:15 – 10:00: Enabling Ultra-Low Vmin SRAM Operation in FDSOI technology

- *Rossella Ranica, PhD, STMicroelectronics*

10:00 – 10:30: Coffee break

10:30 – 11:15: High performance design of ARM CORTEX-A53 based SOC using GLOBALFOUNDRIES® 22FDX™

- *Jia Niu, Globalfoundries*

11:15 – 12:00: Power management IPs in FDSOI for best in class energy efficiency SOCs targeting IoT, Automotive and computing applications.

- *Lionel Jure, Dolphin Design*

12:00 – 13:30: Lunch

13:30 – 14:15: ID-Xplore: A disruptive EDA for emerging applications of FDSOI technology

- *Ramy Iskander, PhD, Intento*

14:15 – 15:00: FDSOI Pre-Silicon PPA Optimization Leveraging Adaptive Body Bias

- *Holger Eiseinreich, Racyics*

15:00 – 16:00: Coffee break

16:00 – 16:45: FDSOI technologies pave the way to reliable, safety-critical automotive products

- *Vincent Huard, PhD, SOITEC*

16:45 – 17:30: mmW and THz design considerations in FDSOI

- *Hani Sherry, TiHive*

17:30 – 18:00: Wrap up

Abstracts:

FD-SOI: how material & design innovations enable new market opportunities

- *Manuel Sellier, PhD, SOITEC*

Material innovation is at the heart of FD-SOI technology. The very thin and uniform FD-SOI substrate not only boosts the intrinsic performance of the circuit, but also opens the way to new design techniques with the full control of the transistor threshold voltage through the back bias. Something that was before fixed by process is now settable by design. This combination of material and design innovation is now bringing value for a growing number of applications including the Internet of Things (IoT) with ultra-low-power Nb-IoT devices with integrated RF, automotive systems from vision processors for ADAS to infotainment, and mobile connectivity from 5G smartphones to wearable electronics. We will review in this talk what are the key disruptions brought by FD-SOI technology and their benefits at the application point of view.

Enabling Ultra-Low Vmin SRAM Operation in FDSOI technology

- *Rossella Ranica, PhD, STMicroelectronics*

An extensive study of key parameters impacting SRAM Vmin and guidelines for its efficient lowering in FDSOI technology will be presented. The challenges to guarantee End-Of-Life SRAM Vmin according to products usage conditions and memory capacity will be discussed. The path towards Ultra Low-Leakage applications thanks to FDSOI technology and Body-Bias technique will be shown.

High performance design of ARM CORTEX-A53 based SOC using GLOBALFOUNDRIES® 22FDX™

- *Jia Niu, Globalfoundries*

This article describes how to implement a high performance design with Quad-cores ARM A53 based SOC by using Forward Body-Biasing(FBB) feature of 22FDX™ technology. Also the results of this design has been silicon proven using Dhrystone benchmark.

Power management IPs in FDSOI for best in class energy efficiency SOCs targeting IoT, Automotive and computing applications.

- *Lionel Jure, Dolphin Design*

The energy efficiency becomes a primary concern for both emerging market as IoT and mature markets like automotive and mobile. Combined to a trend to have heterogeneous requirement in term of computing power, it turns to a real challenge to design energy efficient circuit with limited possibilities for playing with voltage level.

Fortunately, the introduction of FD-SOI technology provides another lever to overcome this challenge: body-biasing. In this talk, we will present some mechanism of power optimization using combination of power supply level and body-biasing. We then discuss challenges around their industrial usage prior to give some insight on their implementation. Finally, we will present power management solutions and illustrate how it may contribute to design energy efficient edge-node devices.

ID-Xplore: A disruptive EDA for emerging applications of FDSOI technology

- *Ramy Iskander, PhD, Intento*

A design migration case of the clock buffer for a ping-pong ADC will be presented. It will be shown that ID-Xplore™ can rapidly migrate the buffer to satisfy the time skew mismatch and the calibration range specifications in 22FDX FDSOI technology, using the dynamic body biasing technique.

FDSOI Pre-Silicon PPA Optimization Leveraging Adaptive Body Bias

- *Holger Eiseinreich, PhD, Racyics*

Adaptive Body Bias (ABB) is mostly used post-silicon to compensate process, temperature and slow voltage variations to optimize performance and power of products implemented by a worst case design approach. This talk presents a methodology and the related IP components to leverage ABB already during the pre-silicon implementation and sign-off phase to significantly improve PPA of FDSOI products. A turnkey ABB IP platform for GLOBALFOUNDRIES' 22FDX (22nm FDSOI) will be introduced, which guarantees yield for performance and power at sign-off time. Furthermore it enables 22FDX ULV implementations down to 0.4V operating reliable over a large temperature range (-40C ... 125C). Besides MCU PPA study results the talk includes 22FDX silicon measurements and volume test statistics.

FDSOI technologies pave the way to reliable, safety-critical automotive products

- *Vincent Huard, PhD, SOITEC*

In the last decade, automotive products have been pushed forward to advanced CMOS nodes with an accelerated pace, mostly driven by the needs for new applications like Autonomous Driving. In parallel, automotive markets are regulated by various reliability and safety norms like AEC-Q100 and/or ISO26262. Finally, the mission profiles of the products are very diverse and are generally very demanding in terms of voltage and temperature excursions as well as in failure rate (typically <1ppm).

This course will show how FDSOI technologies present superior advantage compared to other technologies to enable such high-performance critical applications. This advantage is two-fold. On one hand, the technology itself presents features which makes it a good match for such applications. On the other hand, FDSOI offers with body-bias knob through a joint design/test approach a unique feature to manage at anytime reliability and safety altogether with limited performance penalty.

mmW and THz design considerations in FDSOI

- *Hani Sherry, PhD TiHive*