CUSTOMER CASE STUDY - MIGRATION AND CENTERING OF AN SAR ADC

MOVING AN 11-BIT SAR ADC, PART OF A WIFI TRANSCEIVER, TO A 28nm PROCESS NODE

A customer project to migrate an existing WiFi transceiver design to a 28nm process required careful tuning of the ADC subsystem. Thalia deployed its Reuse Platform as a Service (RePaaS) - combining advanced methodology, proprietary design automation and proven analog expertise - to port and center the design, achieving final results in less than six weeks, a timescale 30-40% shorter than would have been possible using traditional methods

Business issue and need

As more and more devices connect to the Internet, the need for small and power-efficient wireless transceivers is on the rise. As a consequence, RF system designers are today faced with the challenge of designing the most power-efficient, smallest yet configurable RF transceivers. For moderate speed and resolution applications, low-power and area-efficient SAR ADCs are commonly used.

The SAR ADC (Figure 1) was part of a WiFi IP that Thalia's customer was migrating to a 28nm node. The key specifications of the ADC portion are listed overleaf, (Table 1).

The main functional blocks in this SAR ADC design were a binary-weighted capacitive DAC, a comparator, and digital control logic.

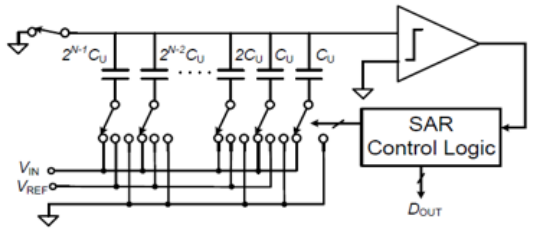

Figure 1: the ADC included a binary-weighted capacitive DAC, comparator, and control logic

Thalia's solution

As the first step in the porting process, Thalia deployed its AMALIA schematic porting toolset to migrate the WiFi IP to a 28nm technology. This process, if done manually, would have taken several weeks, if not months. Thalia was able to generate the schematics of the migrated IP in a fraction of this time. The schematics were error free and readily usable for verification.

For moderate-to-high resolution capacitive DACs, thermal noise is not a limiting factor, but a greater concern is matching of the capacitors. For a binary-weighted capacitive array, the mismatch effect can impact the DNL/INL specifications. The matching property of the capacitors is inversely proportional to the square-root of the capacitor area. So as part of the mapping process, care was taken to to identify capacitors with similar mismatch values in the destination technology. Since in this design, the DAC determines the DNL/INL specifications of the ADC, the DAC was simulated extensively.

The other important block in the SAR ADC was the dynamic latch comparator. This design is seen often in ADC configurations due to its power efficiency. Noise specifications of the comparator had to be checked and any issues due to the thermal noise current of the input transistors and/or thermal noise from reset switches needed to be accounted for. Issues related to noise non-compliance were addressed by deploying the AMALIA design centering capability and an experienced resource.

Once the DAC, comparator and digital logic were independently verified, the next step was to check top-level compliance of the complete design. Thalia checked for ENOB, DNL/INL requirements and current consumption. This was a system-level check: since extensive block-level verification and tuning had already been performed, there was reasonable confidence in the compliance to the top level specifications.

Finally, Thalia deployed automation scripts to generate the baseline layout framework in the destination technology. Thalia delivered verified design schematics and layout in the 28nm technology the customer requested in less than six weeks.

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ADC MIGRATION CASE STUDY

Summary and conclusion

The customer required the complete WiFi IP to be migrated in 30-40% shorter time than conventional approach, and using its RePaaS solution, Thalia was able to achieve this.

Thalia's approach to efficient analog IP reuse involves the deployment of targeted automation and highly capable design expertise. Thalia employed design automation in migrating the schematics of the SAR ADC to a 28nm technology and in the process saved the customer several person-weeks of effort, as well as substantially reducing the calendar timeline of the complete project.

Specification point	Specification			Units
	Min	Nom	Max	
General				
vdd_unreg				V
vdd0v9				V
Sample rate		1		MS/s
Temperature range	-40	27	110	°C
Input range				V
Top-level				
ENOB (Pre+Post)	10.9	11.0	11.0	bits
DNL (Post)			1	LSB
INL (Post)			2	LSB
Area				mm^2
Current consumption				
vdd_unreg (pre)		103	150	µA
Current consumption				
vdd0v9 (Pre)		93	492	µA
Co-sim				
ENOB (Pre)	10.6	10.9	10.9	bits
Voltage of Vcm (Pre)	453.5	457.8	465.2	mV
Block-level				
DAC total array capacitor		4.5		pF
DAC DNL (Post)			0.5	LSB
DAC INL (Post)			0.5	LSB
Comparator input-referred noise (Pre)	53	81	106	µV
Comparator input-referred offset (Pre)		6.7		mV
Comparator systematic offset (Post)				µV
Comparator speed (Pre+Post)	0.4	0.9	4.5	ns
On resistance of top-plate switch (Pre+Post)	1.15	1.37	2.16	kOhm
Voltage droop during conversion Pre+Post)	0.2	0.4	45	µV
Voltage of Vcm (Pre+Post)	449.7	450.3	451.3	mV

Design automation was also used to identify potential solutions at block level. The goal of automation was to quickly identify a candidate solution that an experienced designer could expand upon.

The design was checked for compliance and tuned at the block level, and for design compliance at the system level.

By intelligently deploying targeted automation, Thalia was able to substantially reduce the time taken to migrate, verify and center the design.

Thalia delivered both schematics and layout in DFII format and the effort was completed in less than 6 weeks - reducing the overall project cost, ensuring quality of result, and helping to hit a critical time-to-market window.

More details about our schematic porting capability are available in a separate case study. Click here

THALIA'S RePaaS solution

Thalia's unique approach to customers' analog and mixed signal design projects is encompassed in its Reuse Platform as a Service (RePaaS) offering.

RePaaS combines the use of AMALIA - our proprietary and highly innovative design automation technology - with the experience and expertise of our design team, and advanced development methodology.

This unique combination allows us to cost-effectively undertake development projects on behalf of our customers, with multiple benefits:

- Faster project turnaround
- More cost-effective than using customers' internal engineering resource
- Allows internal teams to focus on innovation/value-add

The AMALIA design enabling software:

- Automates device-level simulation and analysis between technologies and passes results to the porting software
- Ports schematics from one technology/node to another
- Supports our design team in validating and centering the design post migration
- Enables the generation of circuit variants: eg low power, different loads, or area-optimization
- Enables rapid qualification of the circuit topology in a new process node
- Facilitates analysis and understanding of the impact of trading off circuit characteristics

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