cadence®

Tensilica Vision DSP Family

High-performance, low-energy image/vision/NN processing

The Cadence® Tensilica® Vision digital signal processor (DSP) family is designed for demanding imaging, computer vision, and neural network (NN) applications in the mobile, automotive, surveillance, gaming, drone, and wearable markets. The Vision P5 DSP and the Vision P6 DSP are our two imaging- and computer vision-specific products that establish a new standard in high-performance, low-energy digital signal processing. With addition of the Vision C5 DSP, we now have a member designed specifically for NN processing. Plus, since all our DSPs are built on the highly successful Cadence Tensilica Xtensa® processor, the Vision DSP family shares the same development environment.

Overview

For sufficient pixel processing throughput, the Vision DSP family architecture incorporates advanced VLIW/SIMD support for the industry's highest number of ALU and MAC operations per processor cycle, as well as the industry's widest and most flexible memory bus.

Specialized instructions also allow the Vision DSP family to efficiently speed up pixel processing. In our Vision C5 DSP, we have given significant focus on optimized implementation of all the layers of a NN rather than just the convolution layer. These instructions were optimized in close collaboration with a number of customers and partner companies and after detailed profiling of key imaging, vision, and NN applications.

Various architecture enhancements boost the performance while keeping the energy consumption low. The Vision DSP family provides unprecedented flexibility in system implementations at power-consumption levels that significantly reduce the need for hardware accelerators. The DSPs also offer an integrated DMA engine, interface for instruction memory, instruction cache, and two AXI interfaces. It offers industry's widest data memory bus of 1024-bit. In the Vision P5 and P6 DSPs, we also offer an optional vector floating-point unit.

		Vision P5	Vision P6	Vision C5
Use Case		**Imaging**	**Imaging and low-end NN**	**Mid- and high-end NN (Always-on NN)**
MACs	8x8	64	256	1024
	8x16	64	128	
	16x16	32	64	512
VFPU	16b half precision	No	32-way SIMD (optional)	No
	32b single precision	16-way SIMD (optional)		No
MAX SIMD Width		64-way 8-bit		128-way 8-bit
SuperGather		Yes		No
Data Rearrangement–Efficient switch		Limited		Extensive
Coefficient Decompression - Saves memory bandwidth		No	Yes	Yes
AXI Interface - More AXIs = less sharing and higher memory bandwidth		2 AXIs 128b bus bandwidth for instruction and data		

Vision DSP Family Features and Benefits

- Provides a high-performance, energy-efficient imaging, vision, and NN embedded DSP
- Implements 64-way 8-bit SIMD on Vision P DSPs and 128-way 8-bit SIMD on Vision C DSPs with multiple VLIW slots
- Achieves up to 1.1GHz on 16nm process technology
- Only DSPs in the industry to offer 1024-bit memory bus for transferring the high-resolution data associated with today's imaging systems
- Provides a complete subsystem using the integrated DMA that allows the system to transfer high-resolution data directly into the local memory of the DSP, thus hiding the data access latency associated with accessing data from an external DRAM
- Implements the Tensilica SuperGather™ enhanced memory interface on Vision P DSPs to quickly and efficiently read/write non-contiguous locations from local memory
- Features an instruction set that's customized for better code density, fewer cycles, and lower power
- Provides a comprehensive software tool suite for quickly implementing high-performance imaging pipelines in C
- Features instruction-set extensibility for more algorithm-specific optimization via Tensilica Instruction Extensions (TIE)
- The Vision P DSPs deliver scalable, optimized performance with low energy for computer-vision and pixel-processing applications that span a large range of data types from 8b to 32b, such as face detection, object detection, lens distortion correction, and many more advanced vision applications
- The Vision C DSP delivers a efficient, flexible, scalable, and future-proof solution for the NN problem
- Optional vector floating-point unit (VFPU) in the Vision P DSPs offers flexibility to provide high-precision math at a minimal area penalty

Vision C5 DSP Features and Benefits

- Highest computational capacity in the industry
  - 1024 MACs
  - 128-way SIMD VLIW processor
  - Industry-leading wide 1024-bit memory interface with dual load/store
  - Integrated DMA
- Highly programmable and extensible
  - Flexible and future proof
  - Support for new layers as NNs evolve
  - On-the-fly decompression
  - Flexible instruction set for quantization
- Dedicated NN DSP that runs all NN layers
  - Eliminates moving data between Vision C5 DSP and main processor
  - Includes normalization and max pooling layers
  - Simple programming model
  - Simplified hardware architecture
- Architected for multi-processor clusters
  - Computation capacity and scalability for all NN applications and segments in surveillance and automotive

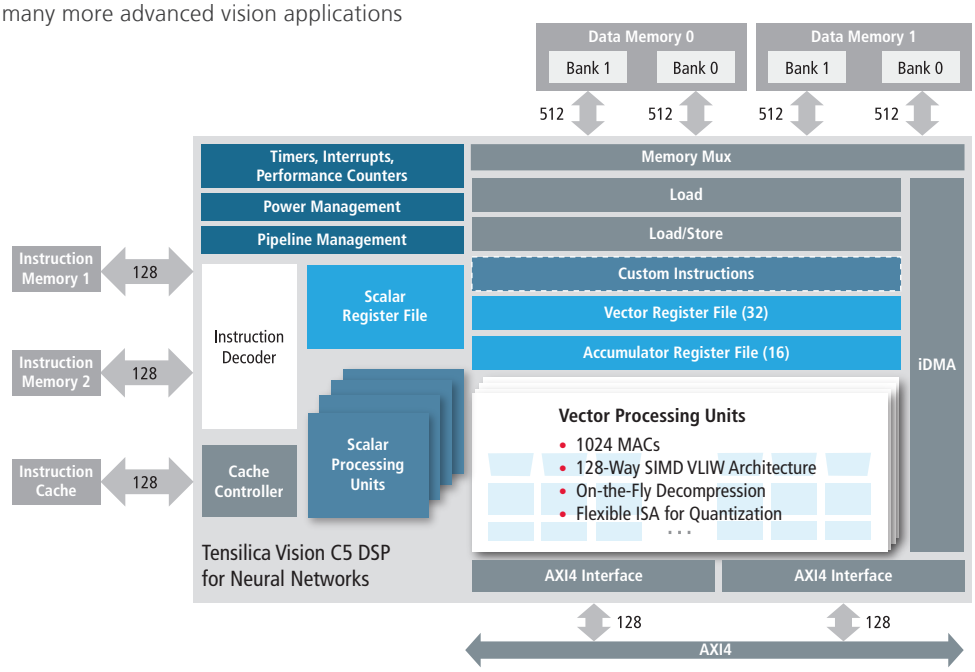

Figure 1: Vision C5 DSP block diagram

Vision P6 DSP Features and Benefits

- Processes 9728 bits per cycle
- Offers 256 MACs: 4X MACs compared to Vision P5 DSP
- Enhanced instruction set
- Smart instruction slotting
- Supports SuperGather enhanced memory interface
- Optional VFPU with single-precision (32-bit) floating-point and half-precision (16-bit) floating-point support offers flexibility to port GPU code and high-precision math at a minimal area penalty

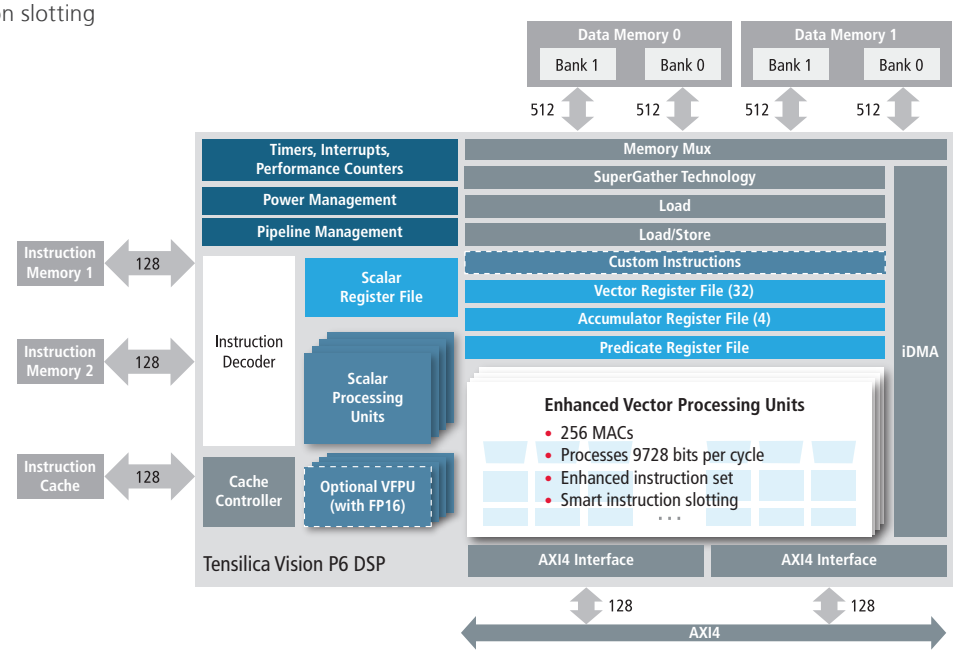

Figure 2: Vision P6 DSP block diagram

Vision P5 DSP Features and Benefits

- Offers up to 13X vision-processing performance improvement over the highly successful IVP-EP DSP
- Processes 7168 bits per cycle
- Supports SuperGather enhanced memory interface
- Optional VFPU with single-precision 32-bit floating-point support offers flexibility to provide high-precision math at a minimal area penalty

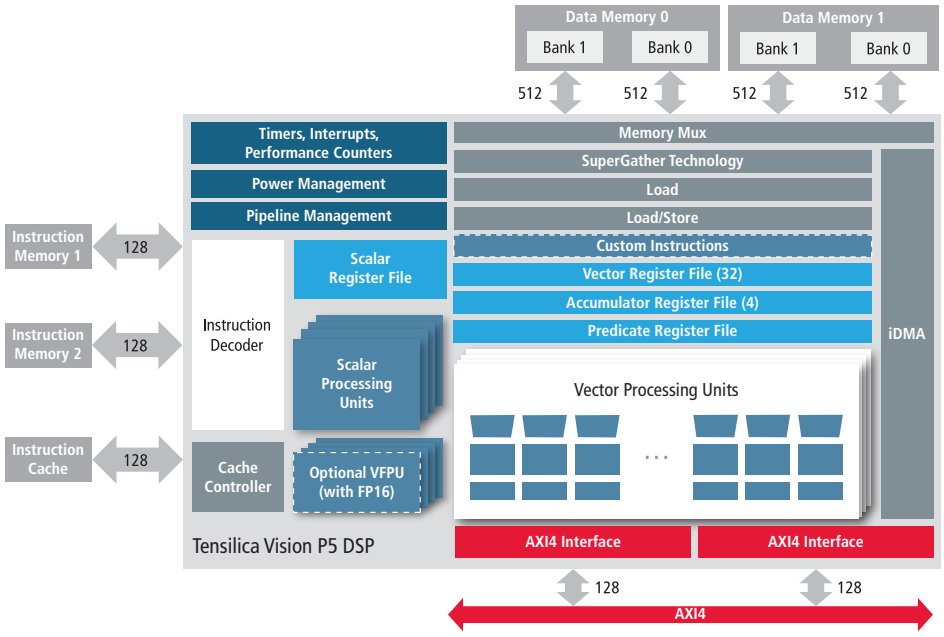

Figure 3: Vision P5 DSP block diagram

Library Support

- Vision P DSPs offer highly optimized OpenCV-based library functions, which can accelerate applications development
- Vision P DSPs offer OpenVX-based support to enable fast application development in a heterogeneous environment
- Offers highly optimized NN library on Vision P6 DSP and Vision C5 DSP

Toolchain

The Vision DSPs are delivered with a complete set of software tools:

- A high-performance C/ C++ compiler with automatic bundling and vectorization supports the VLIW and SIMD capabilities.
- Linker, assembler, debugger, profiler, and graphical visualization tools are included.
- A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance.
- When working with large systems or lengthy test vectors, the fast, functional TurboXim simulator achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification.
- Tensilica Xtensa Modeling Protocol (XTMP) for system modeling in C and Xtensa SystemC (XTSC) for system modeling in SystemC provide for full-chip simulations. The pin-level XTSC model offers co-simulation of the SystemC model at the pin level for fast, cycle-accurate system simulations.
- The Vision C5 DSP and the Vision P6 DSP come with the Cadence neural network mapper toolset, which will map any neural network trained with tools such as Caffe and TensorFlow into executable and highly optimized code for both DSPs, leveraging a comprehensive set of hand-optimized neural network library functions.
- All major back-end EDA flows are supported.

Cadence Services and Support

- Cadence Tensilica application engineers can answer your technical questions, and provide technical assistance and custom training.
- Cadence certified instructors teach a series of courses on Tensilica IP and bring their real-world experience into the classroom
- Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- The Cadence Tensilica IP support site gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more at ip.cadence.com/support

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