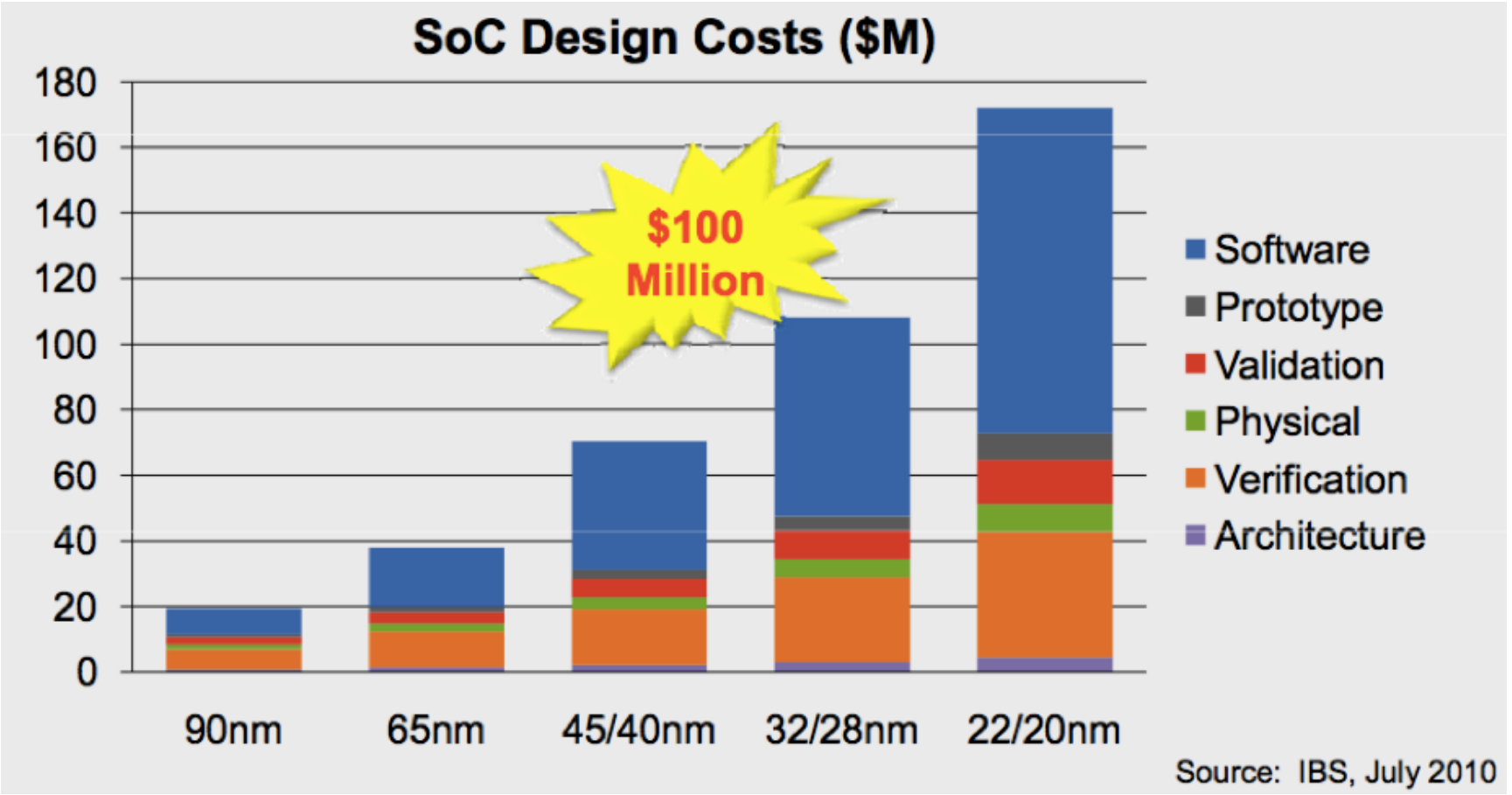
How and Why eFPGA Will Become Pervasive Over the Next Decade

D&R IP-SoC Grenoble 6 December 2017

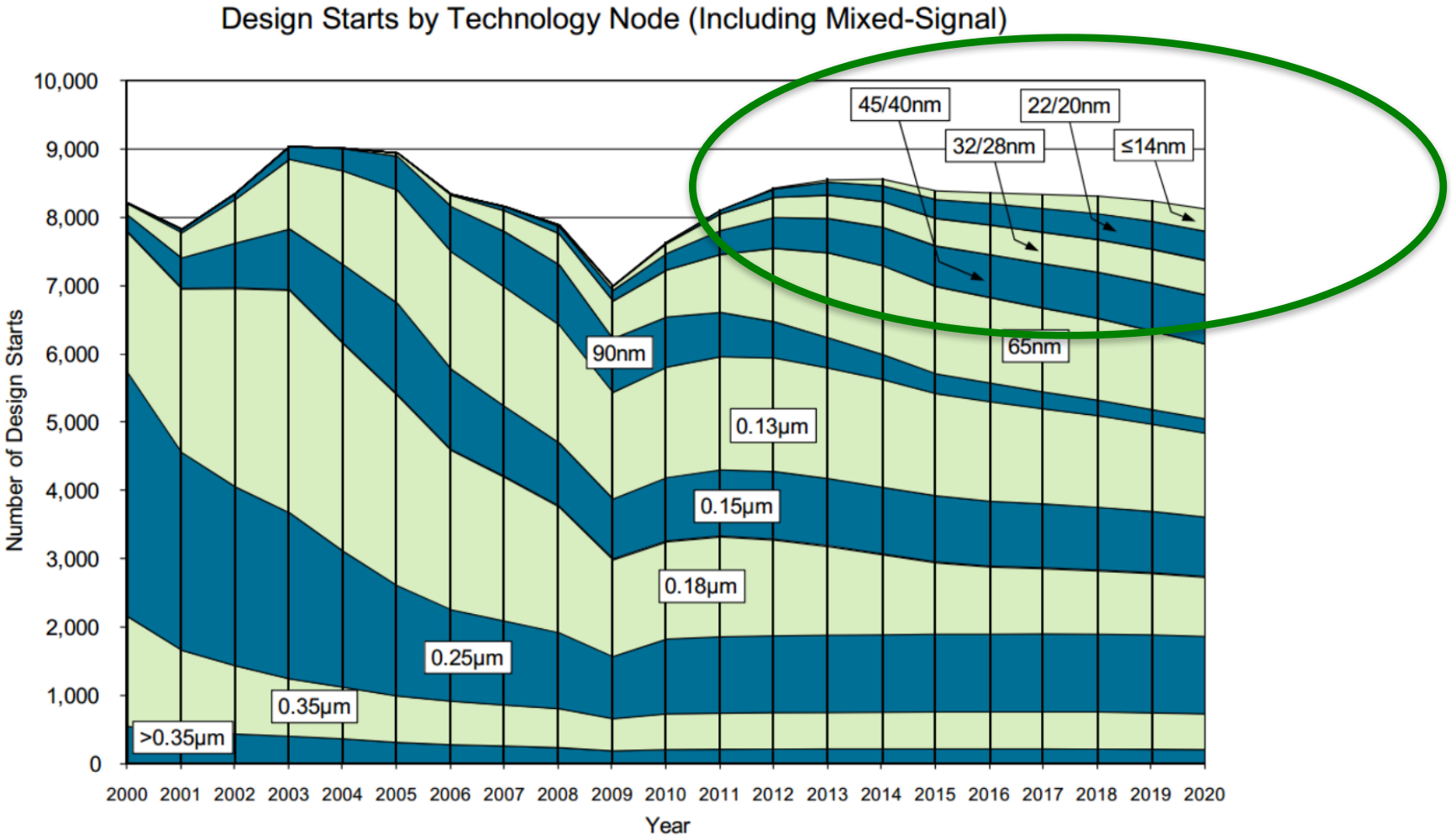
Chip Design Costs Escalating With Each Node



Mask costs: ~$1M for 40nm, ~$2M for 28nm, ~$5M for 16/14nm!

Engineering cost/complexity shifting full custom to high level design

Fewer Tapeouts On Advanced Nodes



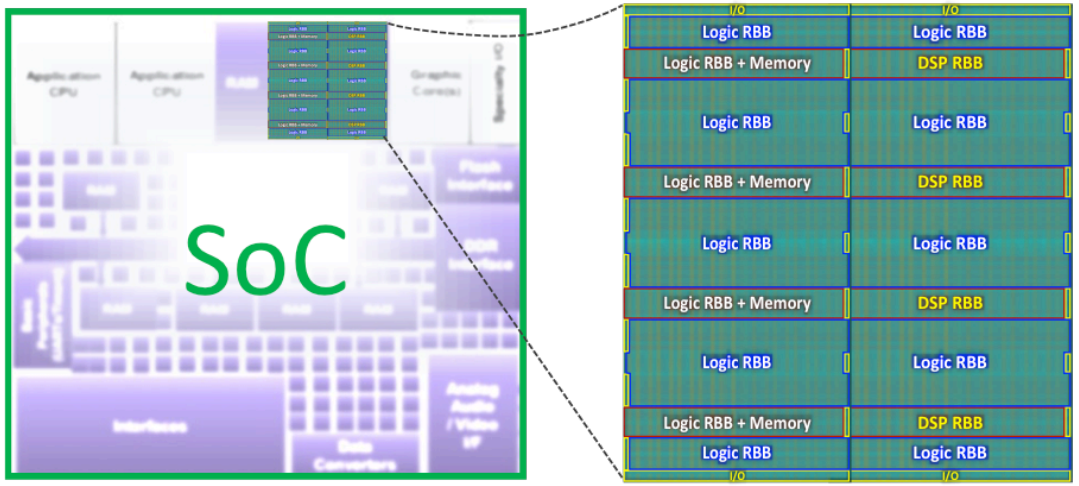
40+28+16/14nm: ~800 designs in 2016, ~1,300 in 2020

Chips Must Do More

- The Semiconductor TAM continues to grow
- The breadth of applications is increasing
- So fewer tape-outs means chips must do more by being programmable
- Processors are good and have become pervasive
- But FPGA provides a different type of programmability that can sometimes do what processors can't, e.g.
  - Parallelism
  - State machines
  - Low power without memory references

eFPGA Make ICs Flexible

- Reconfigure RTL in your SoC/MCU anytime
  - Keep up with changing algorithms, industry standards, and customer requests
  - One chip can serve multiple applications
  - Longer chip life, higher ROI
- Embedded FPGA IP can be used anywhere in a chip



Why Will eFPGA Succeed This Time?

- eFPGA has been tried many times in the last 20 years
  - Actel
  - IBM/Xilinx
  - LSI Logic
  - Leopard Logic
  - And more
- Found one product in last 20 years using eFPGA: Stretch
- Not sure why they failed
  - probably because they didn't meet the needs of the market

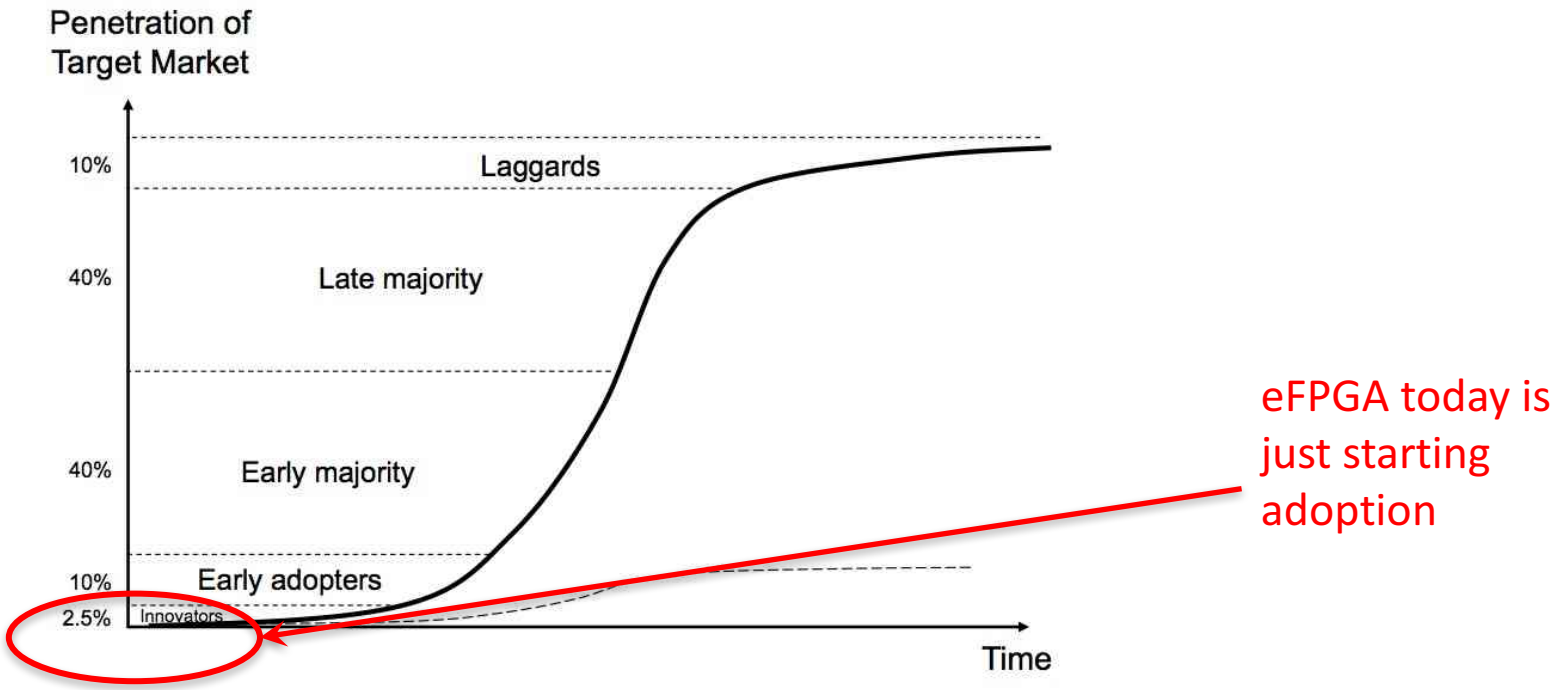
What Customers Need From eFPGA IP

- Available in the target process node and metal stack
- Density similar to FPGA chips in terms of LUTs/mm^2
- Proven in silicon
- Available in the size needed (# of LUTs)
- Available with DSP/MAC and/or RAM if required
- High I/O count for connecting to wide, fast buses
- Software to program with high speed & utilization

eFPGA ≠ FPGA

- FPGAs are designed every few years for each new process node and are optimized with full-custom logic and typically use maximum metal stacks
- eFPGA based on an FPGA may
  - Not be in the process variant the customer needs and be slow/expensive to port due to full-custom logic
  - Not be compatible with the customer's metal stack
  - Not be scalable in size to meet the customers' needs

New Technology Adoption Curve



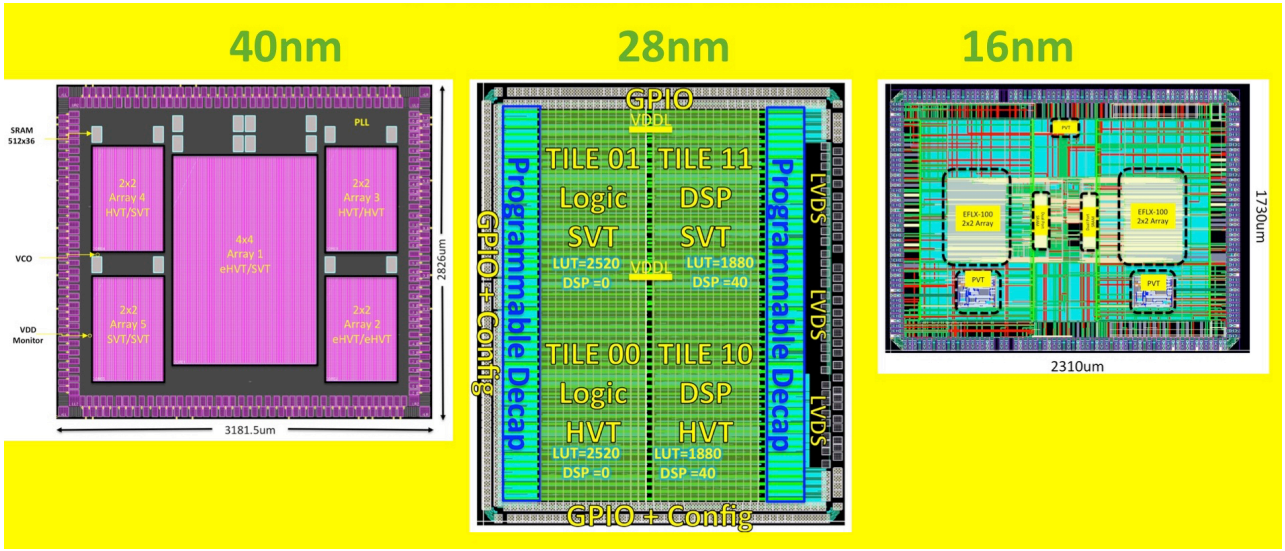
ARM took 5 years to get 5 customers

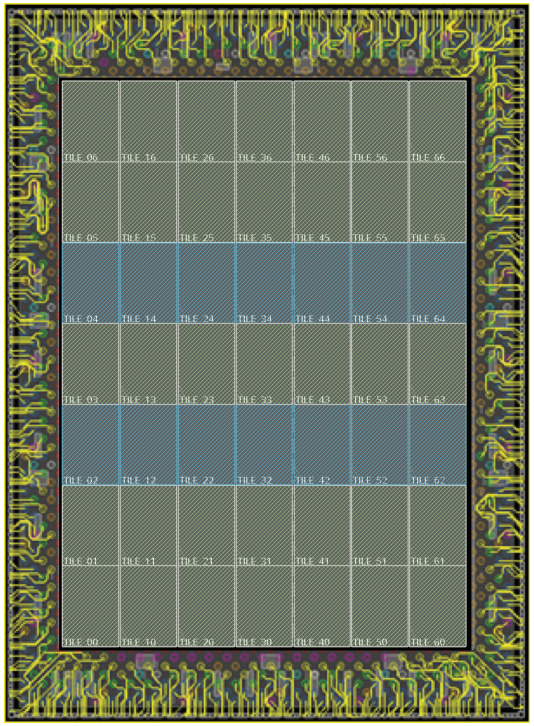
Rambus took 5 years to get Nintendo-64

eFPGA is at the start of a similar “S Curve”

eFPGA Now Available on Mainstream Nodes

16nm





Now Multiple eFPGA Suppliers

- Flex Logix
- Achronix
- Adicsys
- Efinix
- Menta
- QuickLogic

Multiple eFPGA Users Announced in 2017

- Four announced eFPGA users (all using Flex Logix)
  - DARPA for any US Government application in 16nm
  - Harvard University Deep Learning chip in 16nm
  - Sandia 180nm captive port for multiple products
  - SiFive customizable 28nm SoC and 180nm MCU platform chips
- More have prototypes and are in design

Sandia National Laboratories

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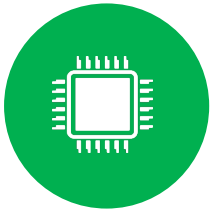
SiFive

Wide Range of Applications for eFPGA



Microcontroller/IoT

- Reconfigurable accelerators/DSP
- Reconfigurable Serial I/O
- Customer specific RTL
- Battery life extension

SOCs & ASICs

- Reconfigurable accelerators/DSP
- Deep Learning
- Algorithm iteration in real time

Aerospace/Defense

- Integration to reduce power, size, weight
- Manufacturing in US/Europe
- Rad-Hard eFPGA

Networking

- Reconfigurable protocols
- Programmable parsers
- Programmable NIC

Data Center

- Processor+FPGA
- Accelerators
- Programmable switch
- Programmable NIC

Wireless Base Station

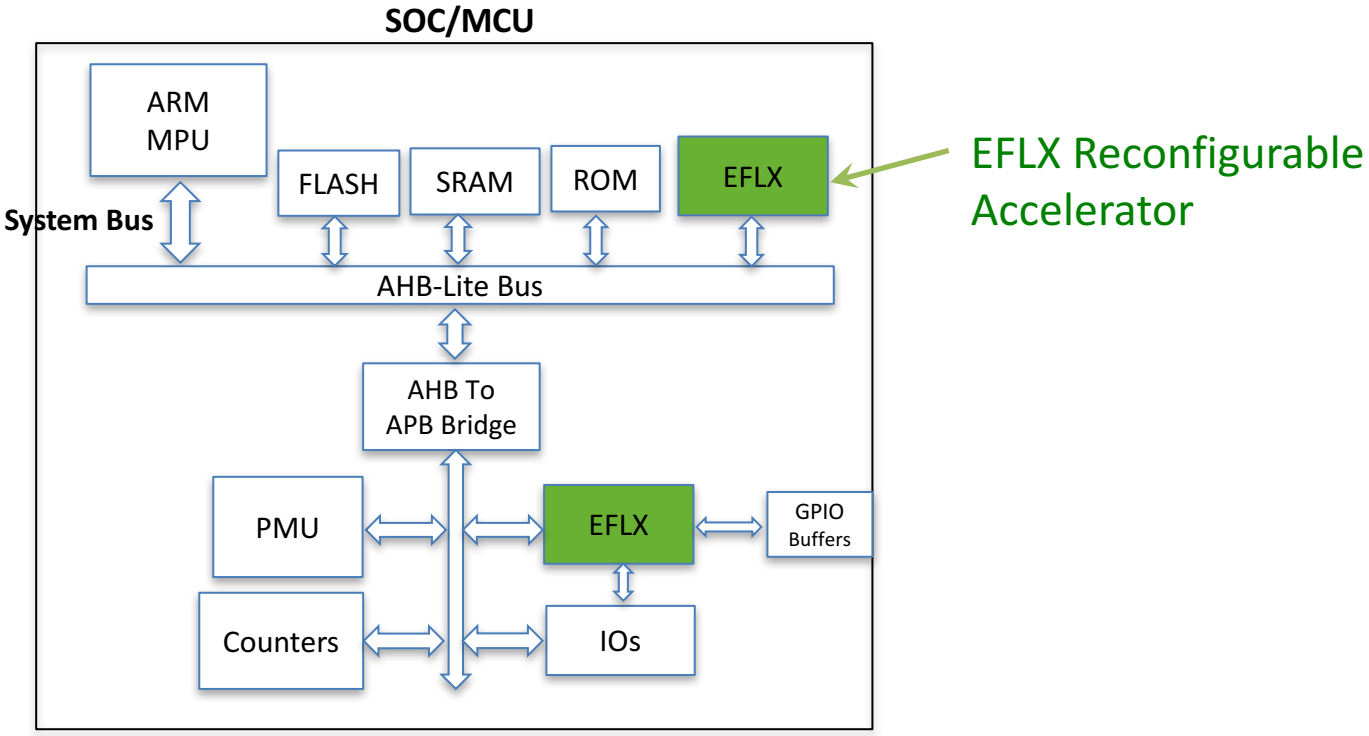
- Reconfigurable DFE (digital front end)

Aerospace/Defense Electronics

- Reconfigurability is critical for aerospace/defense systems given their long design cycles and long deployments
- eFPGA provides
  - Lower power
  - Smaller volume
  - Lower weight
  - US Fabrication
  - Even Rad-Hard for space applications

- DARPA believes embedded FPGA is strategic for defense ICs
- Sandia using eFPGA for multiple products in their 180nm fab

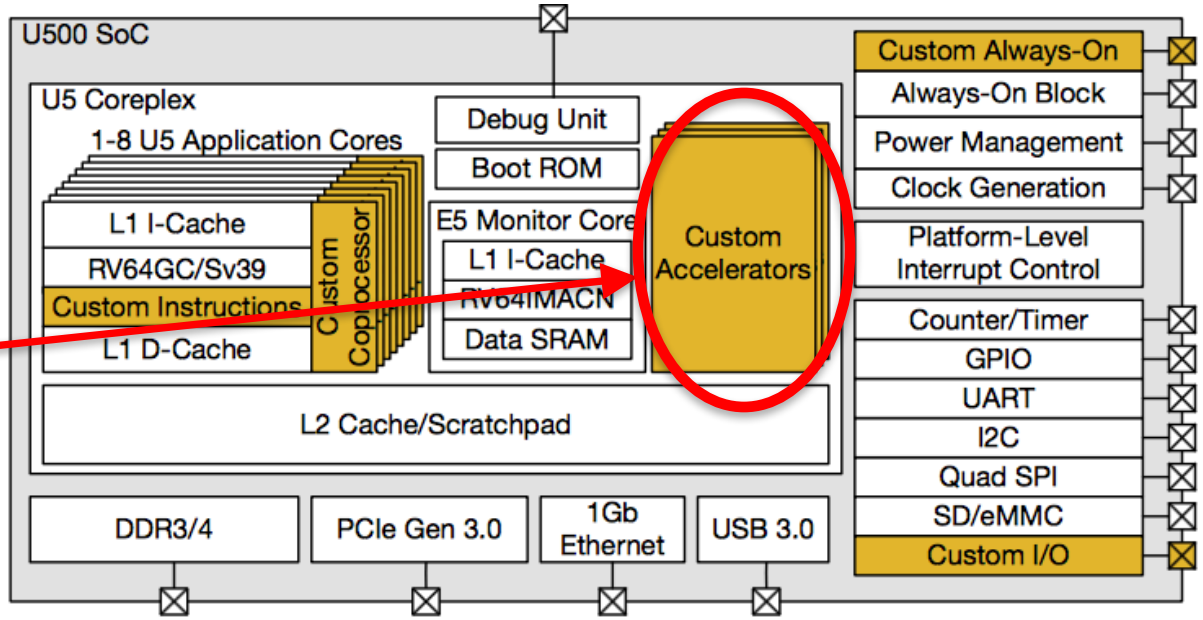
Reconfigurable Accelerator



eFPGA accelerates AES/SHA/JPEG/FFT 30-140x faster than ARM

eFPGA for SiFive SoC Platform Chips

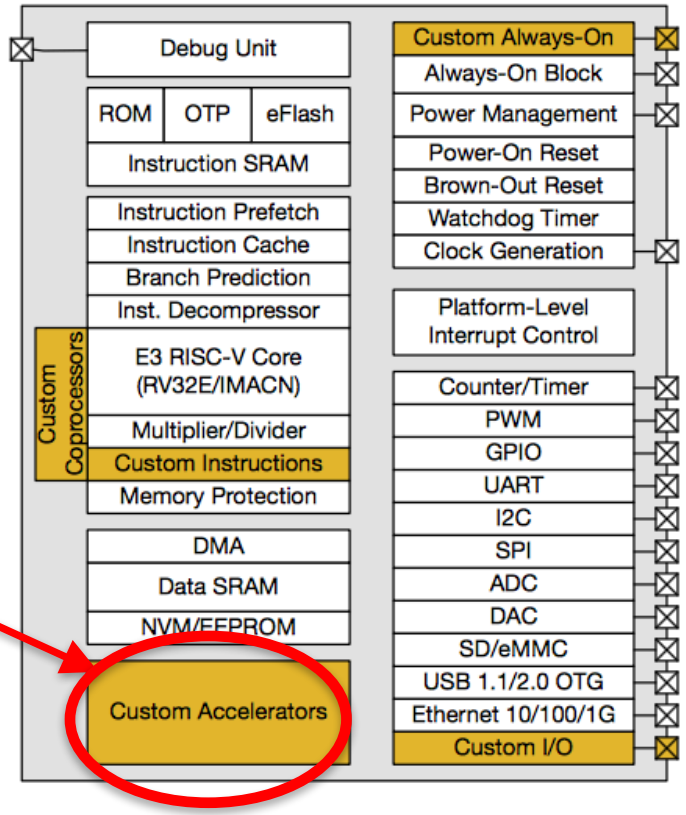
- Freedom U500
- Customizable 28nm SoC
- eFPGA: reconfigurable accelerator and up to 64 GPIO
- Platform chip in design with eFPGA



~$750K for customized U500 with eFPGA for ~100 package prototypes

eFPGA for SiFive MCU Platform Chips

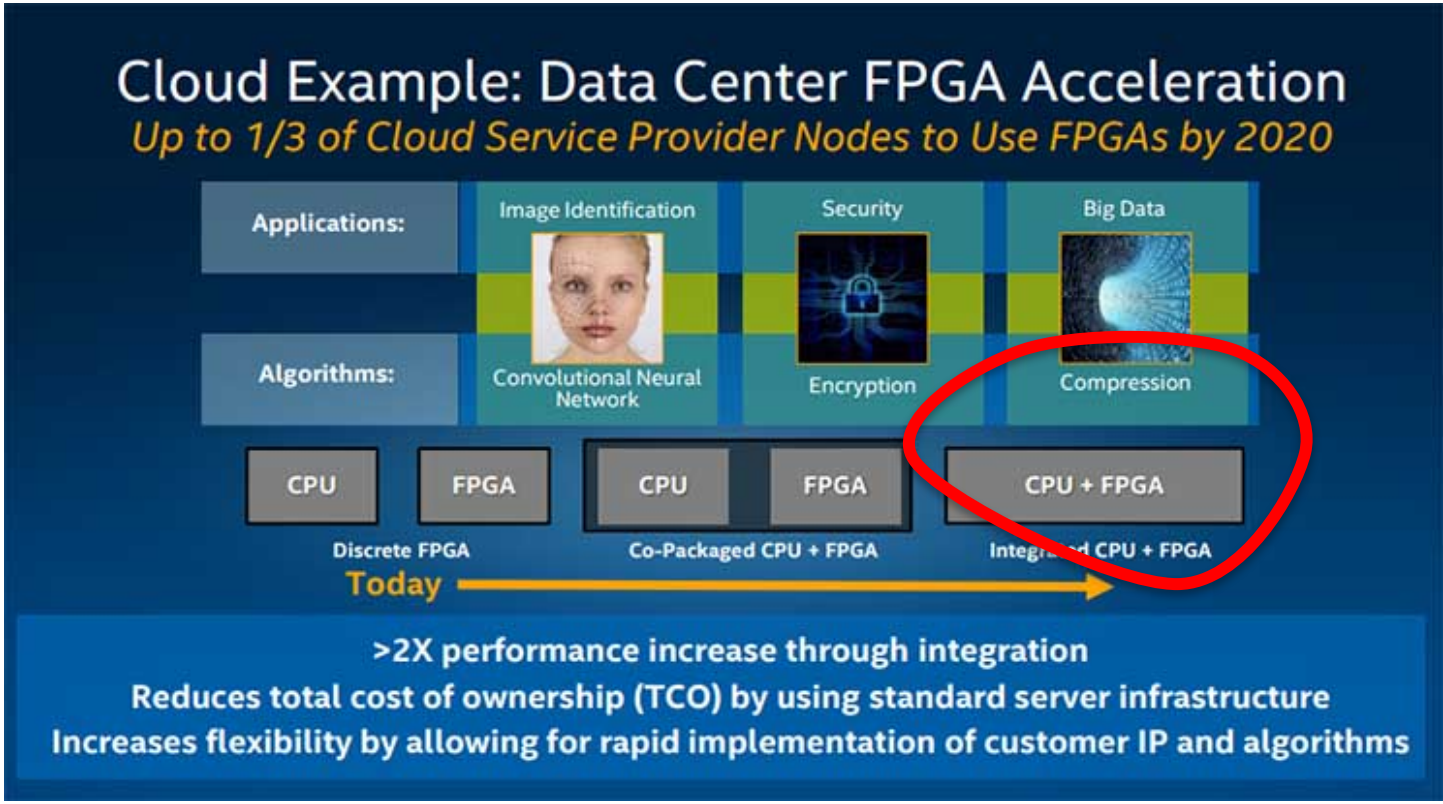
- Freedom U500
- Customizable 180 MCU
- eFPGA: reconfigurable accelerator and up to ~32 GPIO
- Will port T180 on demand



~$100K for customized U500 with eFPGA for ~100 package prototypes

Reconfigurable Cloud: Data Centers

- Reconfigure hardware protocols
  - Networking
  - Storage
  - Security
- FPGA Acceleration
  - Deep Learning
  - AI



Deep Learning / AI

- Harvard 16nm Deep Learning Chip with eFPGA in evaluation
- Professor Gu-Yeon Wei:
  - "Huge opportunity for reconfigurable logic in deep learning. Algorithms for deep learning change and improve quickly: with eFPGA we can iterate in real-time"

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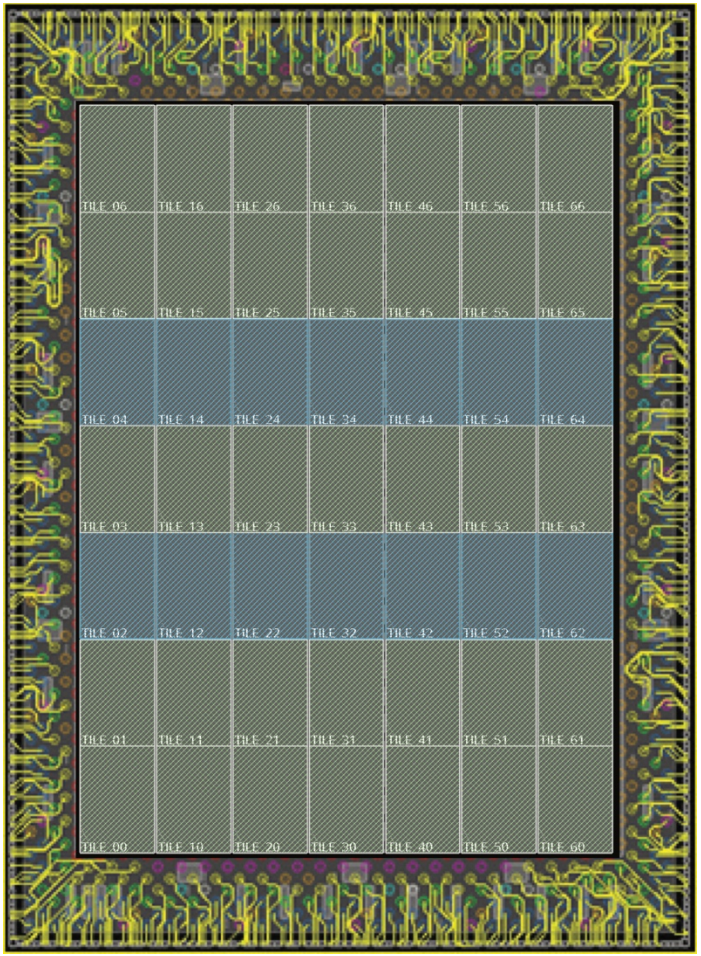
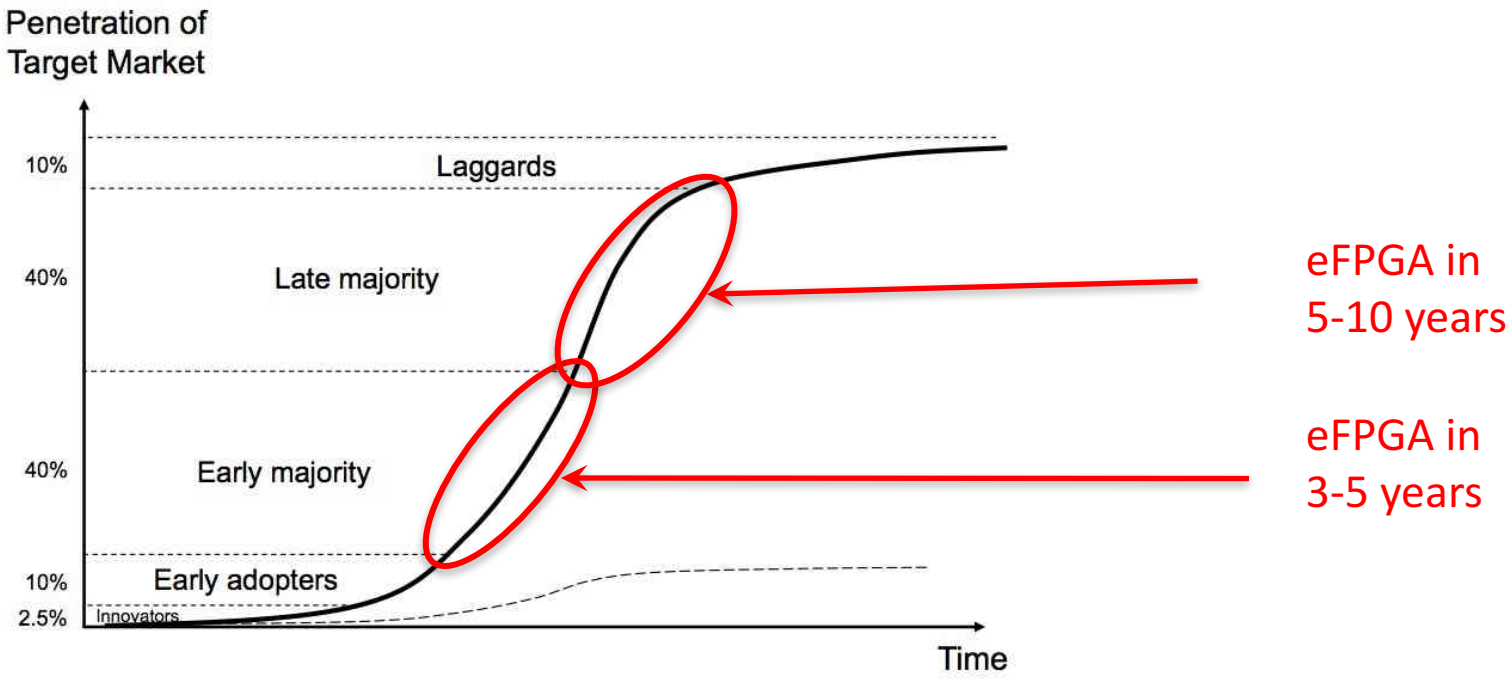
Very Large eFPGA Available

- EFLX200K in validation
- ~183K LUT4
- 560 22x22 MACs
- Multiple SRAM blocks, PLL & PVT monitors for testing >1GHz to validate all specs over temperature and voltage



eFPGA Will Become Pervasive



We have talked to 100s of customers

- >95% say “eFPGA is great, we will use it”
- >90% want to wait for others to go first
- When current customers go to production, adoption will take off

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