# The FDSOI history and its future

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### Our "digital" world in 2020



### **Power Efficient Technologies are mandatory**



# Choosing the right material is essential !

**Raw Material** 

**Engineered Material** 



### **Needs of fully-depleted transistors**



### **FD-SOI: more than 20 years success history**



### The electrical history of FDSOI

![](_page_4_Figure_1.jpeg)

### Soitec ensures FD-SOI wafer supply

![](_page_5_Picture_1.jpeg)

Soitec Bernin II, France HVM

![](_page_5_Picture_3.jpeg)

650 K wafers/y. capacity of which FD-SOI capacity will be increased from 100 K wafers/y. to 400 K wafers/y.

> Total potential 300mm capacity = Up to 1.5 M wafers/y.

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Pasir Ris, Singapore Ready HVM

![](_page_5_Picture_7.jpeg)

+ 800 K wafers/y. capacity (FD-SOI pilot line launch – Sept. 17)

![](_page_5_Picture_9.jpeg)

![](_page_6_Picture_0.jpeg)

![](_page_6_Picture_1.jpeg)

GF Chengdu fab announcement & fast construction

![](_page_6_Picture_3.jpeg)

Increasing number of products

15

12nm node announced with 7nm FF perf

![](_page_6_Picture_6.jpeg)

![](_page_6_Picture_7.jpeg)

![](_page_6_Picture_8.jpeg)

![](_page_6_Picture_9.jpeg)

Increasing number of products

![](_page_6_Figure_11.jpeg)

### FD-SOI at the heart of Samsung foundry strategy

![](_page_6_Picture_13.jpeg)

#### The winning combination

![](_page_6_Figure_15.jpeg)

#### 18nm announcement

	18FDS
Performance	1.2X
Power	0.60X
Logic Area	0.70X
Mask set (10MTL)	+5Layer

![](_page_6_Picture_18.jpeg)

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![](_page_7_Picture_0.jpeg)

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![](_page_7_Figure_1.jpeg)

![](_page_7_Figure_2.jpeg)

![](_page_7_Picture_3.jpeg)

# 22nm benchmark

	TSMC 28HPM-8T	TSMC 22ULP-7T	GF 22FDX-8T	intel 22FFL-7T
			104/80	108/90
CPP/Mx	126/90	108/90 (est.)	0.78x	0.92x
Die Scaling	1.0x	0.85X	36	>47
Masks	47	4/	1.55x	1.35x
Peri@iso-Pwr TT, 25C	1.0x	0.65x	0.30x	0.50x
D Cell Area (um²)	0.127	0.122	0.110	0.088
D SRAM Vmin (V)	0.81v	0.81 (HD cell) 0.60v (10T cell)	0.72v (HD cell) 0.65v (6T LV cell)	0.77v
imeline	Qualified	V1.0 in 1Q18	Qualified	Qualified 4Q17

# Is Body Bias really a Game Changer?

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![](_page_10_Picture_0.jpeg)

### **Body Bias as key differentiator for FDSOI**

![](_page_11_Figure_1.jpeg)

![](_page_12_Figure_0.jpeg)

![](_page_12_Picture_1.jpeg)

### **FD-SOI key features summary**

![](_page_13_Figure_1.jpeg)

### **FD-SOI ecosystem is getting stronger**

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![](_page_14_Figure_1.jpeg)

scitec

![](_page_15_Picture_0.jpeg)

### **FD-SOI for Automotive**

Best power efficiency allowing simpler integration and enhanced reliability

FD-SOI - Reference technology for ADAS level 3 applications

![](_page_15_Picture_4.jpeg)

![](_page_15_Picture_5.jpeg)

![](_page_15_Picture_6.jpeg)

![](_page_15_Picture_7.jpeg)

![](_page_16_Picture_0.jpeg)

## **FD-SOI for Internet of Things**

A game changer technology for better battery life

![](_page_16_Figure_3.jpeg)

![](_page_16_Picture_4.jpeg)

### **FD-SOI : 3 steps adoption**

![](_page_17_Figure_2.jpeg)

#### **Platform Versatility:** Energy Efficiency + Performance on Demand

![](_page_17_Picture_4.jpeg)

### Differentiation Options: RF, MRAM, ULP

![](_page_17_Figure_6.jpeg)

![](_page_17_Picture_7.jpeg)

### **Take-Aways**

![](_page_18_Picture_1.jpeg)

FDSOI is at the heart of every day life !

Power efficient & flexible technology with easy Analog/RF integration

**Power, Performance not forgetting cost** 

Engineered substrate brings clear value to device

This is just the beginning...