The FDSOI history and its future

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Our “digital” world in 2020

2020

4
BILLION
Connected People

$4
TRILLION
Revenue Opportunity

25+
TRILLION
Apps

25+
BILLION
Embedded and Intelligent Systems

50
TRILLION
GBs of Data

Power Efficient Technologies are mandatory

Source: IDC
Choosing the right material is essential!

Needs of fully-depleted transistors
FD-SOI: more than 20 years success history

Flexibility, scalability and innovation: the success story of Silicon-on-Insulator (SOI) technology through key collaborations and achievements

- Smart Cut invention
- 1991
- SOITEC creation
- 1992
- 300mm Fab
- 1999
- Smart Cut Fab
- 2002
- UTBB
- 2009
- FDSOI prod
- @ GF, SEC, ST
- 2013 - 2014
- Multi-foundries adoption
- 2015
- R&D acceleration
- 2008 - 2012
- 3GHz+ AP
- 2017
The electrical history of FDSOI

- **Bulk Planar**
  - Electrostatic issues
  - ☹ High Sub-VT slope
  - ☹ High DIBL
  - ☻ Low Body Biasing Efficiency
- **PDSOI**
  - Electrostatic issues
  - ☹ High Sub-VT slope
  - ☹ High DIBL
  - ☻ Low Body Biasing Efficiency
  - ☻ History effect
- **ETSOI**
  - Electrostatic Recovery
  - ☺ Low Sub-VT slope
  - ☺ Low DIBL
  - ☻ Low Body Biasing Efficiency
- **UTBB**
  - Electrostatic Recovery
  - ☺ Low Sub-VT slope
  - ☺ Low DIBL
  - ☻ High Body Biasing Efficiency

**Substrate**

- Punch Through!
- Through Substrate
- Back Gate
Soitec ensures FD-SOI wafer supply

- Soitec Bernin II, France HVM
- 300mm SOI
- 650 K wafers/y. capacity of which FD-SOI capacity will be increased from 100 K wafers/y. to 400 K wafers/y.
- + 800 K wafers/y. capacity (FD-SOI pilot line launch – Sept. 17)

Total potential 300mm capacity = Up to 1.5 M wafers/y.

Pasir Ris, Singapore Ready HVM
FD-SOI focus stronger than ever

GF Chengdu fab announcement & fast construction

Increasing number of products
The winning combination

FD-SOI at the heart of Samsung foundry strategy

18nm announcement

<table>
<thead>
<tr>
<th>Performance</th>
<th>1.2X</th>
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</thead>
<tbody>
<tr>
<td>Power</td>
<td>0.60X</td>
</tr>
<tr>
<td>Logic Area</td>
<td>0.70X</td>
</tr>
<tr>
<td>Mask set</td>
<td>+5Layer</td>
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### 22nm Benchmark

<table>
<thead>
<tr>
<th></th>
<th>TSMC 28HPM-8T</th>
<th>TSMC 22ULP-7T</th>
<th>GF 22FDX-8T</th>
<th>Intel 22FFL-7T</th>
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</thead>
<tbody>
<tr>
<td>CPP/Mx</td>
<td>126/90</td>
<td>108/90 (est.)</td>
<td>104/60</td>
<td>108/90</td>
</tr>
<tr>
<td>Die Scaling</td>
<td>1.0x</td>
<td>0.85x</td>
<td>0.78x</td>
<td>0.92x</td>
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<tr>
<td>Masks</td>
<td>47</td>
<td>47</td>
<td>36</td>
<td>&gt;47</td>
</tr>
<tr>
<td>Perf@iso-Pwr TT, 25C</td>
<td>1.0x</td>
<td>1.20x</td>
<td>1.55x</td>
<td>1.35x</td>
</tr>
<tr>
<td>Pwr@iso-Perf TT, 25C</td>
<td>1.0x</td>
<td>0.65x</td>
<td>0.30x</td>
<td>0.50x</td>
</tr>
<tr>
<td>HD Cell Area (um²)</td>
<td>0.127</td>
<td>0.122</td>
<td>0.110</td>
<td>0.088</td>
</tr>
<tr>
<td>HD SRAM Vmin (V)</td>
<td>0.81V</td>
<td>0.81 (HD cell)</td>
<td>0.72V (HD cell)</td>
<td>0.77V</td>
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<tr>
<td></td>
<td></td>
<td>0.60V (10T cell)</td>
<td>0.85V (6T LV cell)</td>
<td></td>
</tr>
<tr>
<td>Timeline</td>
<td>Qualified</td>
<td>V1.0 in 1Q18</td>
<td>Qualified</td>
<td>Qualified 4Q17</td>
</tr>
</tbody>
</table>
Is Body Bias really a Game Changer?
YES!
Body Bias as key differentiator for FDSOI

**Take the control of your circuit**
- Leakage reduction
- Performance Boosting

**Do it dynamically!**
- Dynamically switch between high perf & low leakage

**Take the control of your process**
- Offset process variation

**Operate safe at the edge**
- Adaptive Body Bias

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Energy management

Compensation
Body Bias gain per market segment

- Performance Boost: +200%, +50%, +20%
- Power Reduction: 10X, 2X, 1.5X

Benchmark vs noBB

High Perf | Energy Efficiency | Low Power | Ultra Low Voltage

soitec
FD-SOI key features summary

- **mmWave RF-CMOS**
- **Ultra Low Voltage**
- **Process compensation through body bias**
- **Immunity to radiations**

- Best CMOS mmWave with similar performance to SiGe radios
- Operation at minimum energy point (<0.4V)
- 4X less process spread
  +15% frequency boost
- 20x Soft Error Rate improvement vs. bulk

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- **Performance**
  - 400GHz fMax
  - 24.8 pJ (0.50V, 3 MHz)
  - 13.4 pJ (0.35V, 14 MHz)

- **Neutron SER in FT/Mb**
  - ST Vendor A
  - ST 65nm Bulk
  - ST 45nm Bulk
  - Vendor A 28nm Bulk
  - ST 28nm Bulk
  - ST 28nm FD-SOI

Source: GF, GTC2017
Source: Sugii, Low Power El. Appl. 2014
Source: P. Fiatresse, ST, ICICDT17
Source: ST, Shanghai FDSOI forum, 2015
FD-SOI ecosystem is getting stronger

- Research Technology & IP
  - CEA
  - LETI
  - STI
  - SAMSUNG
  - GLOBALFOUNDRIES

- Substrates
  - Soitec & Licensees

- Foundries & IDMs
  - SILICON FOUNDRIES
  - RENESAS
  - SAMSUNG
  - GLOBALFOUNDRIES
  - HLMC

- Tools & EDA
  - Keysight Technologies
  - Mentor Graphics

- IP & Design Services
  - Calchip
  - Surecore
  - Invectas
  - QUALCHIP
  - VeriSilicon
  - I-Micron
  - SILVACO
  - SYNAPSE Design
  - ARM
  - Open-Silicon
  - SFARDS
  - Analog Bits
  - Unify
  - Mentor Graphics
  - QuickLogic
  - Sigma Designs
  - Cadence

- Fabless & OEMs
  - NXP
  - SONY
  - Rambus
  - ARM
  - SiFive
  - Xilinx
  - AMICORE
  - ATTOPSEMI
  - Leader Silicon
  - X-FAB
  - LATTICE

- >100 customer engagements
FD-SOI for Automotive

Best power efficiency allowing simpler integration and enhanced reliability

FD-SOI - Reference technology for ADAS level 3 applications

Next generation e-Cockpit solution with full management of car infotainment
FD-SOI for Internet of Things

A game changer technology for better battery life

FD-SOI cuts standard GPS power consumption by 5 to 10 times

i.MX reference platform by NXP
FD-SOI: 3 steps adoption

Unique Features:
- Body Bias Compensation
- mmWave CMOS
- Radiation immunity

Platform Versatility: Energy Efficiency + Performance on Demand

Differentiation Options: RF, MRAM, ULP
Take-Aways

FDSOI is at the heart of every day life!

Power efficient & flexible technology with easy Analog/RF integration

Power, Performance not forgetting cost

Engineered substrate brings clear value to device

This is just the beginning...