A mixed-signal ic for managing power in 5G applications

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Introduction

• Architecture of mixed-signal ic’s in handsets
MODEM architecture

- Protocol stack (RTOS)
- Transceiver soup letter TDMA, OFDM, CDMA
OFDM subcarriers interference

Frequency

Time

Peak Power

Average Power

64 subcarriers per 20 MHz channel
(48 data subcarriers, 4 pilot subcarriers,
12 null subcarriers)
Power amplifier

- “Unreasonable” requirements on RF transistor
- Large Peak to Average Power ratio
- Hard to predict subcarrier interference
OFDM subcarriers interference

• Temptation to use math (from dsplog.com)

• PAPR is the maximum full scale signal power divided by the expected (average) power
  – PAPR of a single sine tone = 2
  – PAPR of a single complex sinusoidal tone = 1
  – Maximum expected PAPR from OFDM waveform with k subcarriers = k

• Important result
PAPR mitigation approaches

- Do nothing
- Allow for worst-case high peak power
- Drive signal saturation probability
Ideal high PAPR solution

PAPR Boost Event – Example 2

Power Supply
V_{max}

Threshold (Th)

Time

Fig. 10
Mixed-signal circuit to the rescue

• Many approaches to PAPR mitigation include “detectors”
• Power supply compliance has to be just 10%
• Lead us not into temptation...

Carrier frequency is GHz!
Open loop drive (Elastic Backoff™)
Charge-pump circuit (Dickson)

- Each stage boosted by switching voltage
- Simulation typically overestimates efficiency
  - 50% with integrated capacitors
  - > 80% with external capacitors
Actual charge-pump circuit
Charge-pump behavior
Load-line

- Charge-pump is able to supply any current at a fixed voltage (up to the load maximum)
- This is a “voltage” source
- Linear regulation with a switching behavior
Conclusions

• Complex analog/mixed-signal integration, but PV circuit blocks
• Saves 30% power consumption with easy to integrate components
• Semiconductor does not know if it’s analog or digital!!!