

Adding SALT™ to Product Lifecycle Management (PLM) for IP tracking and Silicon Configuration

Enabling Silicon-as-a-Service

Algodone at a Glance

When/Where

Founded in 2015

HQ in
Montpellier,
France

Founders

Jérôme Rampon

Gaël Paul

Professor
Lionel Torres

Vision

Enabling
Silicon-as-a-
Service

Technology

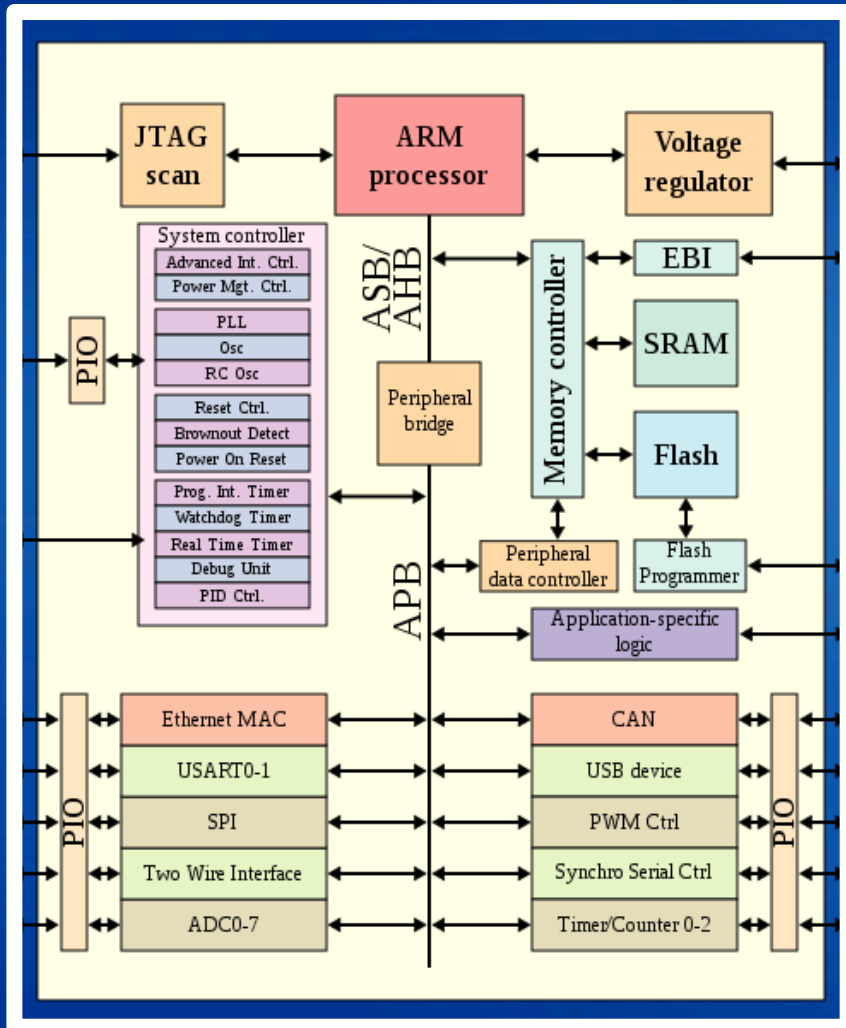
Silicon
Activation
Licensing
Technology
(SALT)TM

Algodone Silicon-as-a-Service Portfolio



Silicon Activation Licensing Technology (SALT™)

Today's Complex SoCs: Lots of Party IPs



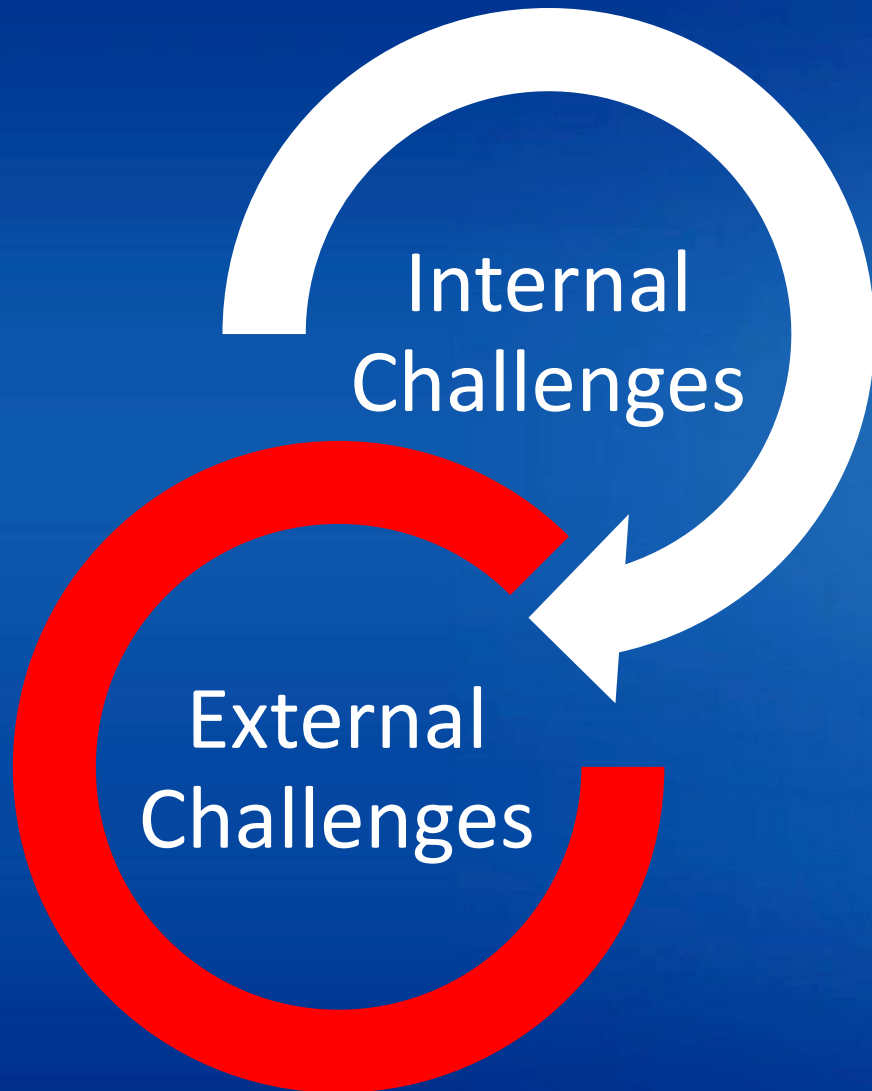
- Processor cores
- Memory blocks
 - ROM, RAM, flash
- Timing sources/clock generators
- Peripherals
- External interface for communication
 - USB, FireWire, Ethernet, USART, SPI, HDMI
- Analog interface
 - A-D/D-A converters
- Voltage regulators or power management circuits

Source: Wikipedia

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IP Management: Nightmare for Operations and Finance



- Internal challenges:
 - IP info scattered in different databases, in different formats, time consuming to correlate and prove accuracy
- External challenges:
 - Many IP vendors with different compliance requirements, hard to provide accurate royalty reporting, risk of costly audit

Intel Speaks of the Challenge of IP Tracking

The complexity of keeping track of IP versions and IP drops within the SOC execution schedule becomes a very hard and tedious problem to resolve... To determine this, it takes **several weeks and even months** of human glue effort to create a detailed list of all IP's in the SOC BOM.

*Mukund Pai, et al, Intel, Published
on Design & Reuse*

The Solution: Add SALT Trace to PLM



The goal: IP tracking throughout product life cycle so as to provide real time dashboards including:

- All SOC configuration deployed
 - In term of IP provider reference number, features, monetization
- Licenses fees aggregation based on license models defined in PLM with data volumes

High Performance Semiconductor

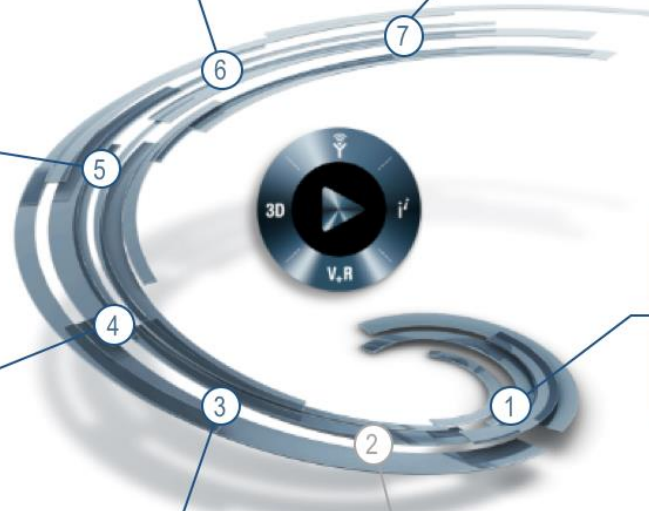
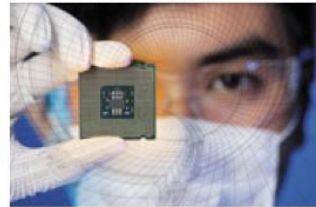
Achieve higher efficiency and zero re-spins in developing IOT-ready Systems-On-Chip

Semiconductor Packaging Performance



Functional Safety Delivery (ISO26262)

Semiconductor Verification & Validation



Semiconductor Materials Optimization

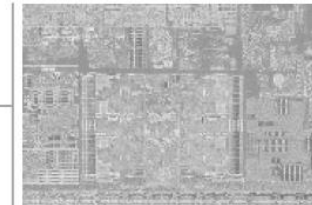
Mentor Graphics
cādence
SYNOPSYS
KEYSIGHT TECHNOLOGIES
Semiconductor Collaborative Design



Semiconductor IP Management



Semiconductor Architecture Design

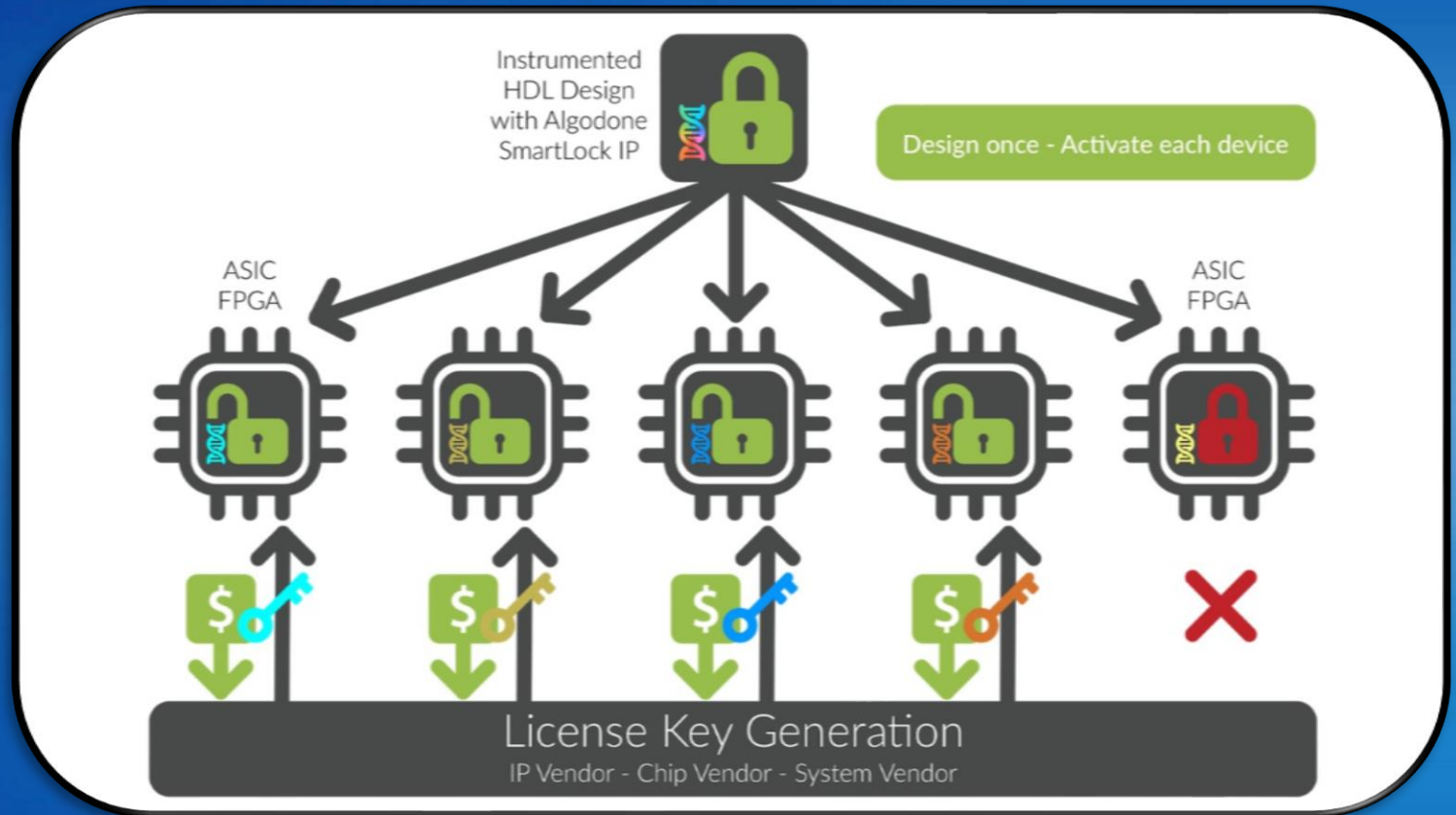




SALT Trace Feature: Silicon Licensing

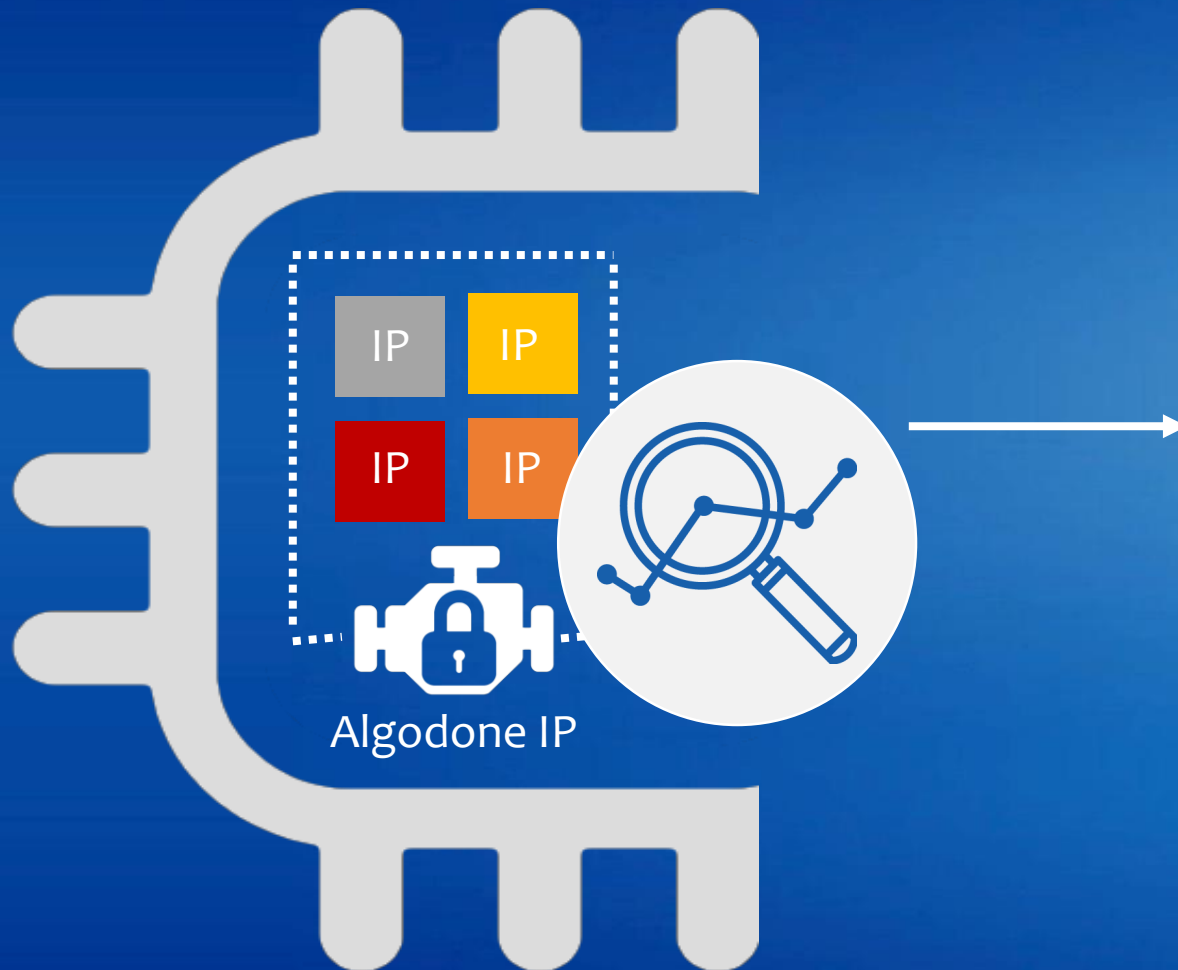
Unique Chip ID based
Silicon Licensing for
IP Activation & Configuration

Accurate and Verifiable





SALT Trace Feature: Secure Data Retrieval



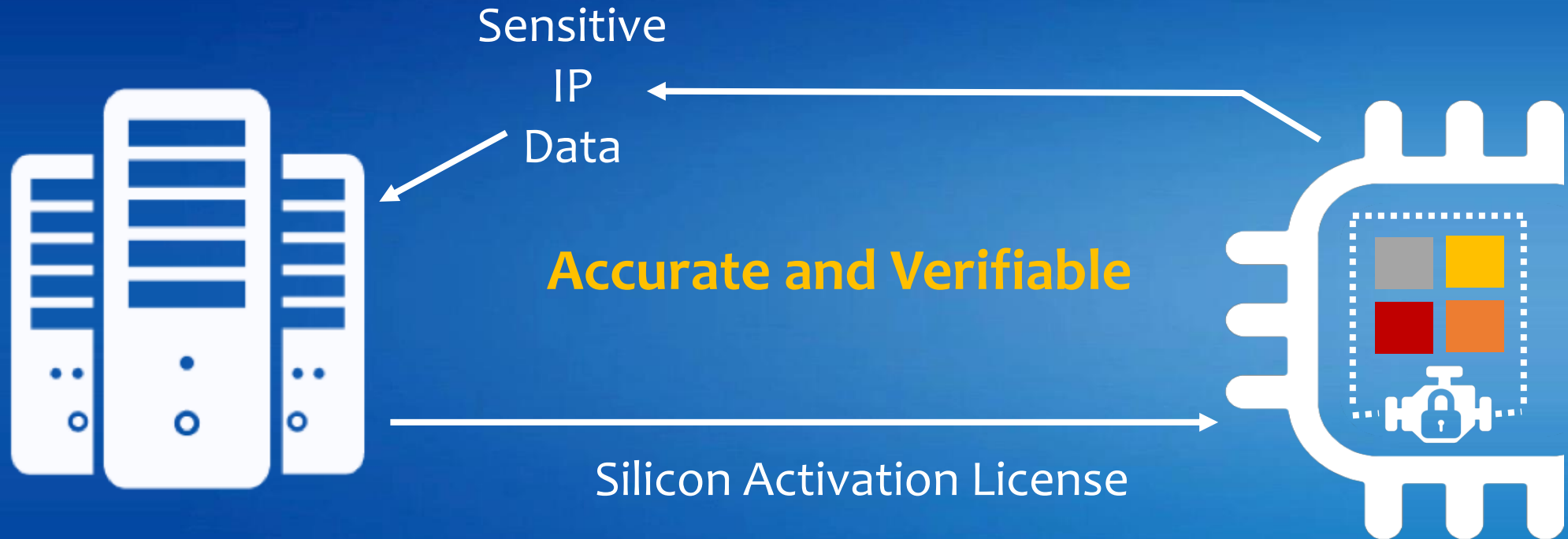
On-chip Secure Retrieval of Sensitive IP Info:

- Vendor
- Library
- Name
- Version
- Configuration

Accurate and Verifiable

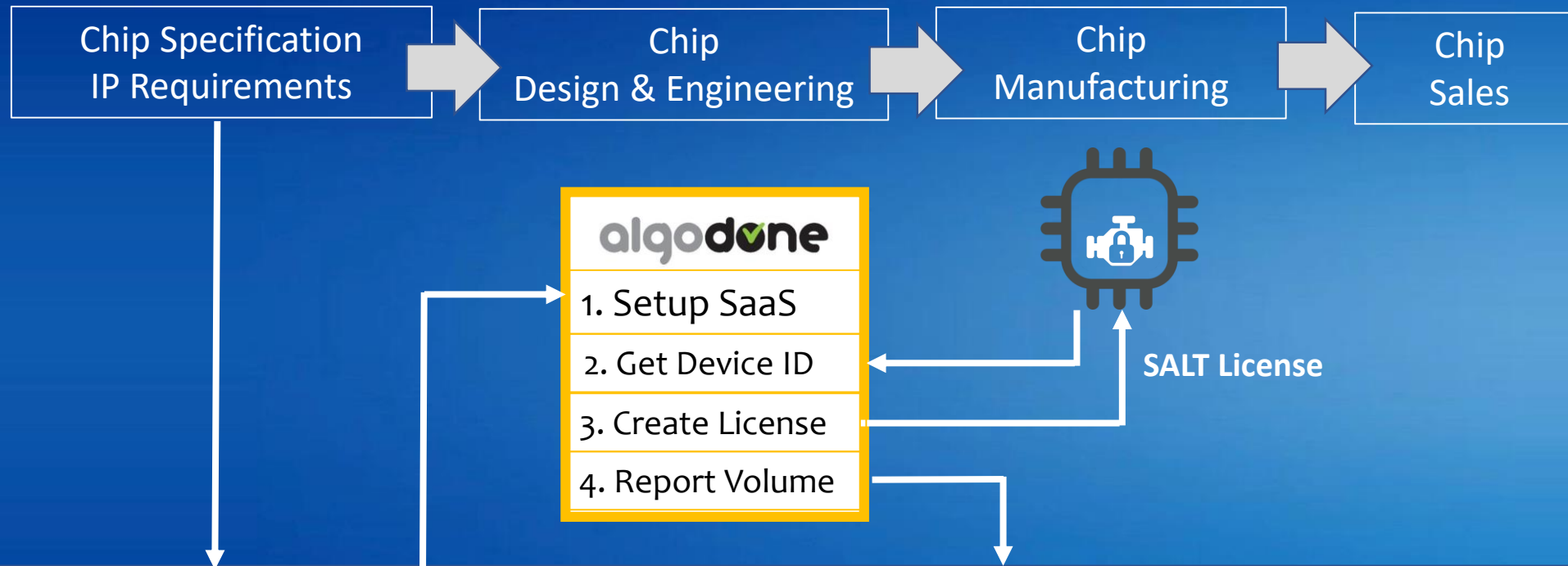


SALT Trace Feature: 3rd Party Transparency



Independent trusted 3rd Party Maintains Secure Storage and Communication

SALT Trace & DS 3D Interoperability Overview



3D Experience High Performance Semiconductor Platform –
Semiconductor IP Management

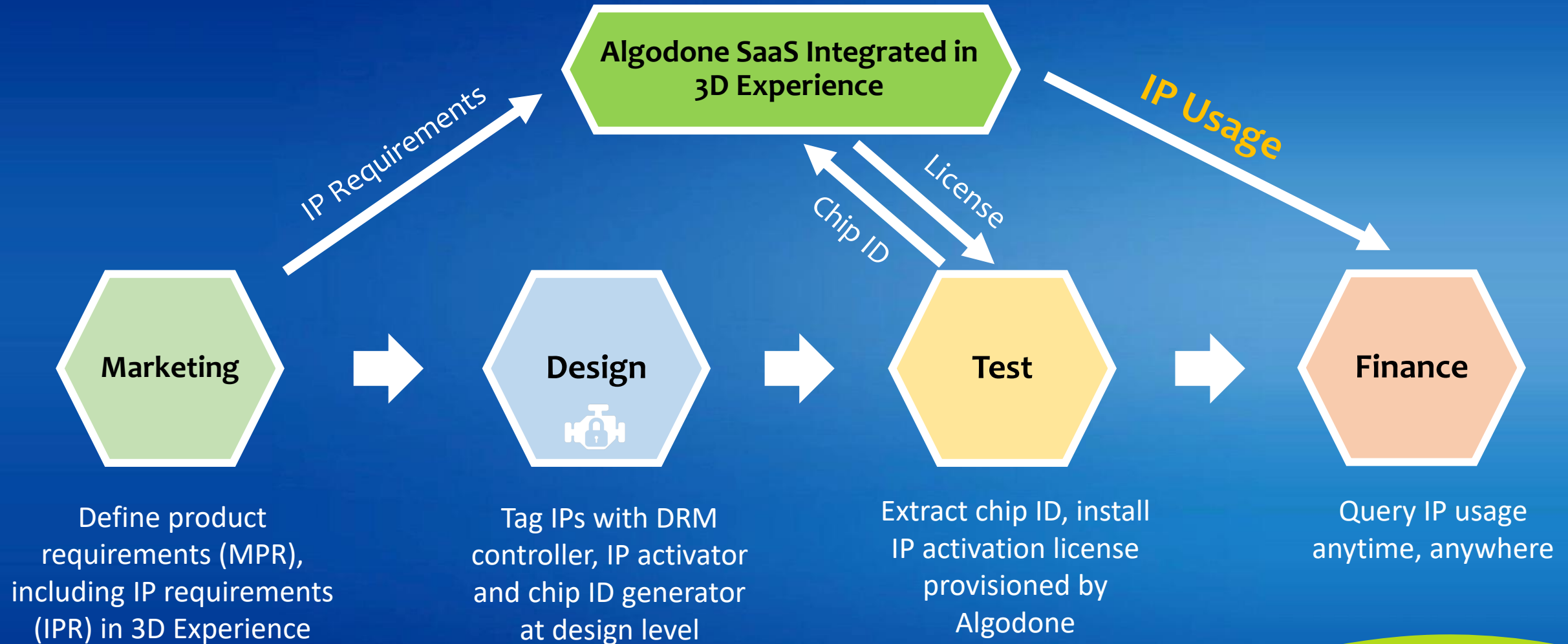
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Confidential

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SALT Trace: In a SoC Development Flow





Your Life with SALT Trace

- Accurate and verifiable IP information at your fingertip
 - Ease query based on a specific vendor, or IP or SoC

- **Realtime IP dashboard reported back in PLM tool (Volumes & licensing fees)**

Vendor View

Processor Core Vendor	
Core-A	12,974,630
Core-B	35,254,110
Core-C	89,124,210

IP View

Core-A	
High-Perf SoC	2,341,125
Low Power SoC	5,692,156

SoC View

SoC-1	
Core-A	2,341,125
USB IP	5,873,291
Memory IP	3,424,523

Accurate and Verifiable IP Usage at a Glance

SALT Trace: Benefit Summary

SALT Trace



Traceability
Verifiability

Easy adoption & deployment through PLM Integration

- Integrated with popular PLM platforms, SALT Trace offers easy adoption and push-button end-to-end IP management solution

Secure and tamper-proof sensitive data retrieval

- Secure communication of IP info and activation licensing through secure on-chip tag and in-cloud SaaS infrastructure

Traceable & verifiable IP info throughout product life cycle

- Tracking IP info from marketing requirements to chip production and sales by extracting accurate IP usage on chip non-intrusively and securely

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