DOLPHIN INTEGRATION

The Enabler of Low-Power Systems-on-Chip

Unlocking the full potential of Body Biasing with FD-SOI to design the most Energy Efficient SoC

FREDERIC RENOUX – IP SOC DAYS – DEC. 2018

CORPORATE ID

Since 1985

Serving more than 500 companies worldwide, incl. more than 80 companies in Asia

150 highly qualified engineers to enable the design of Energy Efficient SoCs

> 200 Silicon IPs available from 180 nm down to 22 nm in multiple foundries

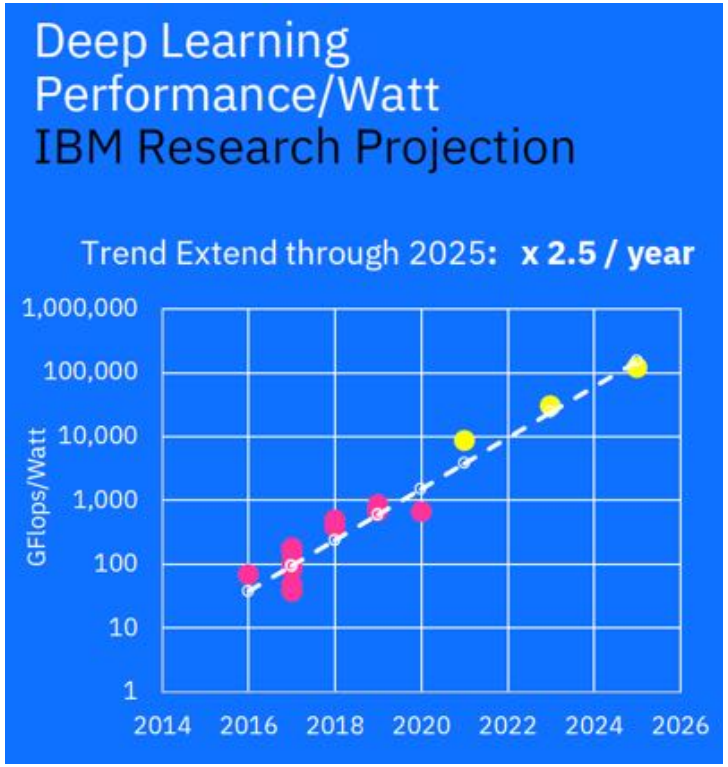
- Power Management
- Standard Cell libraries
- Memory Compilers
- Audio CODECs/ADCs/DACs and Triggers
- Oscillators

Renown for quality and support excellence

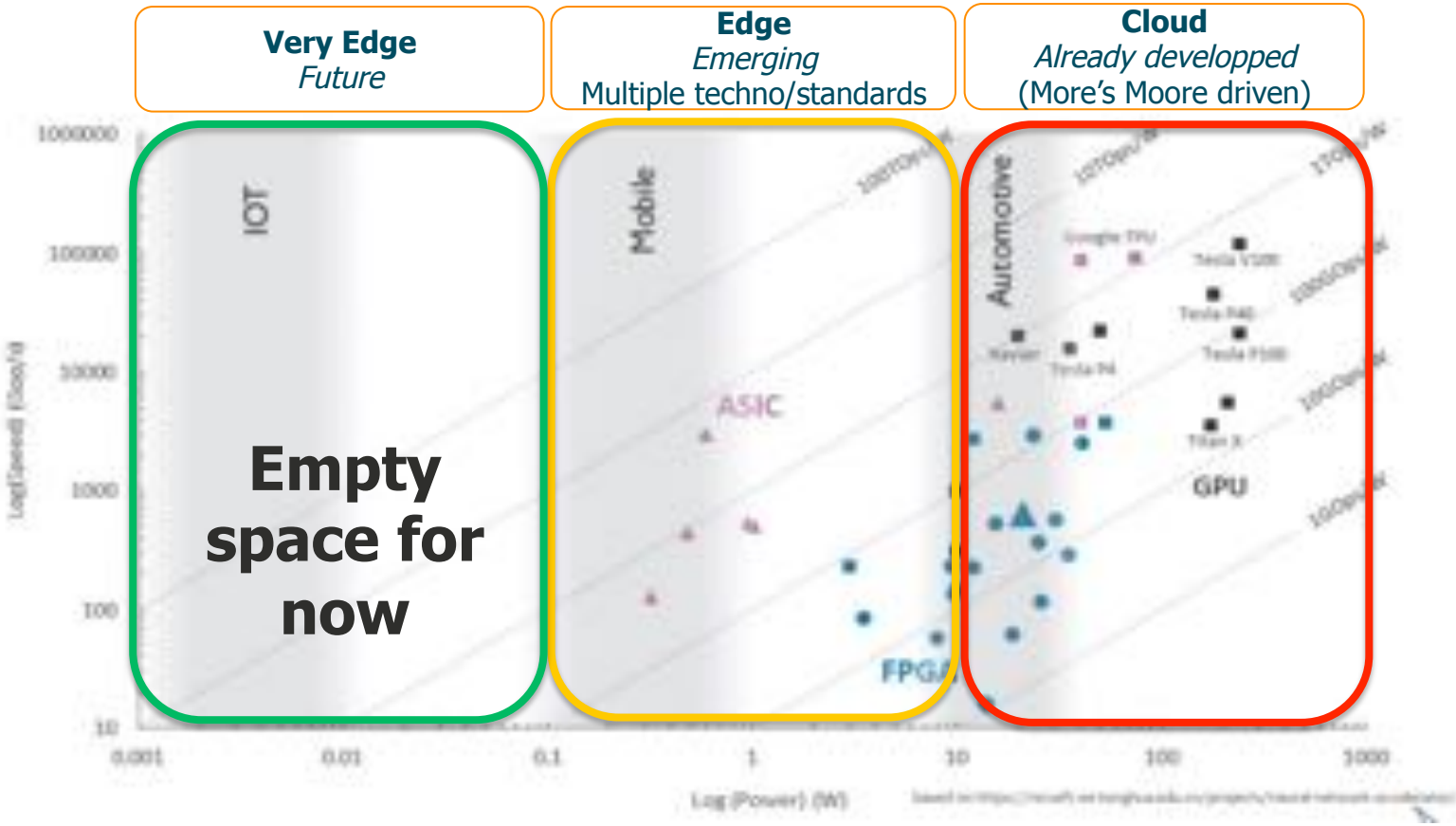
ENERGY-EFFICIENCY, THE NEW METRIC

- Performance is not anymore the only constraint
- Power consumption has to be in the equation

Mops/µW



Source: IBM, Semicon West 2018



Source: IMEC, ITF2018

A WORLD OF OPPORTUNITY, BUT

« There will be trillions of these IoT devices out there »

Jensen Huang, CEO of NVidia

« The speech and voice recognition market is expected to be valued at USD 6.19 Billion in 2017 and is likely to reach **USD 18.30 Billion by 2023**, at a **CAGR of 19.80%** between 2017 and 2023. »

Markets and Trends

« The IoT technology market is expected to grow from **USD 176.00 Billion in 2016 to USD 639.74 Billion by 2022**, at a CAGR of 25.1% during the forecast period. »

Markets and Trends

« One of today's technology **most significant challenges** is how to **create a SOC** that meets the conflicting consumer demand for devices with **both high performance and extended battery life** »

Samsung Semiconductor business

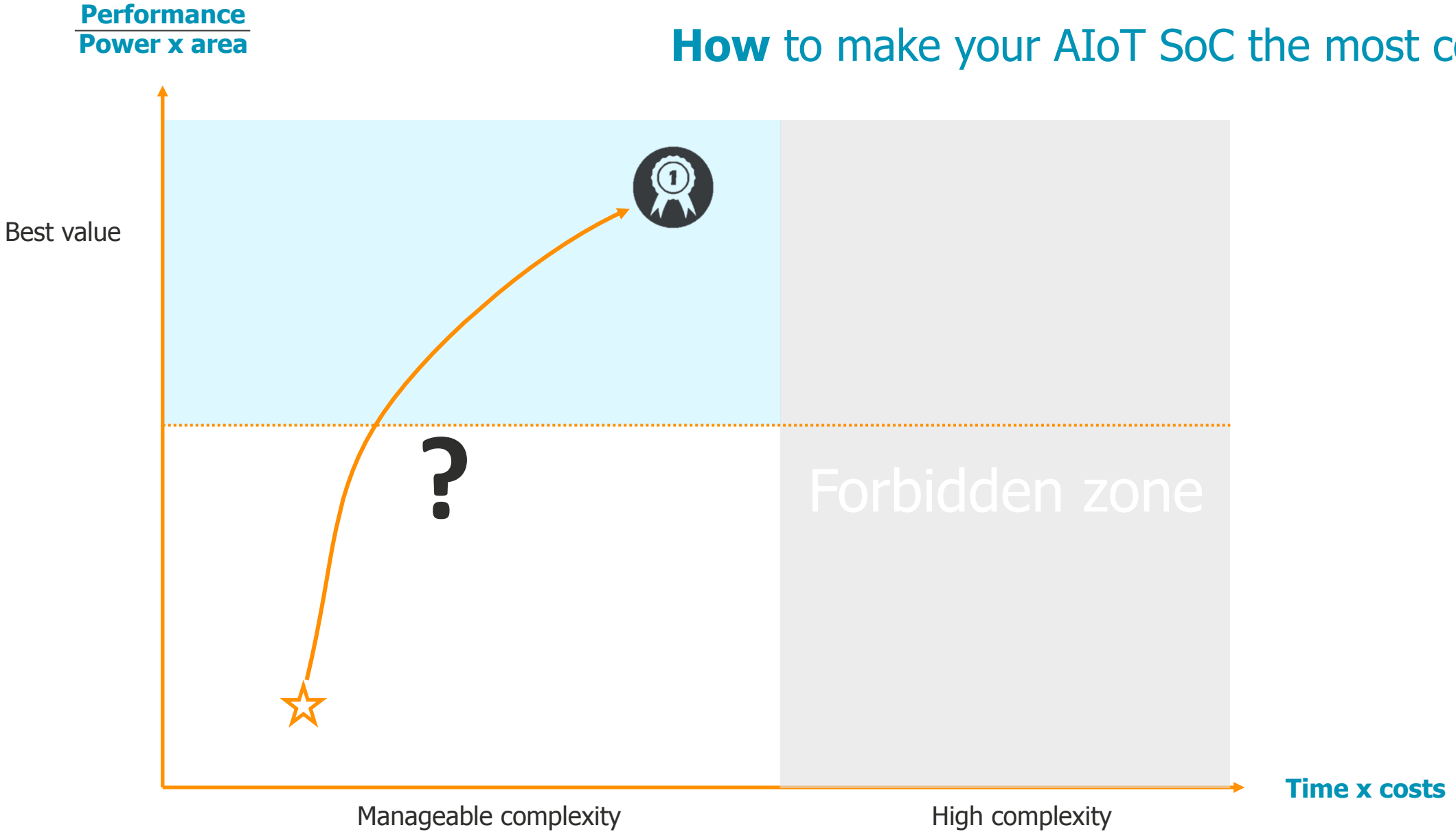
« …**Power management** is another feature, which in some cases may be the **determining factor** for whether a product (MCU) does well or fails because it affects battery life. Some of these MCUs have more than 16 low-power states, but to transition from one power state to the next is complex. »

Andrew Caples, Mentor a Siemens business

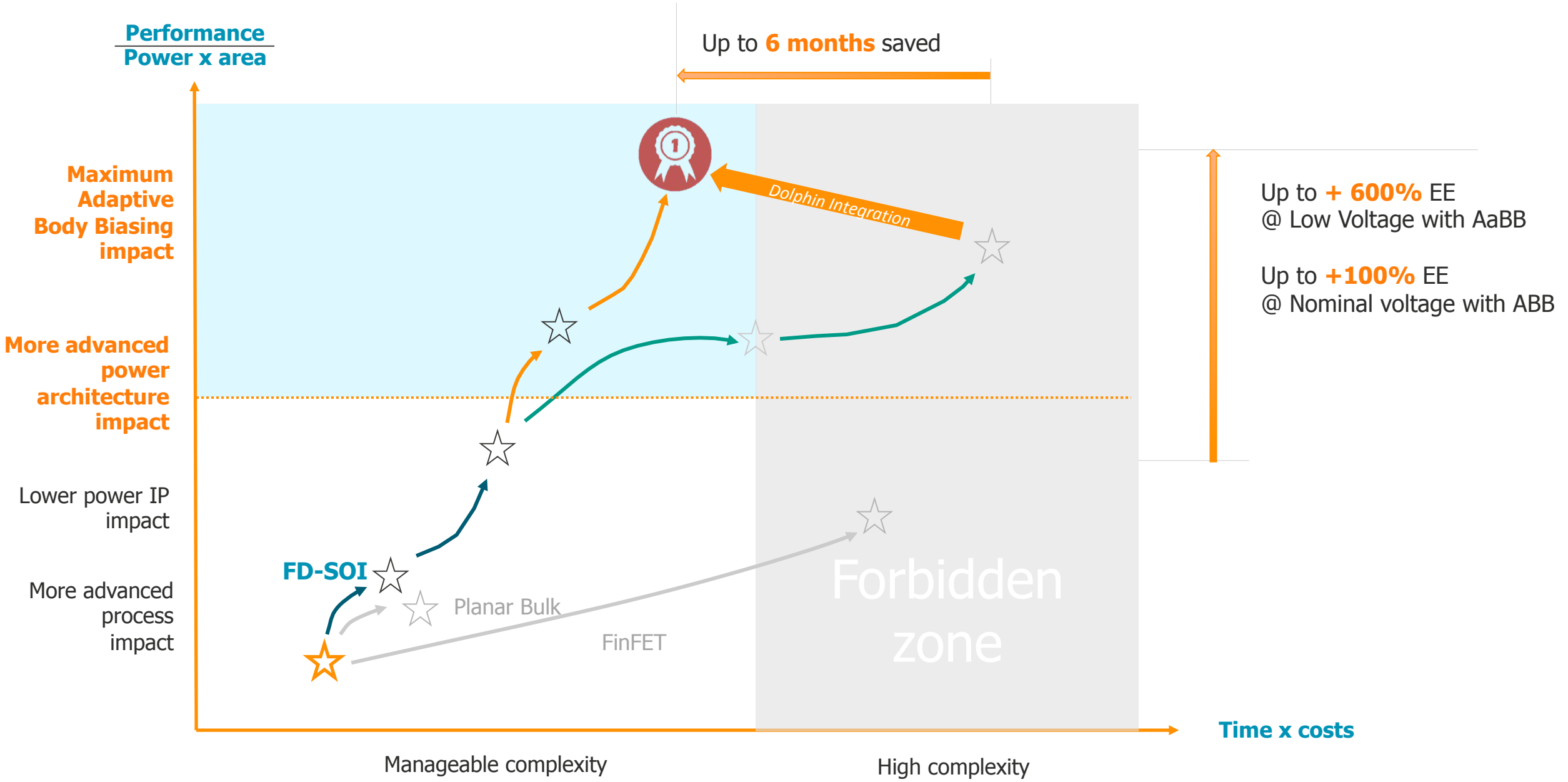
Design Technology Disconnect

THE CHALLENGE

How to make your AIoT SoC the most competitive?



FILLING THE "DESIGN TECHNOLOGY DISCONNECT" GAP



4 WAYS TO IMPLEMENT BODY BIASING

ABB
Boosting

- Wider dynamic operating range

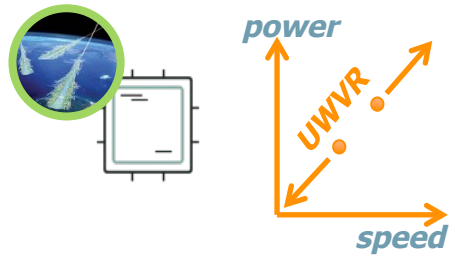


ABB
Static

- Reduced design corners
- Process compensation

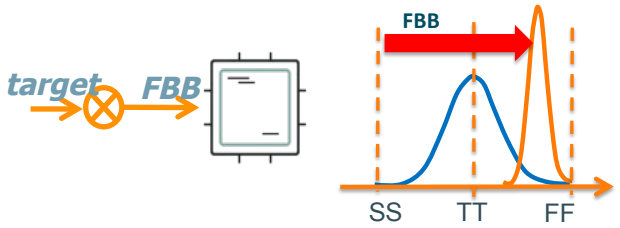
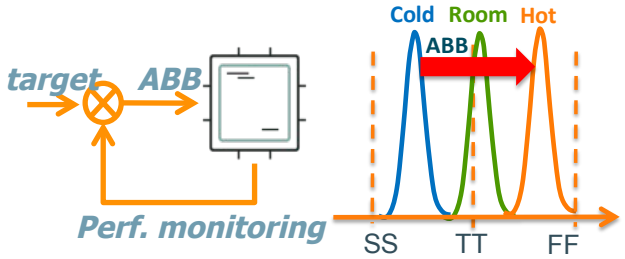


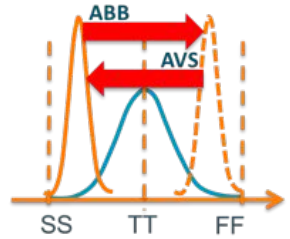
ABB
Dynamic

- Real time T. compensation
- Aging compensation



ABB/AVS
Hybrid

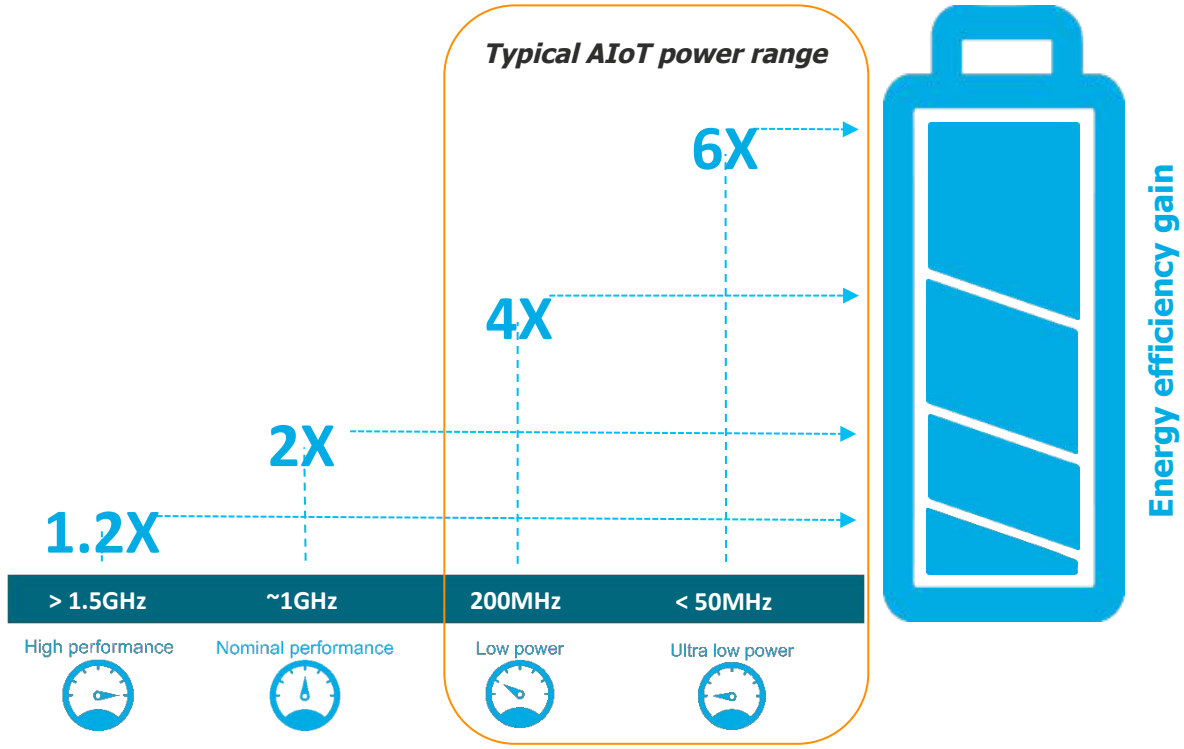
- Ultimate energy efficiency



FD-SOI OPPORTUNITY FOR BEST ENERGY EFFICIENCY

Leakage Optimized Power Modes

BODY BIASING CONTRIBUTION



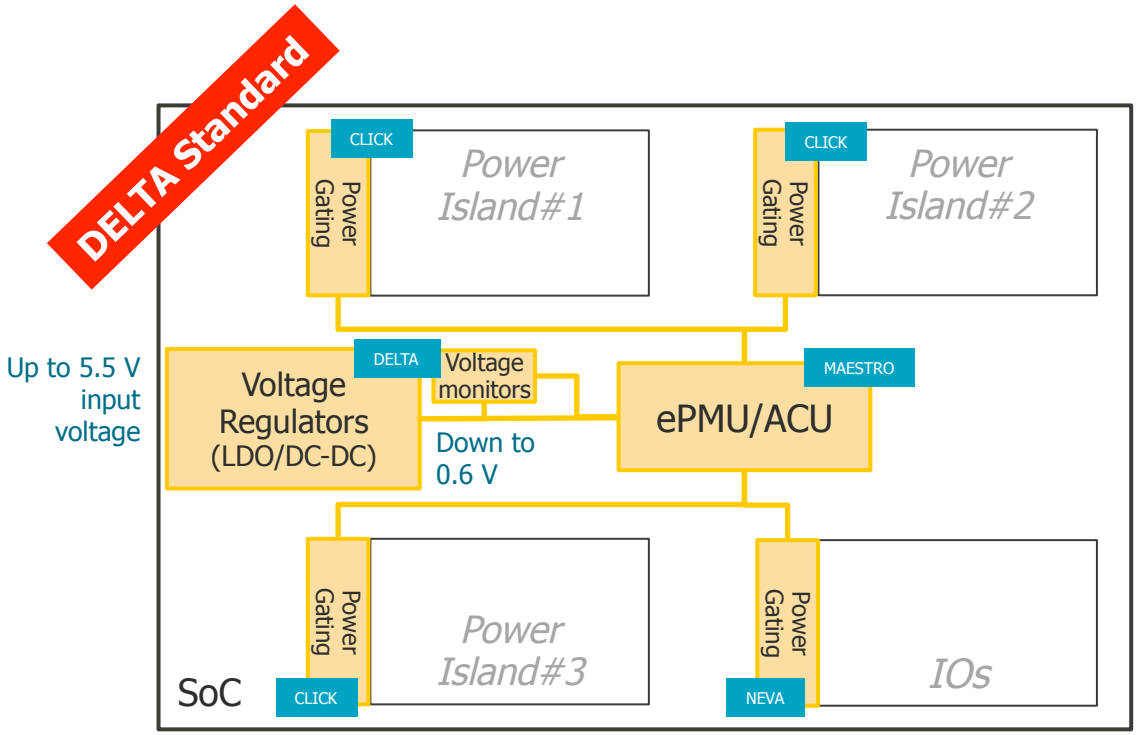
Body-bias impact (AVS, ABB) on energy efficiency

Source: Dolphin Integration, 2018

Process Variations Mitigation

FD-SOI PHASE #1 – since 2016

Power management IP platform
To design fast, safely and cost-effectively Energy Efficient SoCs



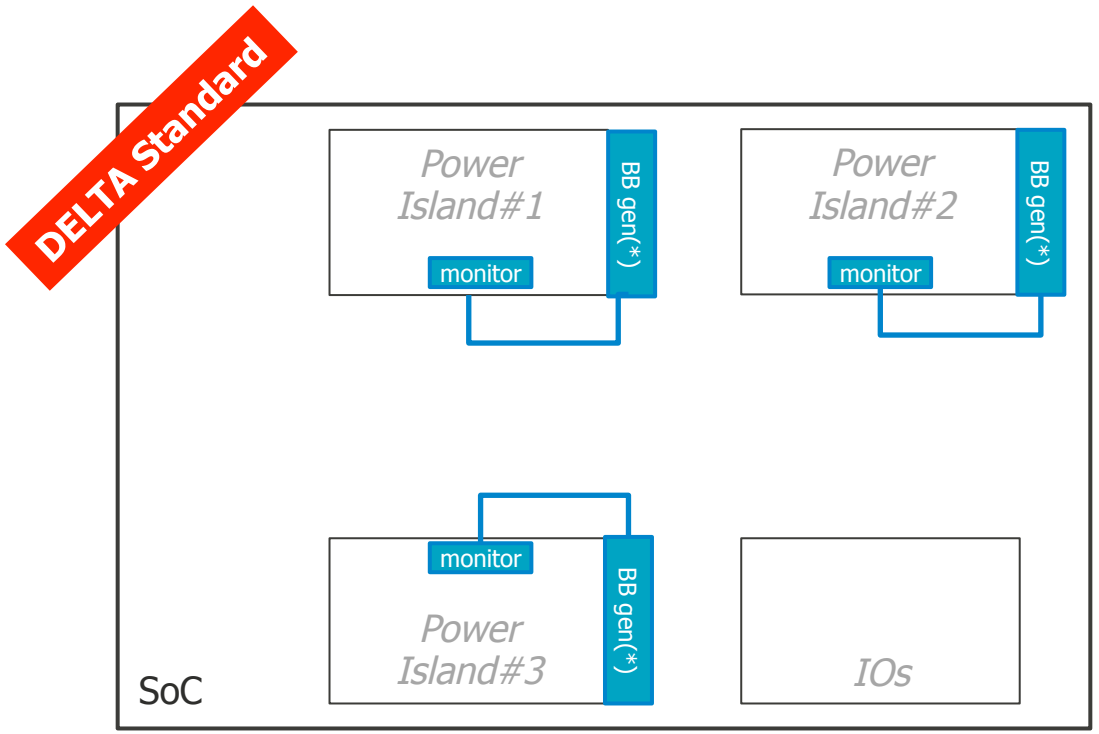
Key features

1. Modular and Configurable power management IPs (preventing risky customization)
2. Scalable to any SoC complexity and load current requirements (up to 128 power domains…)
3. DVFS, AVS, NTV, multi power domain… readiness
4. Open platform to third-party silicon IPs
5. Standardized IP interface for safe and fast SoC int.
6. Compliant with pure logic design flow
7. Best-in-class IP performances: EE, small area, low fabrication costs, Low BoM costs…
8. Built-in safety features to prevent SoC failures
9. Based on silicon proven IP architectures…

TO MAKE THE *HARD* BODY BIASING *EASY*

FD-SOI PHASE #2 – since 2018

Enablement of Adaptive Body Biasing as turnkey solution for best Energy Efficiency without risks

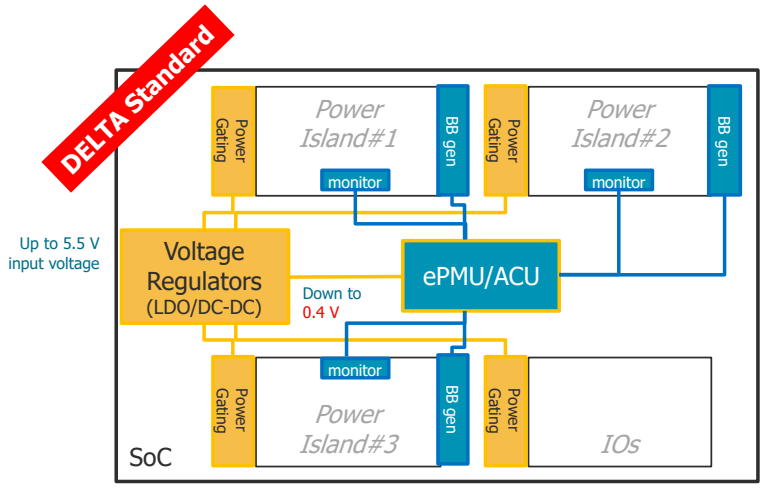


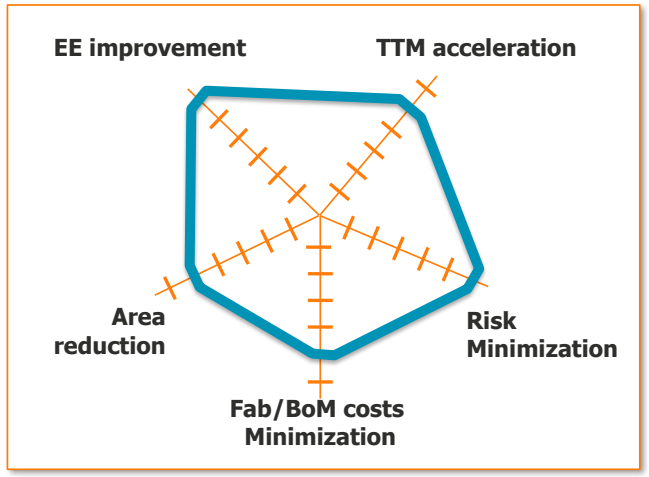
(*) includes light weight MAESTRO controller

Enhanced System Design Platform

+ Body Bias Generators
  - → Ultra low power (10 uA)…
+ Monitors
  - → High accuracy Monitors…
+ Fully integration
  - → Embedded regulation loop for process, temperature & aging compensation
  - → Workable with any standard-cell library & memory…
+ Design methodology & support

Total solution for best Energy Efficiency at minimal costs and without risks





LP design techniques

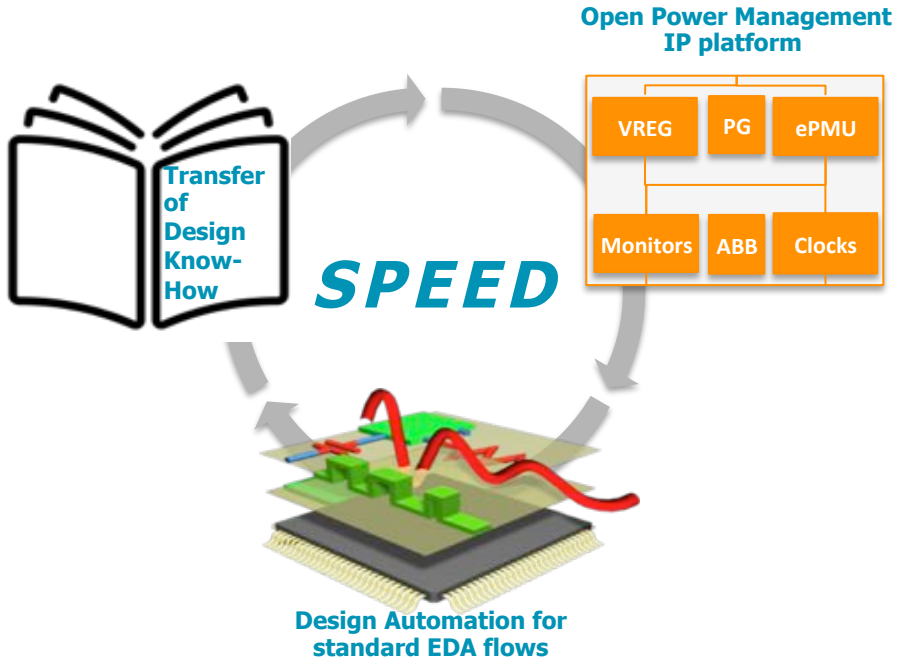
- NTV 0.9 - 0.6 V
- NTV 0.4 – 0.5 V
- ABB PVT sens.
- ABB Aging sensors
- AVS Workload detector

Supported
Soon
Roadmap

Advanced SoC power architectures

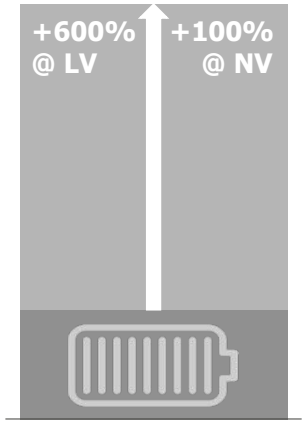
- Clock gating
- Global island power gating (VREG)
- Coarse grain island power gating (PMK-like)
- Advanced Coarse grain island power gating (CLICK)
- Coarse grain IO power gating (NEVA)
- Static voltage scaling (MDRV in sleep modes)
- Static voltage scaling (NV/LV/NTV in active modes)
- Dynamic voltage scaling (active modes)
- Dynamic voltage scaling fine grain (NV-NTV - active modes)
- Speed-up mode transition

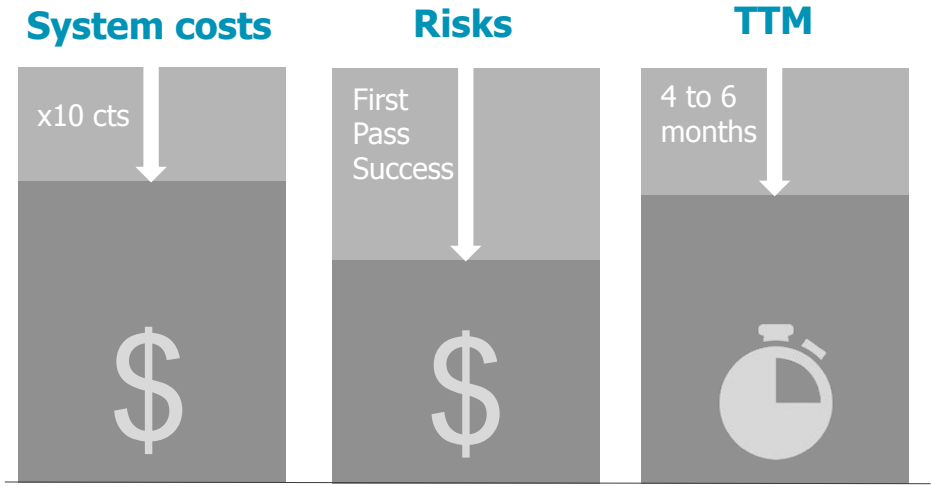
THE DOLPHIN INTEGRATION'S *SPEED* BREAKTHROUGH

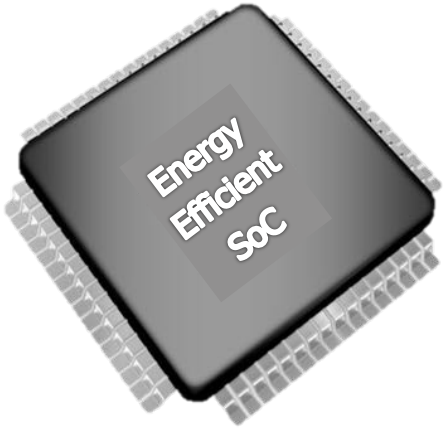


√ PD
√ DVFS
√ AVS
√ NTV
√ ABB…

Improved EE with







PD = Power Domain partitioning
DVFS = Dynamic Voltage Frequency Scaling
AVS = Automatic Voltage Scaling
NTV = Near Threshold Voltage
BB = Body Biasing

SUCCESS STORY ILLUSTRATION

GREENWAVES TECHNOLOGIES

CATALOG OF SILICON IPS FOR ENERGY-EFFICIENCY

Energy Efficiency System Design Platform

SUPPORT FROM SOC ARCHITECTURAL EXPERTS

Optimized Power Architecture

SOC DESIGN

Consistent and complete set of IP deliverables

SUPPORT FROM SOC INTEGRATION EXPERTS

Streamlined and secured integration

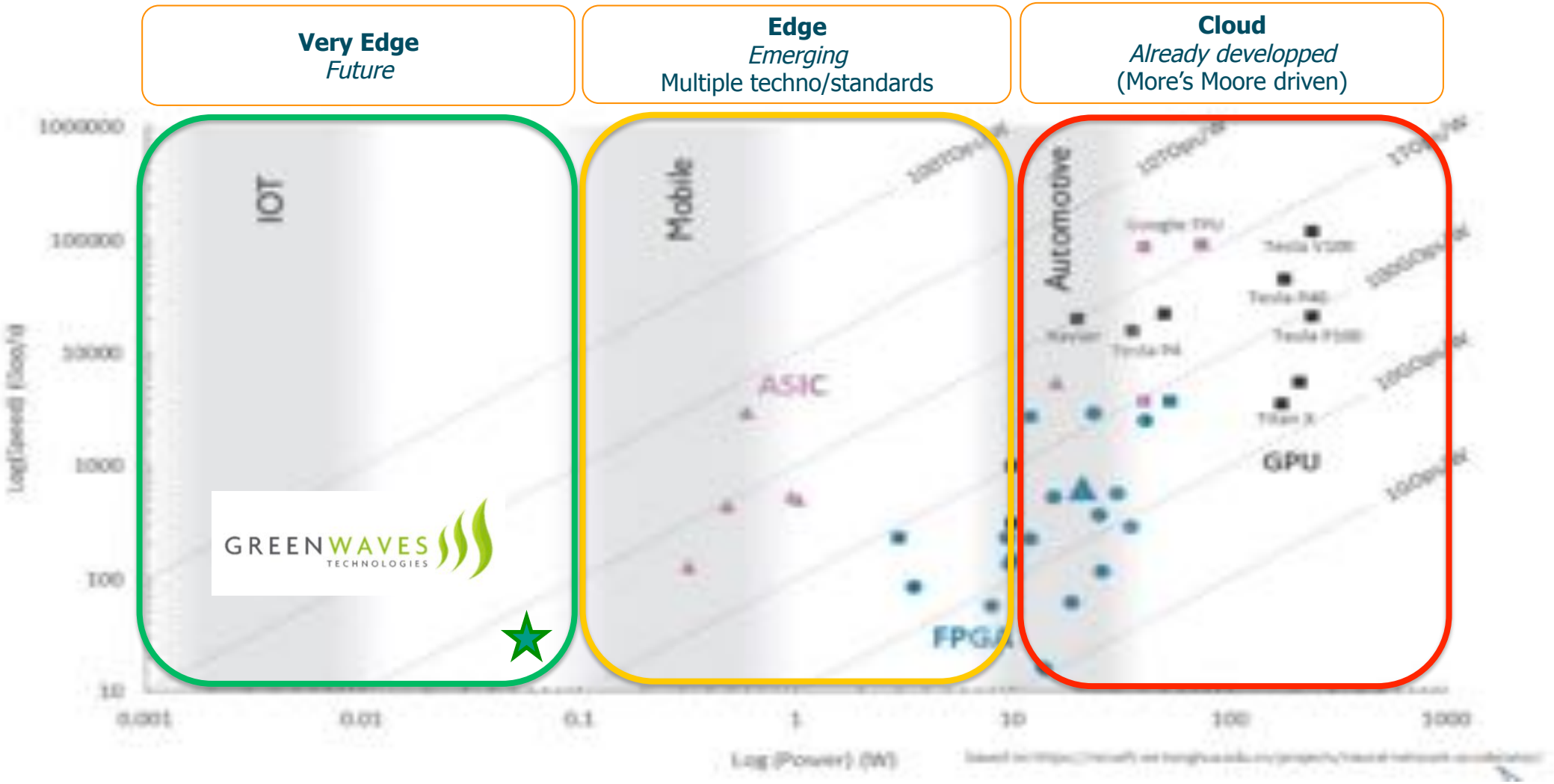
COOPERATIVE APPROACH FOR BEST PPA WITH FIRST TIME SILICON SUCCESS

Industry's lowest power **IoT application processor**, enabling groundbreaking Artificial Intelligence at the very edge (55 nm)

- ✓ **200 MOPS at 3 mW**
- ✓ Minimum **2 µA** standby current
- ✓ Energy efficiency : **15 GOPS for 70 mW**
- ✓ 2 DVFS domains
- ✓ Fast switching (**from us to sub ms**) between 6 operating modes
- ✓ Designed in less than **18** months
- ✓ **First Time Silicon Success**

Read or listen the insights of Eric Flamand – Greenwaves' CTO – on Dolphin Integration's power management offering
www.dolphin-integration.com

ENERGY-EFFICIENCY, THE NEW METRIC



Source: IMEC, ITF2018

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