Unlocking the full potential of Body Biasing with FD-SOI to design the most Energy Efficient SoC

Frederic Renoux – IP SoC days – Dec. 2018
Since 1985

150 highly qualified engineers to enable the design of Energy Efficient SoCs

Renown for quality and support excellence

Serving more than 500 companies worldwide, incl. more than 80 companies in Asia

> 200 Silicon IPs available from 180 nm down to 22 nm in multiple foundries

- Power Management
- Standard Cell libraries
- Memory Compilers
- Audio CODECs/ADCs/DACs and Triggers
- Oscillators
• Performance is not anymore the only constraint
• Power consumption has to be in the equation

Source: IBM, Semicon West 2018

Source: IMEC, ITF2018
« There will be trillions of these IoT devices out there »

Jensen Huang, CEO of NVidia

« The speech and voice recognition market is expected to be valued at USD 6.19 Billion in 2017 and is likely to reach USD 18.30 Billion by 2023, at a CAGR of 19.80% between 2017 and 2023. »

Markets and Trends

« The IoT technology market is expected to grow from USD 176.00 Billion in 2016 to USD 639.74 Billion by 2022, at a CAGR of 25.1% during the forecast period. »

Markets and Trends

« One of today’s technology most significant challenges is how to create a SOC that meets the conflicting consumer demand for devices with both high performance and extended battery life »

Samsung Semiconductor business

« ...Power management is another feature, which in some cases may be the determining factor for whether a product (MCU) does well or fails because it affects battery life. Some of these MCUs have more than 16 low-power states, but to transition from one power state to the next is complex. »

Andrew Caples, Mentor a Siemens business
How to make your AIoT SoC the most competitive?
Filling the "Design Technology Disconnect" Gap

- Maximum Adaptive Body Biasing impact
- More advanced power architecture impact
- Lower power IP impact
- More advanced process impact

- Performance: Power x area
- Time x costs

- Manageable complexity
- High complexity

- Up to 6 months saved

- Up to +600% EE @ Low Voltage with AaBB
- Up to +100% EE @ Nominal voltage with ABB

FD-SOI

Planar Bulk

FinFET

Forbidden zone

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4 Ways to Implement Body Biasing

- **ABB Boosting**
  - Wider dynamic operating range

- **ABB Static**
  - Reduced design corners
  - Process compensation

- **ABB Dynamic**
  - Real time T. compensation
  - Aging compensation

- **ABB/AVS Hybrid**
  - Ultimate energy efficiency
Leakage Optimized Power Modes

Body-bias impact (AVS, ABB) on energy efficiency

Source: Dolphin Integration, 2018
**FD-SOI PHASE #1 – since 2016**

Power management IP platform  
To design fast, safely and cost-effectively Energy Efficient SoCs

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**Key features**

1. Modular and Configurable power management IPs (preventing risky customization)
2. Scalable to any SoC complexity and load current requirements (up to 128 power domains...)
3. DVFS, AVS, NTV, multi power domain... readiness
4. Open platform to third-party silicon IPs
5. Standardized IP interface for safe and fast SoC int.
6. Compliant with pure logic design flow
7. Best-in-class IP performances: EE, small area, low fabrication costs, Low BoM costs...
8. Built-in safety features to prevent SoC failures
9. Based on silicon proven IP architectures...
FD-SOI PHASE #2 – since 2018

Enablement of Adaptive Body Biasing as turnkey solution for best Energy Efficiency without risks

Enhanced System Design Platform

- Body Bias Generators
  - Ultra low power (10 μA)...

- Monitors
  - High accuracy Monitors...

- Fully integration
  - Embedded regulation loop for process, temperature & aging compensation
  - Workable with any standard-cell library & memory...

- Design methodology & support

(*) includes light weight MAESTRO controller
Total solution for best Energy Efficiency at minimal costs and without risks

LP design techniques
- NTV: 0.9 - 0.6 V
- NTV: 0.4 - 0.5 V
- ABB PVT sens.
- ABB Aging sensors
- AVS Workload detector

Advanced SoC power architectures
- Clock gating
- Global island power gating (VREG)
- Coarse grain island power gating (PMK-like)
- Advanced Coarse grain island power gating (CLICK)
- Static voltage scaling (MDRV in sleep modes)
- Static voltage scaling (NV/LV/NTV in active modes)
- Dynamic voltage scaling (active modes)
- Dynamic voltage scaling fine grain (NV-NTV - active modes)
- Speed-up mode transition

Supported
- Soon
- Roadmap

EE improvement
- TTM acceleration
- Area reduction
- Risk Minimization
- Fab/BoM costs Minimization

DELTA Standard
- Power Island#1
- Power Island#2
- Power Island#3
- IOs

Voltage Regulators (LDO/DC-DC)
- ePMU/ACU
- Monitor

SoC
- Up to 5.5 V input voltage
- Down to 0.6 V
- Down to 0.4 V
THE DOLPHIN INTEGRATION’S **SPEED** BREAKTHROUGH

**Improved EE with**

- √ PD
- √ DVFS
- √ AVS
- √ NTV
- √ ABB...

**Energy Efficiency**

- +600% @ LV
- +100% @ NV

**System costs**

- $x10 cts

**Risks**

- First Pass Success

**TTM**

- 4 to 6 months

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PD = Power Domain partitioning
DVFS = Dynamic Voltage Frequency Scaling
AVS = Automatic Voltage Scaling
NTV = Near Threshold Voltage
BB = Body Biasing
Success Story Illustration

Catalog of Silicon IPs for Energy-Efficiency

- Energy Efficiency
- System Design
- Platform

SoC Design

- Consistent and complete set of IP deliverables

Support from SoC Integration Experts

- Optimized Power Architecture
- Streamlined and secured integration

Cooperative Approach for Best PPA with First Time Silicon Success

Industry’s lowest power IoT application processor, enabling groundbreaking Artificial Intelligence at the very edge (55 nm)

- 200 MOPS at 3 mW
- Minimum 2 µA standby current
- Energy efficiency: 15 GOPS for 70 mW
- 2 DVFS domains
- Fast switching (from us to sub ms) between 6 operating modes
- Designed in less than 18 months
- First Time Silicon Success

Read or listen the insights of Eric Flamand – Greenwaves’ CTO – on Dolphin Integration’s power management offering www.dolphin-integration.com
ENERGY-EFFICIENCY, THE NEW METRIC

- **Very Edge**
  - Future

- **Edge**
  - Emerging
  - Multiple techno/standards

- **Cloud**
  - Already developed
  - (More’s Moore driven)

Source: IMEC, ITF2018