FD-SOI: how material & design innovations enable new market opportunities

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Digital Electronics BU - Product Marketing Manager

IP-SoC 2018, December the 5th 2018, Grenoble

Introduction to Soitec

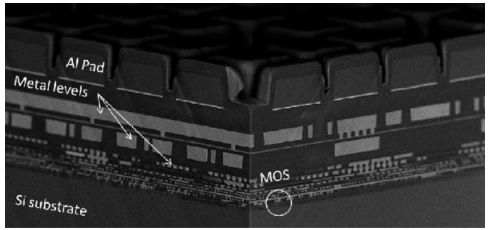
> We design and deliver innovative substrates and solutions to enable our customers' products shaping everyday life

- **Number 1 –** Largest manufacturer of engineered substrates
- **Global presence –** 1,100 employees worldwide
- **Serving 4 high-volume markets –** Smartphones, automotive, cloud & infrastructure, IoT
- **Multi-site industrial footprint –** France, Singapore, China
- **Industry standard –** RF-SOI is in 100% of smartphones

Choosing the right base for your product

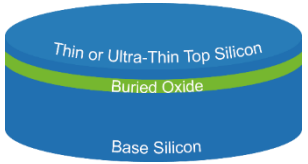
Pinot Noir, Burgundy, Cabernet Sauvignon…

End Product



Soil Properties

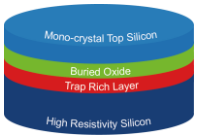
Substrate



Soitec's full range of engineered substrates across multiple segments and applications

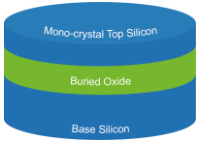
RF Front-End Module

RF-SOI
For high efficient mobile communication



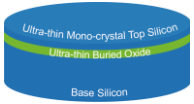
Power

Power-SOI
For seamless high voltage device isolation



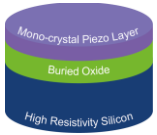
Processor & connectivity SoC

FD-SOI
For power-efficient & flexible digital computing with easy analog/RF integration



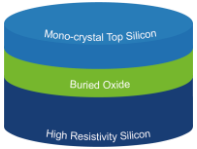
Piezo on insulator

POI
New engineered substrates for filters



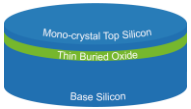
Photonics

Photonics-SOI
To integrate high performance photonics devices into silicon



Imagers

Imager-SOI
For improved imager performance in NIR



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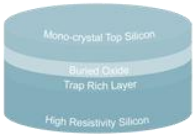
RF Front-End Module

RF-SOI
For high efficient mobile communication



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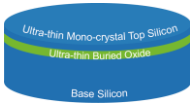

Piezo on insulator

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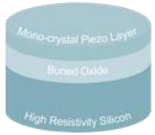

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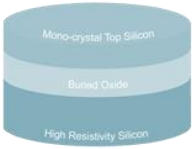


Imagers

Imager-SOI
For improved imager performance in NIR

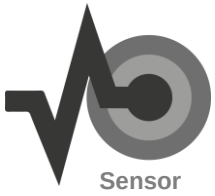
AI is about transforming data into meaningful information

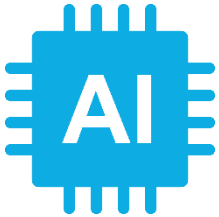
f (data) = information

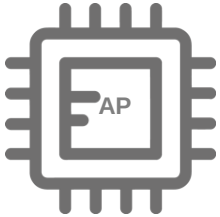
Picture f () = « apple »

Motion f () = « maintenance needed »

Sound f () = « Hello! »

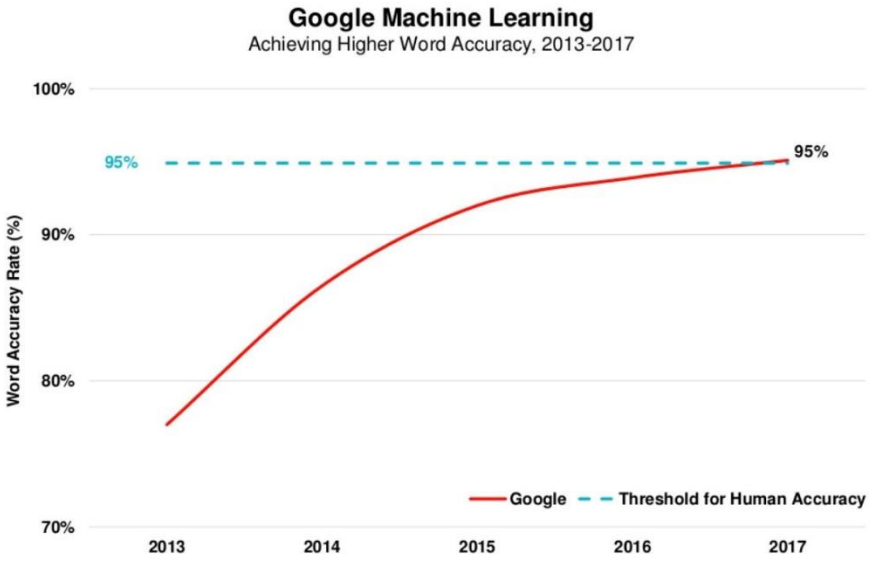






Collect Analyze Act

AI is increasingly sophisticated



Source: Mary Meeker's annual Internet Trends Report

AI inference is moving to the edge

Low-power solutions are required

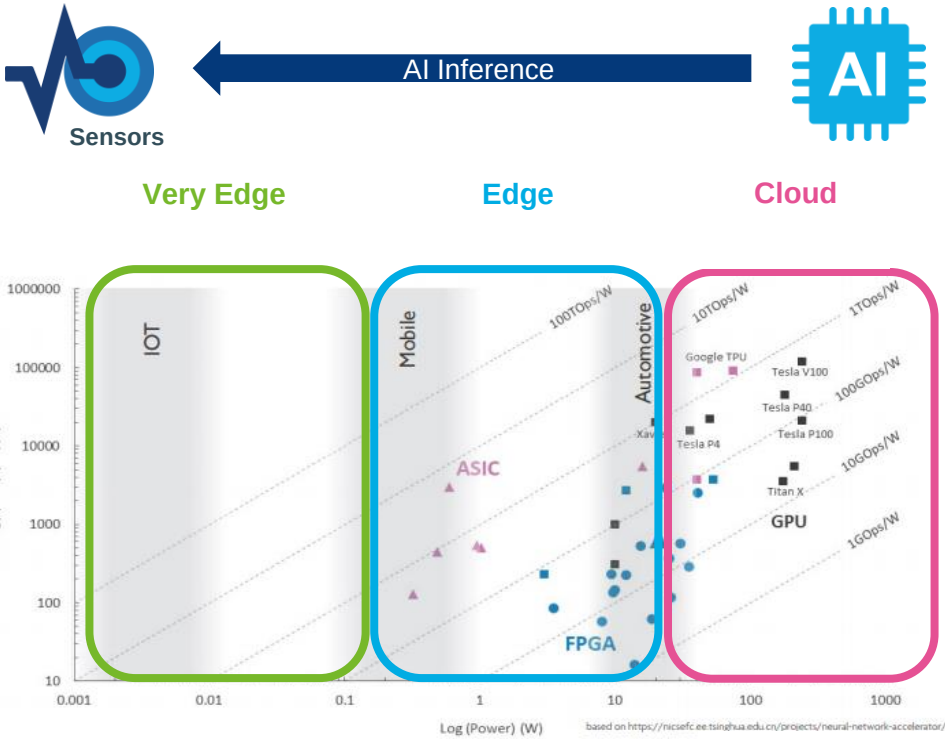
4 drivers pushing AI at the edge

Latency / reliability

Data privacy

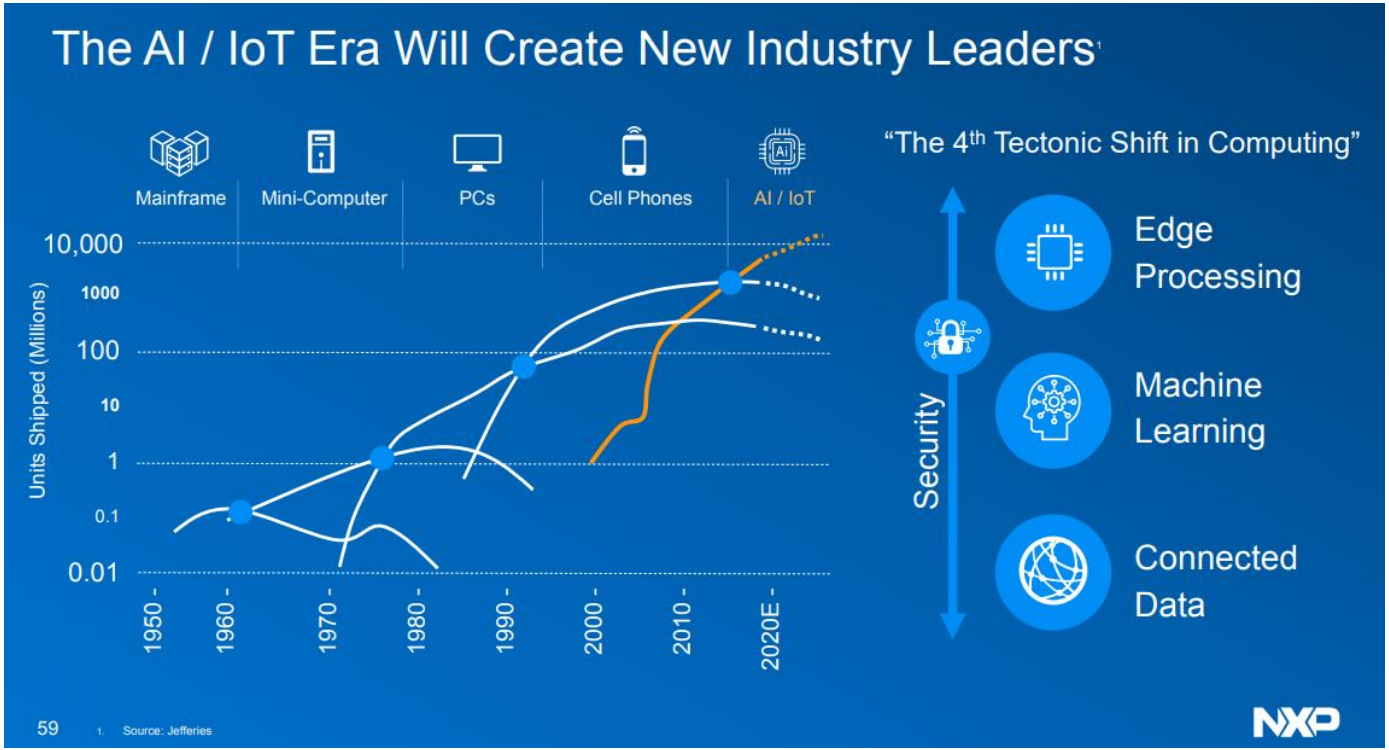
Power consumption

Cost



Source: IMEC, ITF2018

AIoT (AI + IoT) sparks a new semiconductor revolution



Source: NXP Investor Day 2018

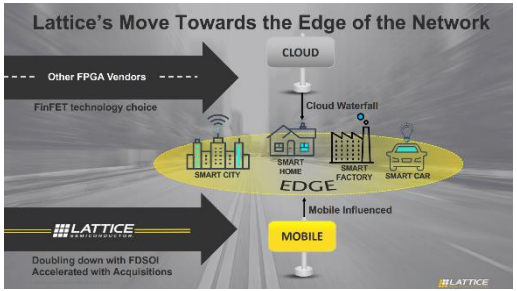
FD-SOI – powering the AIoT revolution

i.MX RT600 crossover processors unlocking the potential of machine learning and artificial intelligence at the edge, are based on FD-SOI

Powering the next generation of voice-assisted end nodes

i.MX RT600 Family of Crossover Processors

Next generation always-on FPGA low power machine learning inferencing (from 1mW to 1W) based on FD-SOI



> "Designers need silicon that allows them to build compact high-performance AI devices that deliver excellent performance without violating footprint or thermal management constraints. Cost is also a crucial factor."

Source: Lattice white paper, May 2018

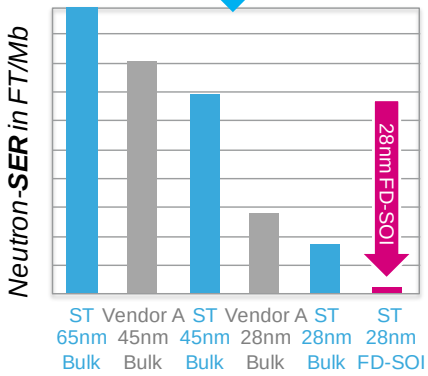
Next generation Human Machine Interfaces powered by AI ambient computing based on FD-SOI

> "The intelligence has to move to the edge [..].Our vision requires a few things [..]. 22FDX has that mix of performance and power and the ability to aggregate functions such as RF or non-volatile memory that we are looking towards. We need also extremely low power so the ability to do active body biasing is very important to us."

Source: Synaptics CEO, GTC, September 2018

FD-SOI unique features

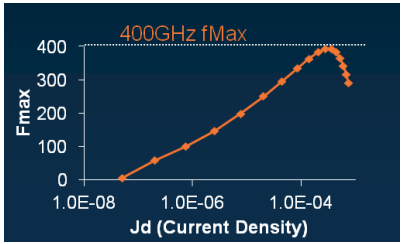
Reliability



Source: ST, Shanghai FDSOI forum, 2015

20x Soft Error Rate improvement vs. bulk

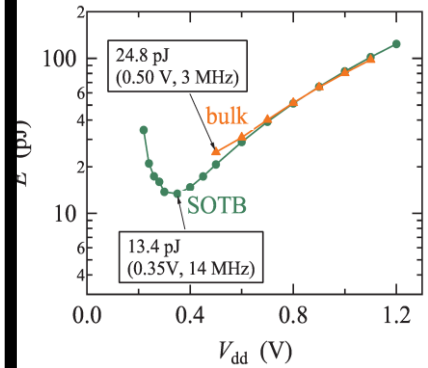
mmWave RF-CMOS



Source: GF, GTC2017

Best CMOS mmWave with similar performance to SiGe radios

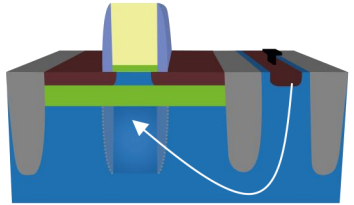
Ultra Low Voltage



Source: Sugii ,Low Power El. Appl. 2014

Operation at minimum energy point (<0.4V)

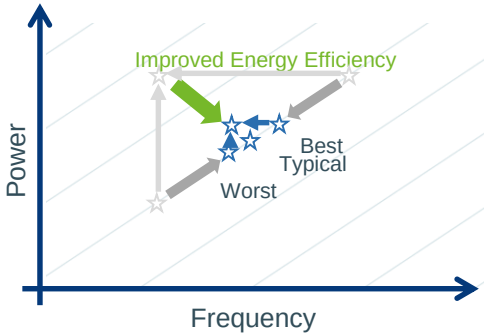
Body Bias



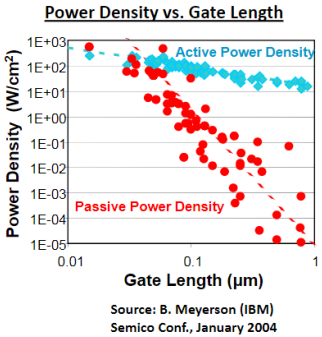
Up to 7X energy efficiency gains at ULV

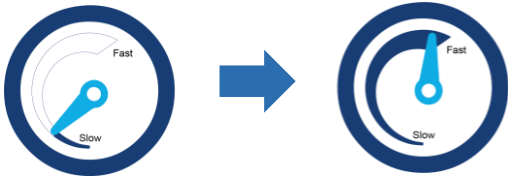
Energy efficiency needs dynamic power/ leakage optimization techniques

Ultra Low Power Energy Efficiency



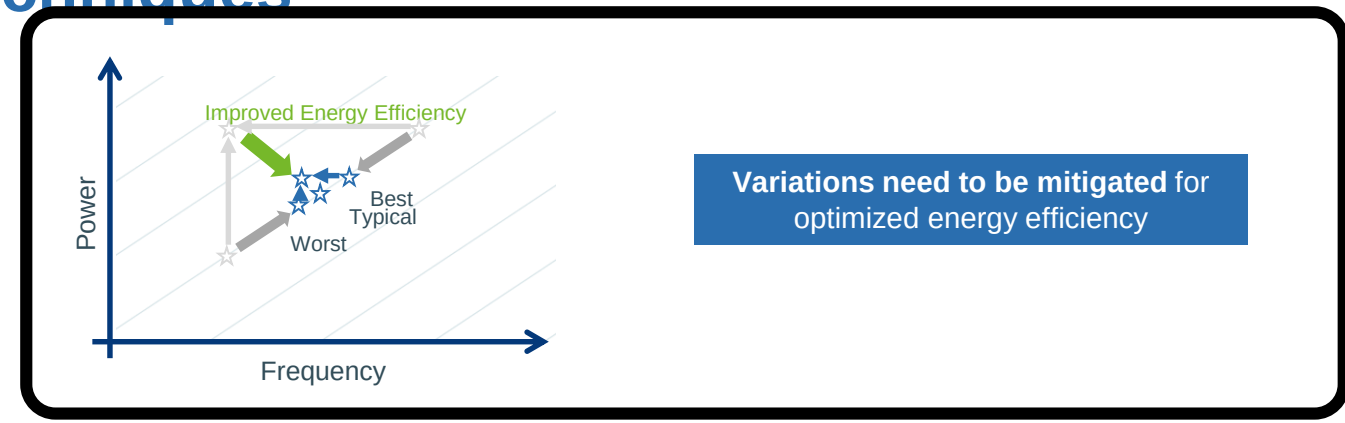
Variations need to be mitigated for optimized energy efficiency





Dynamic Power/ Leakage needs to be optimized **real time**

Energy efficiency needs dynamic power/ leakage optimization techniques



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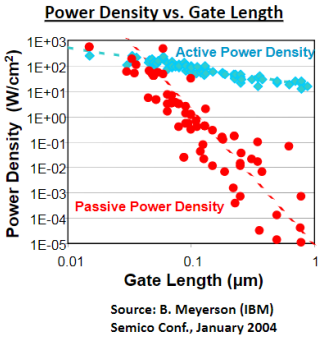
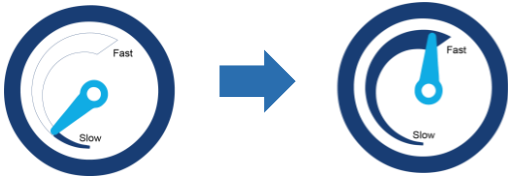
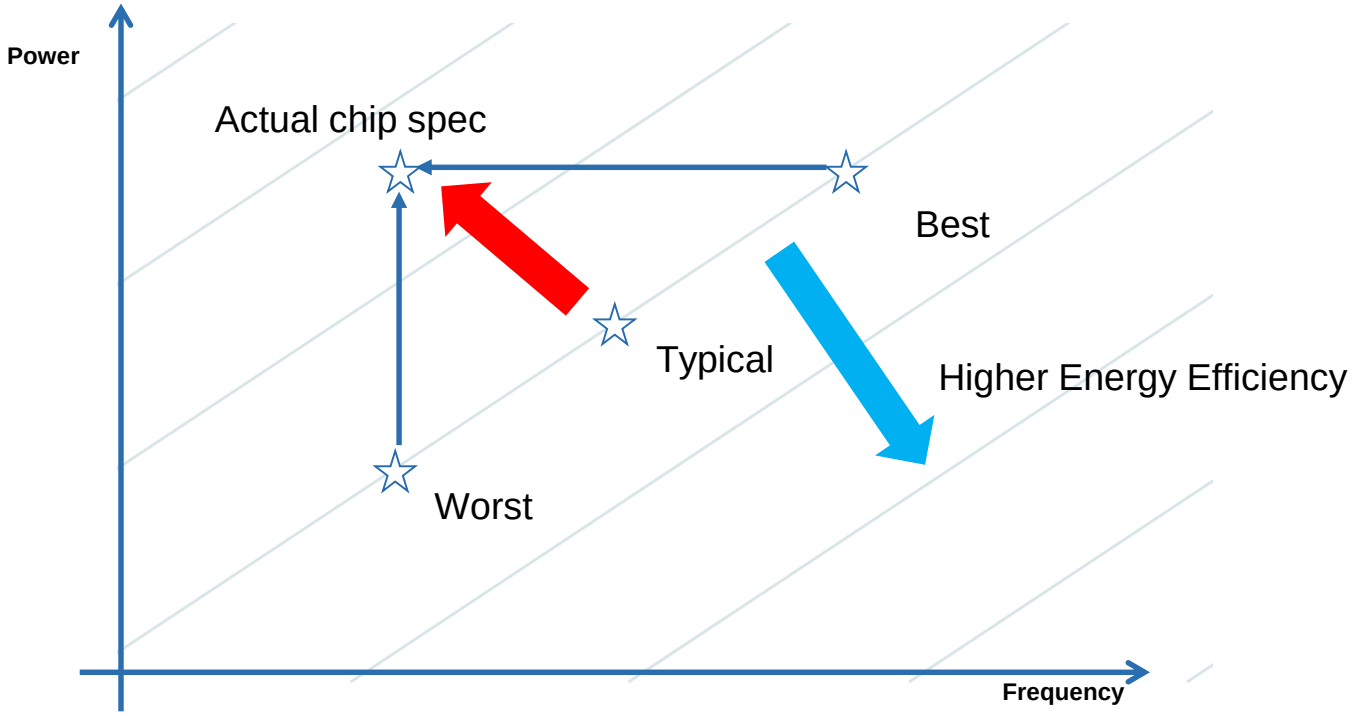




Dynamic Power/ Leakage needs to be optimized **real time**

Variations impact energy efficiency



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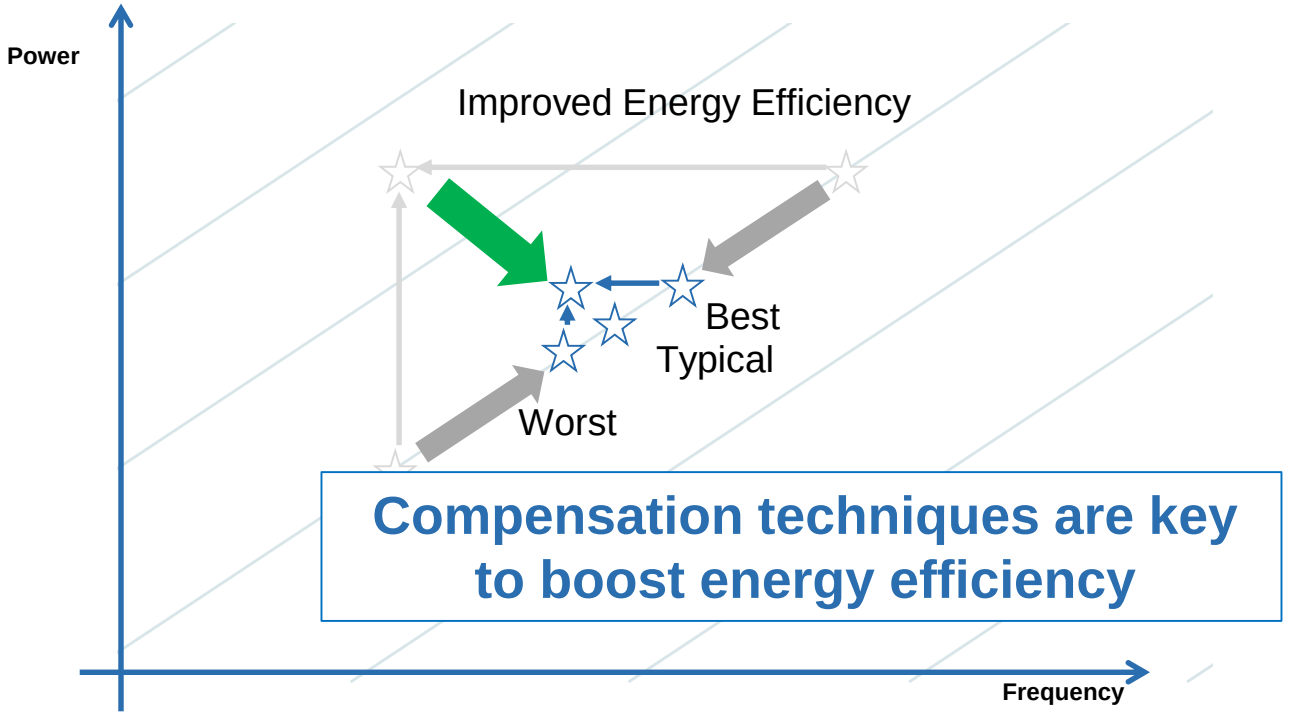
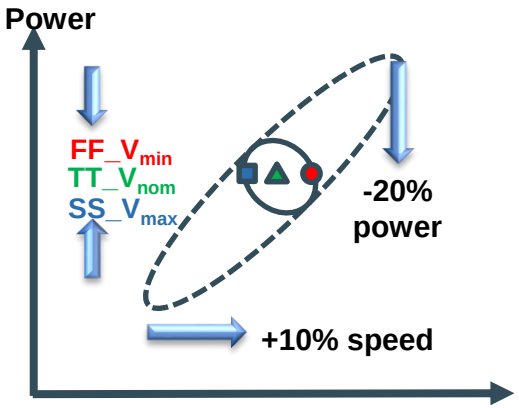


Compensation techniques are key to boost energy efficiency

Static AVS is commonly used in advanced technology nodes but faces severe drawbacks

- Performance and power towards TT corner



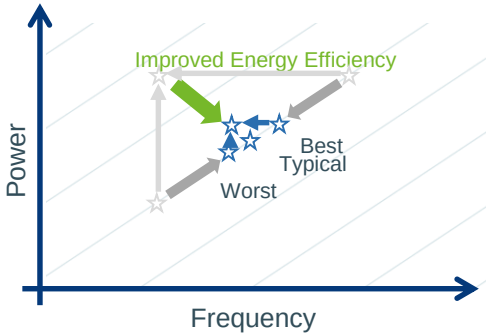
Process	Voltage	Vfloor	Speed	Power	Aging
Slow	High	High	Typical	Typical	High
Typical	Typical	Typical	Typical	Typical	Typical
Fast	Low	Low	Typical	Typical	Low

ST, ITC 2017 – Mhira and Huard, Best Paper award

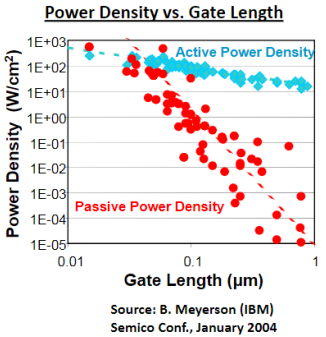
- Aging is degraded
- Vfloor is increased (less room for overdrive)
- Temperature compensation is very difficult (too sensitive). Vdd not the right lever.
- More complex voltage regulators required

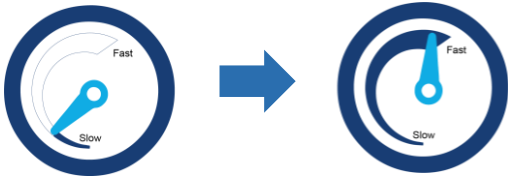
Energy efficiency needs dynamic power/ leakage optimization techniques

Ultra Low Power Energy Efficiency



Variations need to be mitigated for optimized energy efficiency



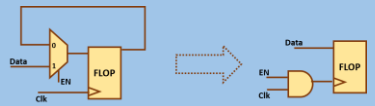


Dynamic Power/ Leakage needs to be optimized **real time**

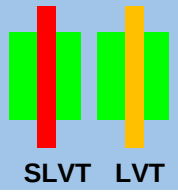
Low Power design techniques principles

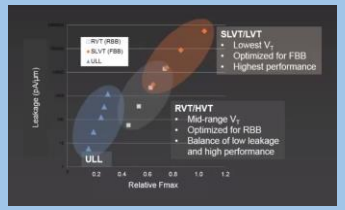
Clock Gating

- Avoid systematic toggling of Flipflops CLK pins
- Put logic in ClockTree to reduce active power



Multi-Vth libs

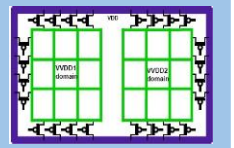




Source: GF seminar

Power Gating

- Define multi-Vdd domains
  - High Vdd only on-demand
  - Low Vdd for low performance
- Switch off unused domains

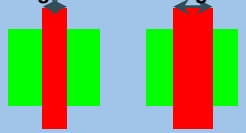


Dynamic Power : $\sim W.V_{dd}^2 .F$

Leakage Power : $\sim (V_{dd}/L).e^{-Vth/S}$

Speed : $\sim W/L\ (V_{dd}-V_{th})^2$

Multi gate lengths



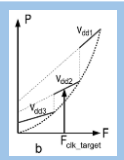
ST, S3S 2017

L_{gate}	PB	28FD
Lmin	PB0	1
+4nm	PB4	x4
+10nm	PB10	x10
+16nm	PB16	x30

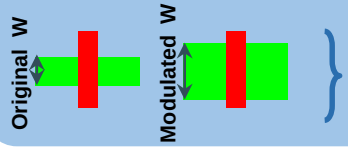
Leakage reduction

DVFS

- Dynamic Voltage Frequency Scaling
- Benefit from V^2 power savings



Multi drive libs

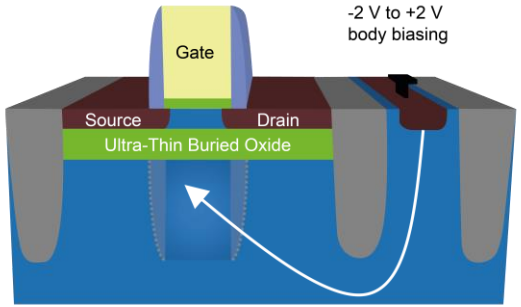


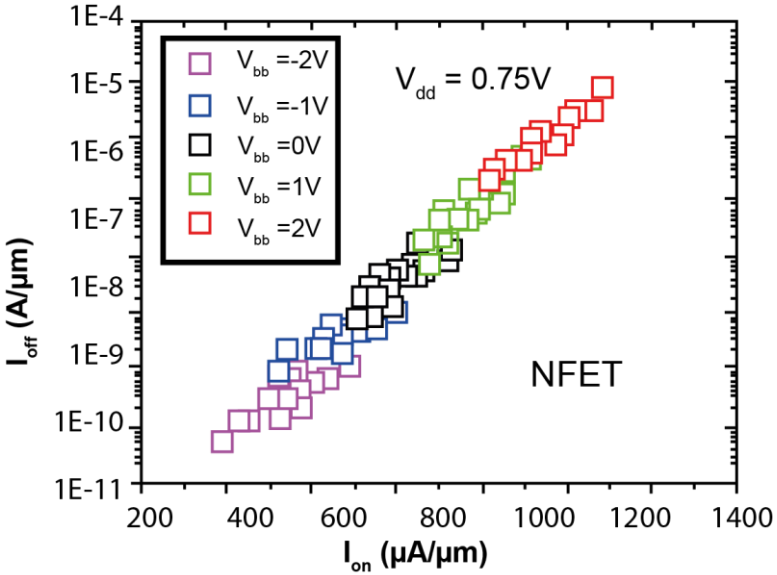
Dynamic and Leakage reduction

Landscape of low power techniques

		BULK (Vdd only)	
Source	**Parameter**	**Static Optimization**	**Dynamic Optimization**
Dynamic Power	W	Multi-drive lib ✓	-
	Vdd	Multi-Vdd lib ✓	DVS ✓
	Vdd/Vth	Multi-Vdd/Vth lib ✓	✗
	F	Clock Gating ✓	DFS ✓
Leakage Power	L	Multi-L lib ✓	-
	Vth	Multi-Vth lib ✓	✗
	Switch off (Vdd)	-	Power gating ✓
Variations	Consumer (Vdd)	Static AVS ✓	✗
	Consumer & Auto (Vth)	✗	✗

Body-bias: a unique solution to fully control threshold voltage dynamically





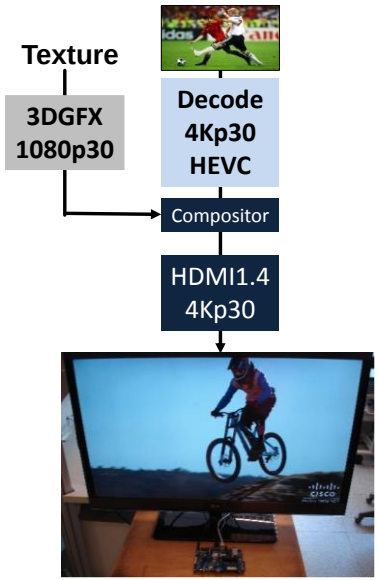
Landscape of low power techniques

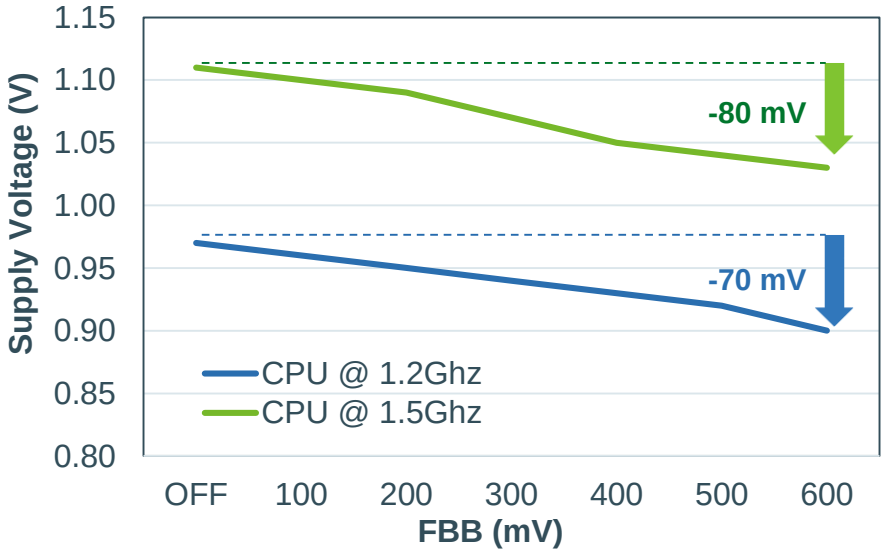
		BULK (Vdd only)		FD-SOI (Vdd + Vbb)	
Source	**Parameter**	**Static Optimization**	**Dynamic Optimization**	**Static Optimization**	**Dynamic Optimization**
Dynamic Power	W	Multi-drive lib ✓	-	Multi-drive lib ✓	-
	Vdd	Multi-Vdd lib ✓	DVS ✓	Multi-Vdd lib ✓	DVS ✓
	Vdd/Vth	Multi-Vdd/Vth lib ✓	✗	Multi-Vdd/Vth/**BB** lib ✓	DV**B**S ✓
	F	Clock Gating ✓	DFS ✓	Clock Gating ✓	DFS ✓
Leakage Power	L	Mult		Multi-L lib ✓	-
	Vth	Multi-Vth lib ✓	✗	Multi-Vth/**BB** lib ✓	**Dynamic ABB** ✓
	Switch off (Vdd)	-	Power gating ✓	-	Power gating ✓
Variations	Consumer (Vdd)	Static AVS ✓	✗	Static AVS ✓	-
	Consumer & Auto (Vth)	✗	✗	**Static ABB (P)** ✓	**Dynamic ABB (T+A)** ✓

This is very unique!!

Adaptive optimization of body-bias and Vdd

- Adaptive body-bias is demonstrated on system running real SW
- Body-Bias enables dynamic power reduction thanks to supply voltage reduction

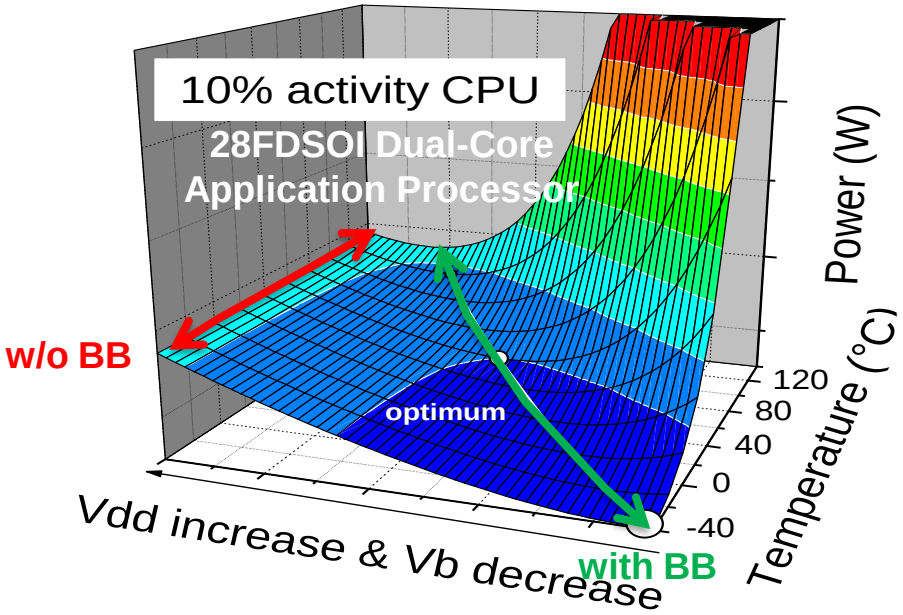




ST, IRPS 2018 – Huard et al., Best Paper preselected

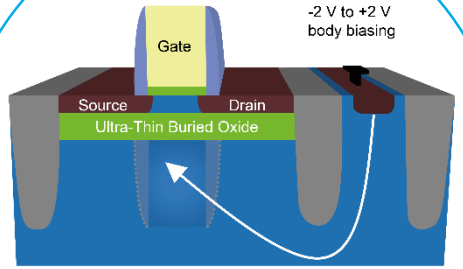
Combining compensation and leakage optimization power mode

- An optimum body bias / Vdd exists for each temperature
- This optimum energy point cannot be accessed by bulk technologies

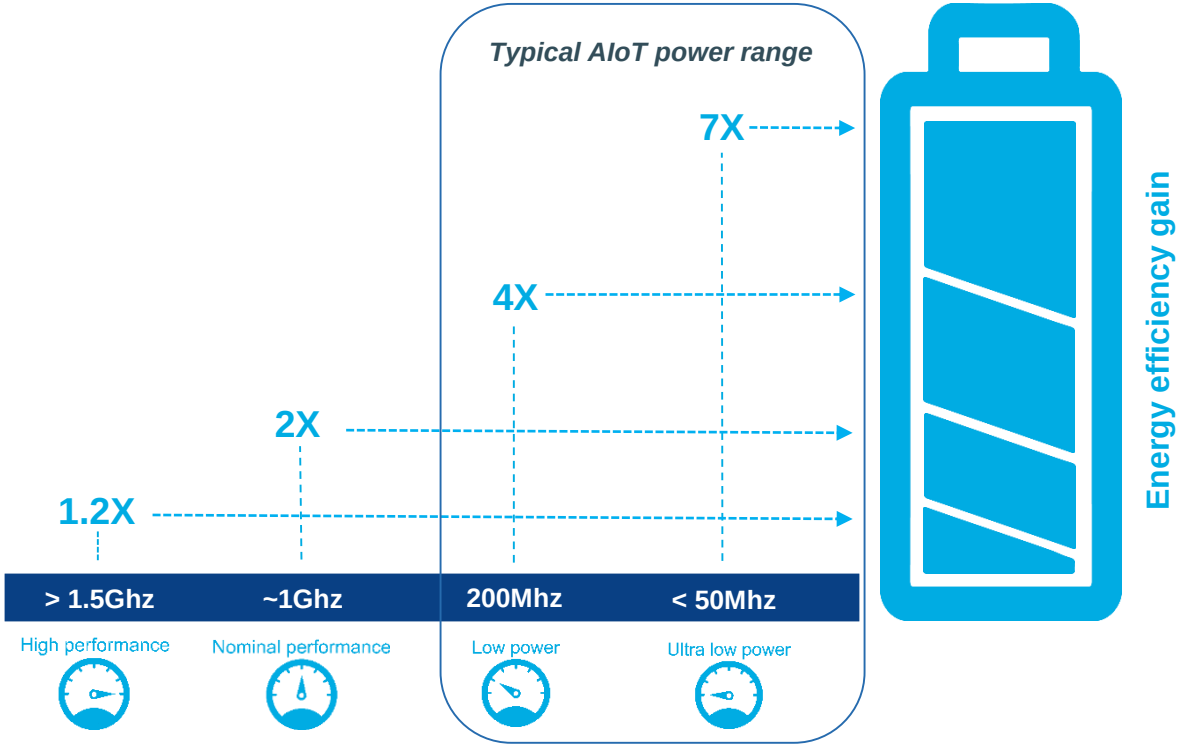


N.B. : Experimental results, ST IRPS 2016

Body Bias



FD-SOI can increase energy efficiency gains by 7 by leveraging its unique body-bias capability



Body-bias impact (AVS, ABB) on energy efficiency

Source: Dolphin Integration, 2018

Body-bias enablement status in the industry

BB Type	Market
Static / Boost	Mobile, Consumer, Computing
Static / Compensation	IoT, Automotive, Mobile, Consumer, Computing , A&D
Dynamic / Compensation	IoT, Automotive, Mobile, Consumer, Computing , A&D
Dynamic / Boost + Compensation	IoT, Automotive, Mobile, Consumer, Computing , A&D

Partial

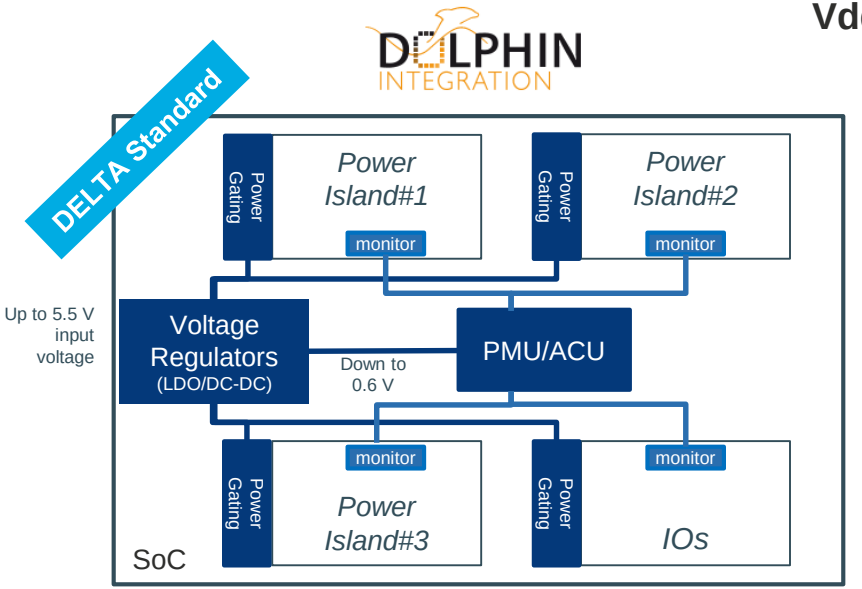
Not Started

A complete power management IP plateform…

Current Dolphin Integration Solution :

Enablement of advanced SoC power architecture to bridge the complexity gap

Vdd modulation



Key features

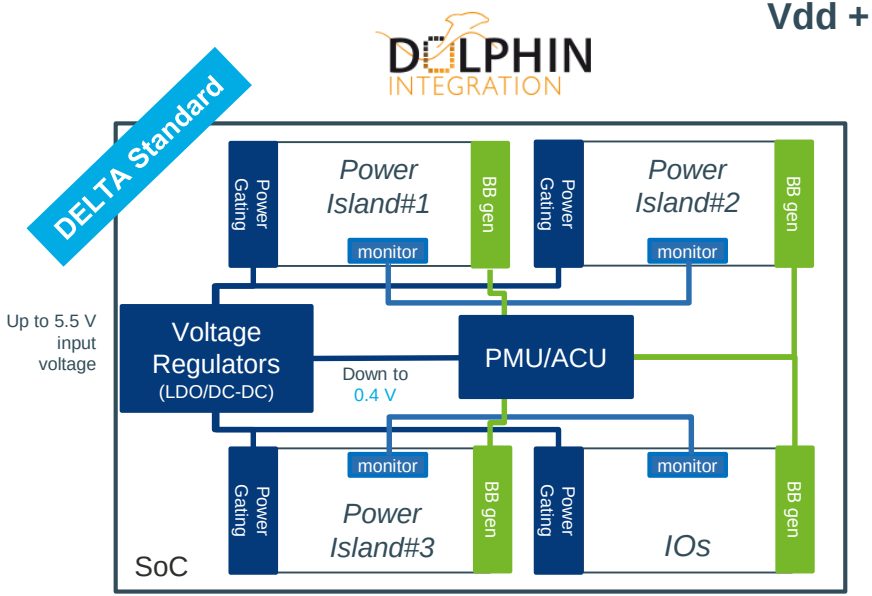
- Wide range of IP offering
- Standardized IPs for streamlined SoC integration
- Scalable according to SoC complexity
- Workable with third-party silicon IPs
- Built-in safety features to prevent SoC failures
- Based on silicon proven IP architectures

… to make body-biasing easy

FD-SOI project – going-on :

Enablement of Adaptive Body Biasing as turnkey solution for best Energy Efficiency without risks

Vdd + Vbb modulation



Key evolutions

- Enhanced Power Management IP Platform Vdd+Vbb
- Fully integrated Power Management IP platform
- Automatic reach of Optimum Energy Point
- Regulation loop for P, V, T & A compensation
- Workable with any standard-cell library & memory
- Design methodology & support

Enabling our customers' products shaping everyday life with engineered substrates

- SOITEC is innovating through substrate technologies bringing solutions to tomorrow technology disruptions
- AI and AIoT will be at the heart of the next human revolution and is moving closer to the edge
- FD-SOI offers unique power efficiency advantages though body bias technologies
- FD-SOI adoption in AIoT is ongoing and will play an increasing role in enabling this new technology disruption

Thank you

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