DOLPHIN INTEGRATION
The Enabler of Low-Power Systems-on-Chip

How to accelerate SoC Power Network Architecture Exploration

IP SoC Day – Grenoble – Martine FALHON – Product Marketing Manager

About Dolphin Integration

Since 1985

HQ in Grenoble, France
Subsidiaries in Canada & Israël

150 highly qualified design engineers for Mixed Signal development

Renowned for

- Silicon IPs
- Design Methodology Software
- ASIC Design & Supply

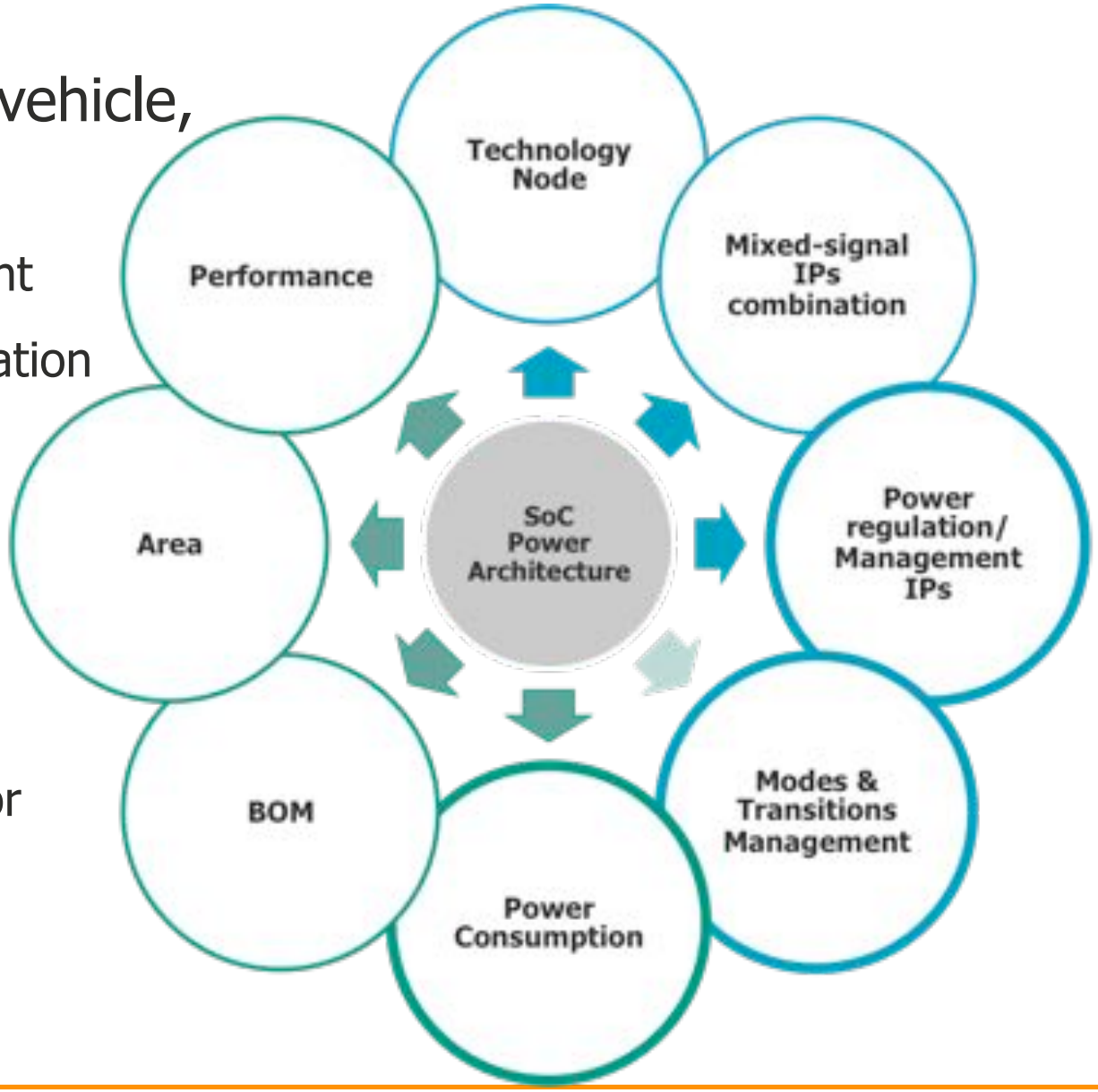
> 200 Silicon IPs available across multiple nodes and foundries

- Power Management
- Standard Cell libraries
- Memory Compilers
- Audio CODECs/ADCs/DACs & Triggers
- Oscillators

> 500 customers worldwide

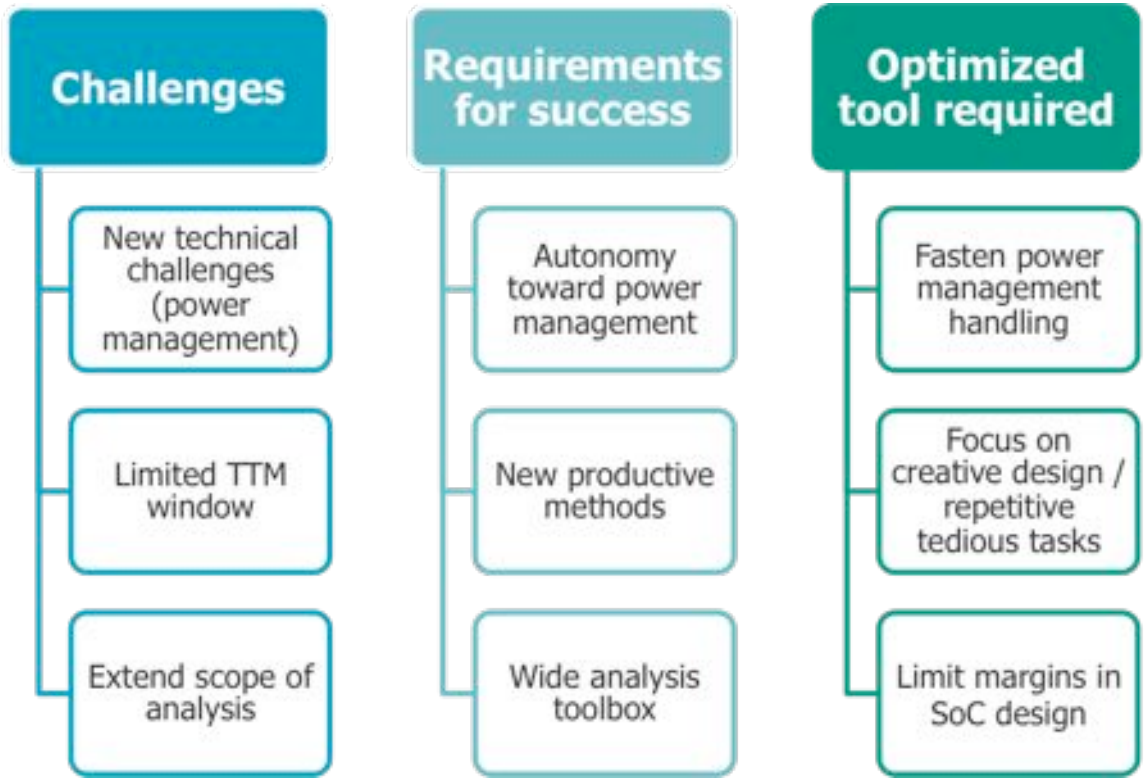
CHALLENGING NEW SOC DESIGNS

- Demanding markets (IoT, Autonomous vehicle, Mobile)
  - Performance is not anymore the only constraint
  - Power consumption has to be part of the equation
- New of smart and energy efficient SoC architectures based on stringent PPA
  - meet end-users quest of compacity
  - counterbalance manufacturing expenses
  - maximized leadtime before battery recharge or replacement
- Manual processing is no more suitable



A GAME CHANGER FOR SOC ARCHITECTS

- SoC Architect, the BIG PICTURE owner
- Energy efficient SoC -> Focus on SoC Power Network



BRIDGE THE GAP BTW SPECIFICATIONS AND EDA TOOLS

DEFINE your SoC architecture
with PowerStudio™

SPEC
from customer

BUILD
a set of SoC achitectures
in PowerStudio

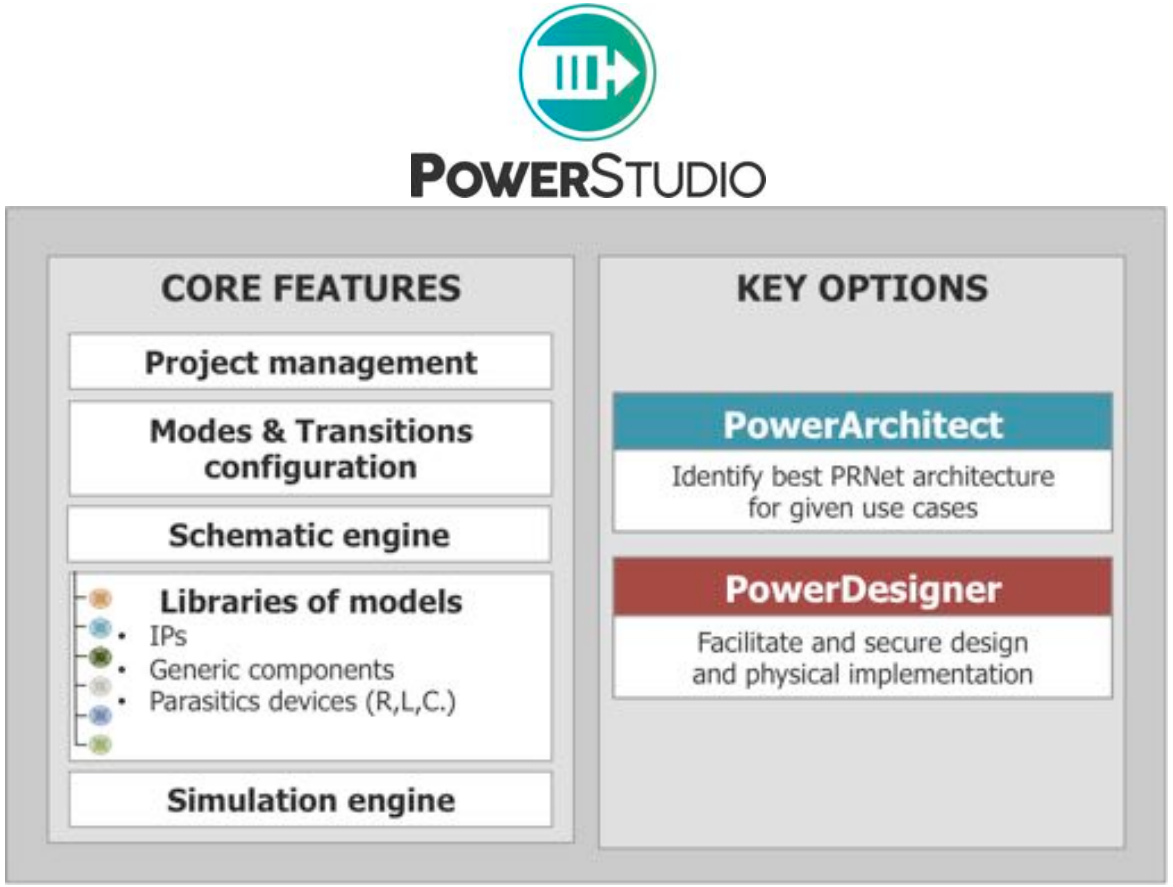
EXPLORE
each candidate architecture
with PowerArchitect

GENERATE
formats of the winning architecture
with PowerDesigner

EDA Solutions

POWERSTUDIO™ FEATURES

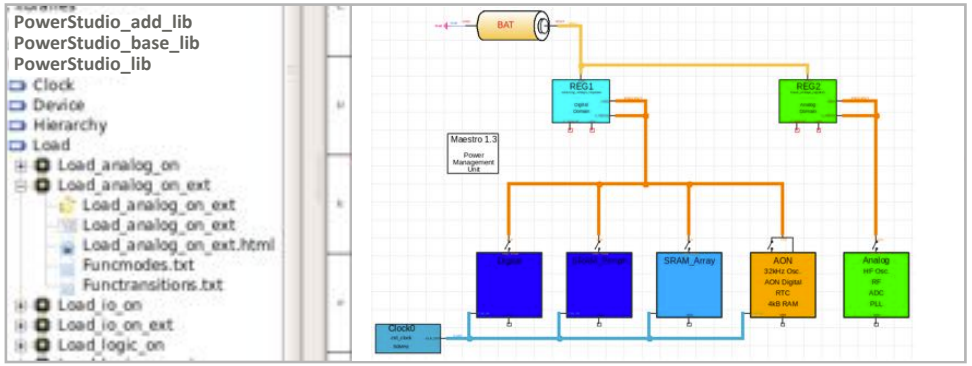
- Core features
  - To **BUILD** a set of candidate SoC power network architectures
  - To RUN all required upcoming simulations
- Key features
  - To **EXPLORE** architectures (PowerArchitect)
  - To **GENERATE** optimized architecture related views (PowerDesigner)



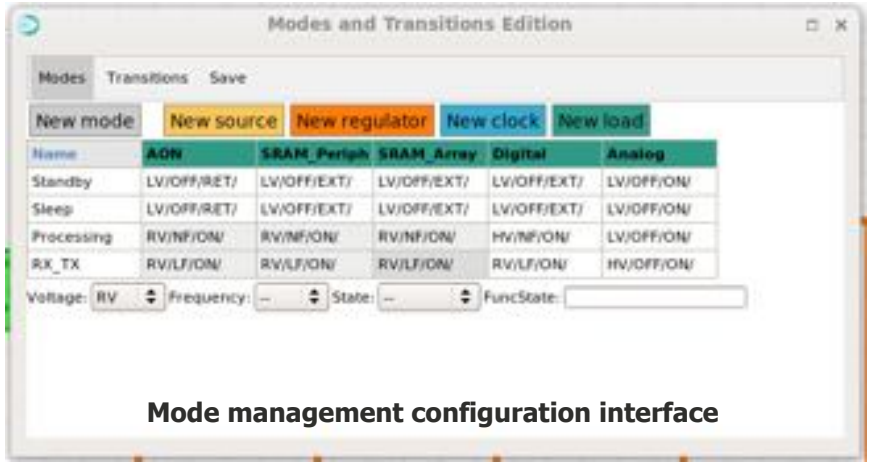
BUILD

BUILD a set of candidates of SoC power network architectures

- Project hierarchy
- Schematics based on a growing library of models
- Modes and transitions
- Build a set of similar synopses for further comparisons



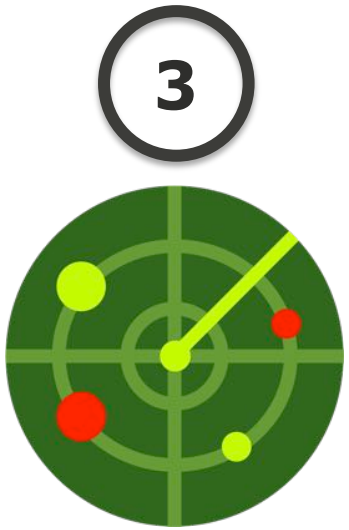
Building of a synoptic in the schematic interface



Mode management configuration interface

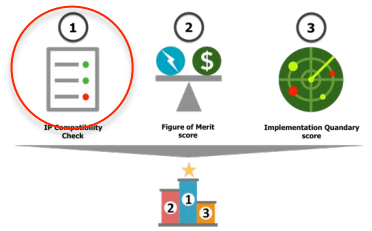
IP Compatibility Check

Figure of Merit score



Implementation Quandary score

IP COMPATIBILITY CHECK (IPCC)



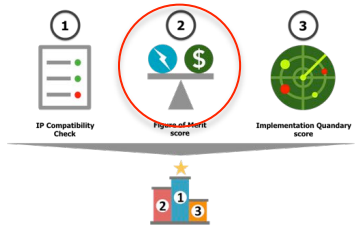
- Early detect big inconsistencies in conception
- Control cross-block electrical specifications compatibility in each mode - input/output voltage, output current and impedance
- Check power supplies can provide the level of current expected by their respective associated loads

✓	0	0	44	MODE
✓	0	0	11	Standby
✓	0	0	11	Sleep
✓	0	0	8	VOLTAGE CHECK
✓	0	0	3	CURRENT CHECK
✓	Check current value is in range 0A 500e-3A	• Description: Check if current on instance BAT port VOUT is in range 0A 500e-3A • current 1.003e-3A is in range 0A 500e-3A		
✓	Check current value is in range 0A 500e-3A	• Description: Check if current on instance REG1 port VREG is in range 0A 500e-3A • current 52.75e-9A is in range 0A 500e-3A		
✓	Check current value is in range 0A 2e-3A	• Description: Check if current on instance REG2 port VREG is in range 0A 2e-3A • current 1.001e-3A is in range 0A 2e-3A		
✓	0	0	11	Processing
✓	0	0	8	VOLTAGE CHECK
✓	Check voltage value is in range 564e-3V 660e-3V	• Description: Check if voltage on instance AON port VDD is in range 564e-3V 660e-3V • voltage 599.9e-3V is in range 564e-3V 660e-3V		
✓	Check voltage value is in range 564e-3V 660e-	• Description: Check if voltage on instance AON port VDD_PSW is in range 564e-3V 660e-3V • voltage 599.8e-3V is in range 564e-3V 660e-3V		

IPCC results display

FIGURE OF MERIT SCORE (FOM)

- Cost efficiency evaluation
- FOM configuration factors
  - Area (SoC components + Pads & Pins for bounding)
  - BOM (peripheral devices)
  - Power consumption (at component and mode levels)
- Sub score weighting / constraints
- Architectures ranking based on respective FOM score comparison



FOM score
=
Area*% + BOM*% + Power consumption*%
(Wa + Wb + Wp = 100%)

The lower the better

Synopsis	Total area (mm2)		BoM costs			Power consumption at battery source (mW)			FoM
	Core	Pads	C	L	Package pins	Active mode	Sleep mode	Total	
#1	1.58	1.65	2	2	10	20.52	0.016	0.103	0.135
#2	0.18	0.24	1	0	3	36.36	0.194	0.192	0.191
#3	0.68	0.71	1	1	5	20.35	0.015	0.102	0.115
#4	0.91	0.94	1	1	5	20.35	0.015	0.102	0.119
#5	0.68	0.71	1	1	5	20.27	0.015	0.102	0.114

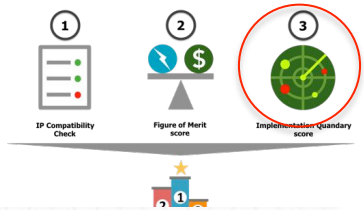
Area of PRNet

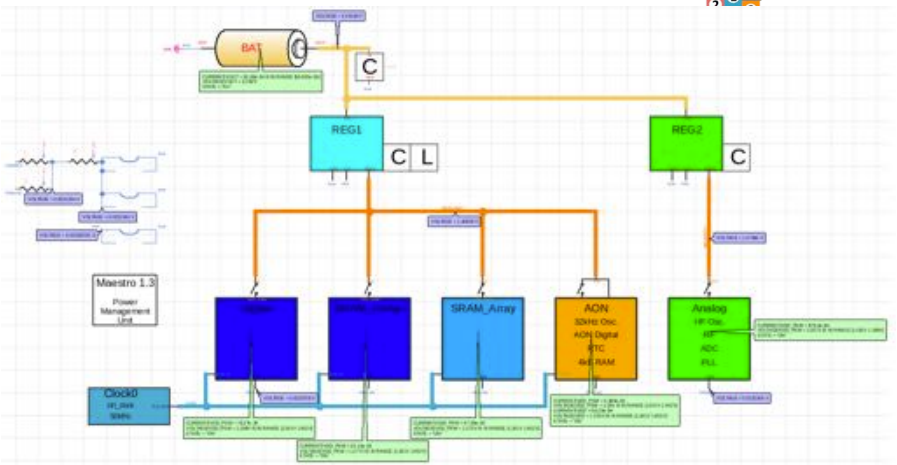
Power Consumption at battery source

Comparison of a set of candidate architectures based on their respective FOM scores

IMPLEMENTATION QUANDARY SCORE (IQ)

- Risk evaluation of component implementation
- Early detection of power integrity issues
- IQ configuration factors
  - Potential noise level generated by agressors (digital loads, regulators)
  - Noise tolerance level of potential victims (analog loads)
- Consolidated view of
  - Level of noise generated by power supply oscillations deterioring the SoC performance
  - Frequences propagation path monitoring
  - Risk of side load aggression
- Architectures ranking based on respective IQ score comparison





CASE	SCORE				IQ
	Sleep	Standby	Processing	RX_TX	
Simple1	-6.97e-08	0.000749	0.0315	0.0106	0.0315

Standby			
Victim	Frequency	Signal	Value
Analog	1e+06	V(Simple1.REG2VOUT,Simple1.VSSANA)	0.000749

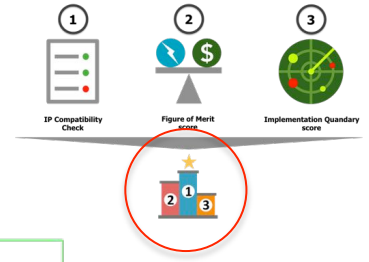
Processing			
Victim	Frequency	Signal	Value
Analog	6.31e+05	V(Simple1.REG2VOUT,Simple1.VSSANA)	0.0315

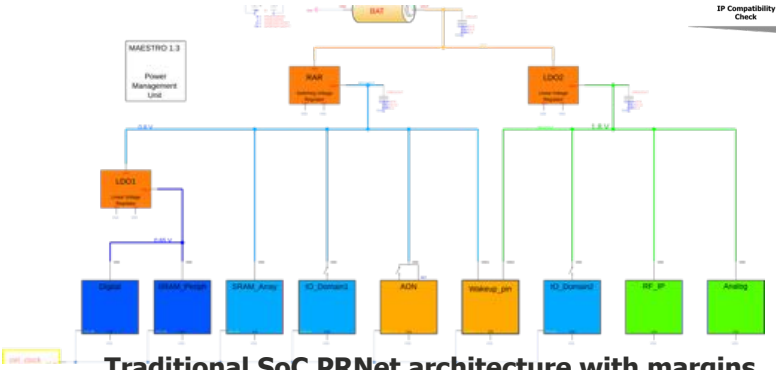
Sleep			
Victim	Frequency	Signal	Value
Analog	1e+06	V(Simple1.REG2VOUT,Simple1.VSSANA)	-6.97e-08

IQ results for one candidate architecture

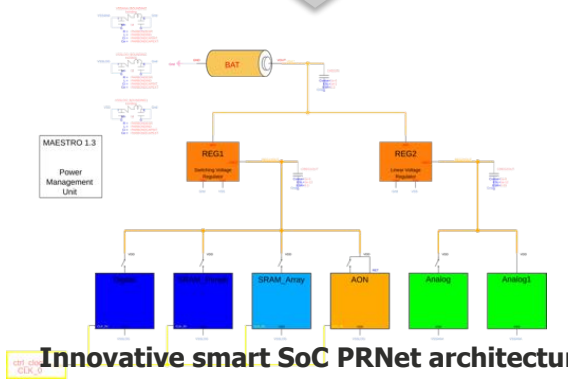
BEST OPTIMIZED ARCHITECTURE

- Compare both FOM and IQ score rankings
- Identify the best trade-off between cost-efficiency and risk of implementation
- From traditional SoC power network architectures to more innovative combinations





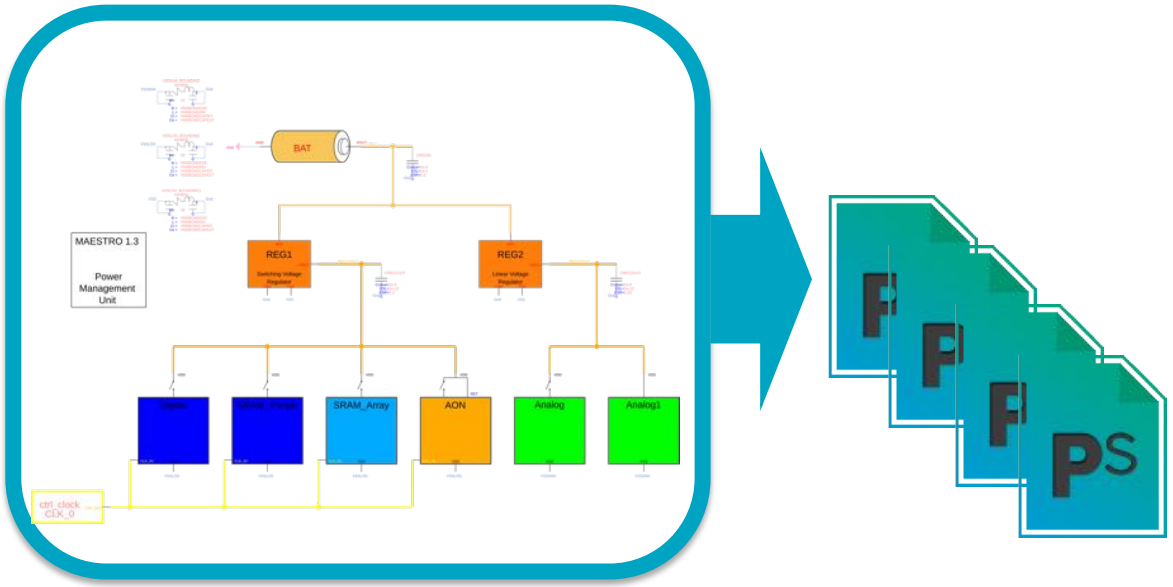
Traditional SoC PRNet architecture with margins



Innovative smart SoC PRNet architecture

GENERATE FORMATS

- From architecture to design stage
  - Budget views
  - Aligned UPF/RTL Top views
  - Dolphin Power Management Unit (MAESTRO) configuration file
- Mirrors all the strategic data of your winning synoptic
- Forget tedious manual generation of views



How will PowerStudio™ add value to architects?

VALUE-ADDED FEATURES

- Agile project management
- Modes configuration interface
- Ever-growing centralized library of IP models
- User-friendly schematics
- Wide scope of exploration criteria
- Automatic views generation
- Noise propagation simulation
- Results export

BENEFITS FOR ARCHITECTS

- Increasing range of PRNet architectures assessed
- Cost efficiency
- Risk limitation

→ Smart and optimized PRNet architecture definition

- Faster PRNet architecture exploration
- Right-on-first pass PRNet architecture (no iteration loop)
- Smart bridge from Architecture to Design

→ Global TTM reduction

SAVE THE DATE

- PowerStudio™ v1.0
  - Includes PowerArchitect's SoC power network architecture exploration key feature
  - Available on January 7th, 2019
- Apply now to become a Beta Tester!
  - Looking for Beta Testers to integrate the PowerStudio™ V1.0 Beta Test program
  - Apply at contact@dolphin.fr

Thank You

Input

- **Key architecture components** and their distribution within Power Islands
- **Modes & Transitions**
- **Power, Area, BoM**-related specific information of each power islands
- **% of use of each mode**
- **Global weight** of Area, BoM & Power for candidate architectures' FoM calculation

PowerStudio™ v1.0
PowerArchitect

Output

- **Scoring/checks algorithms**
  - **IPCC:** Check of PRNet components compatibility **(compatibility check)**
  - **FoM:** Score consolidating weighted BoM, Area and Power consumption for a given architecture. The set of weights of a FoM reflects a specific use case constraints **(cost efficiency optimization index)**
  - **IQ:** Evaluates the noise resilience of a circuit in regards on the various levels of impact that frequency variations propagated through the candidate architecture may have on sensitive loads **(power integrity index)**
- **Results**
  - **Comparison of the analysis results** of a given set of architectures
  - **Export**
    - **to MS Excel**
    - **New export formats to come (PowerDesigner™):** RTL top, UPF top, budgets, and other useful files related to the winning architecture