

Addressing the Energy Efficiency Challenges of IoT end points

D&R IP-SoC Days, Grenoble — December 5[™] 2018

PIERRE GAZULL - BUSINESS DEVELOPMENT & PRODUCT MARKETING MANAGER, IOT







• Since 1985



- HQ in Grenoble, France
- Subsidiaries in Canada & Israel



 About 150 highly qualified engineers



 Strong leadership in ultra-low power and energy-efficient SoC & IP design



> 200 Silicon IPs available across multiple nodes and foundries



> 500 customers worldwide





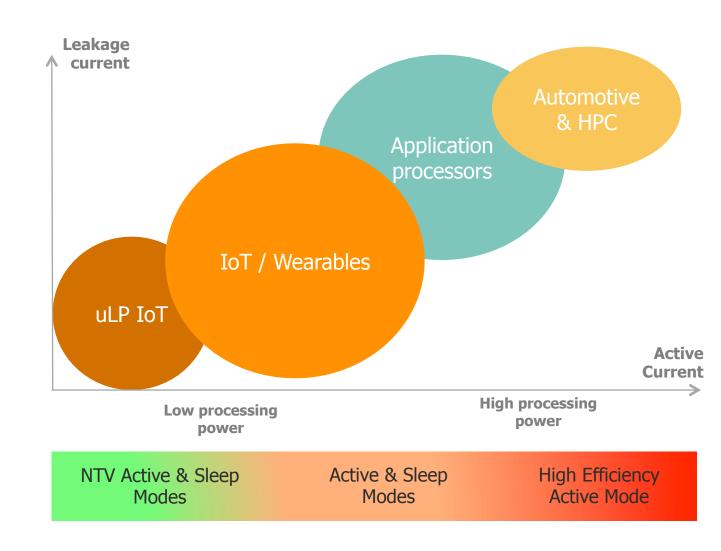


Bridging the Complexity Gap to Design Energy-Efficient SoCs

- Power Efficient Silicon IPs Platform
- Power Network Exploration & Design Tools
- ASIC Design & Supply Services



- Energy efficient products make better products
 - → Cheaper package
 - → Better BoM costs
 - → Higher reliability
 - → Longer battery operation
 - → Smaller form factor







Energy efficiency challenges

Breakthrough Power Management IPs Portfolio

SoC Power Network Exploration

Example on NB-IoT



IOT DEVICES MISSION PROFILES

SMART CITY IOT DEVICES

- Low-cost and small form factor
- Connect to the gateway or direct to cloud
- Mesh or Cellular (NB-IoT)
- Battery powered in remote locations with 10 years operation

Use cases

Environment monitors, utilities metering, smart lighting, asset tracking,



CONSUMER IOT DEVICES

- Connected device balancing performance & power
- Local data or audio processing capabilities
- Integrated BLE
- Rechargeable battery powered

Use cases

asset monitoring, wearables,



EDGE COMPUTING IOT DEVICES

- IoT end points with high levels of data processing and context-based decision making such as AI at the edge
- Integrated BLE, WiFi or Cellular (NB-IoT or LTE-M)
- Wall and battery powered

Uses cases

Smart Home & Industrial gateway, surveillance cameras,

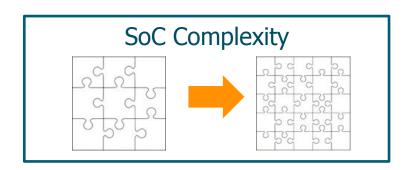




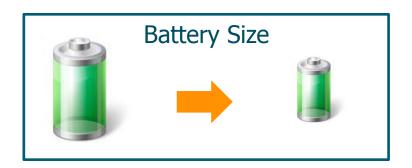
Market trends for battery-operated devices: Get the highest

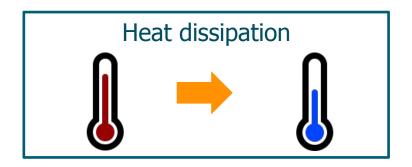
SoC energy efficiency





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CHALLENGES FOR DESIGNING ENERGY EFFICIENT SOCS



How to speed-up the power architecture exploration and selection?



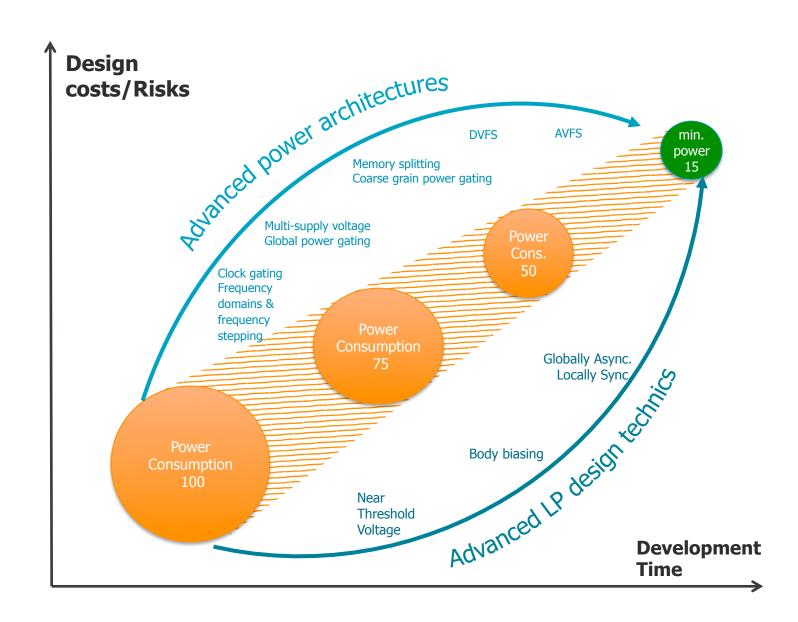
How to leverage on IP power modes and adopt more complex power architectures ?
How to streamline this adoption?



How to reduce design, fabrication and BoM costs?



How to safely speed-up the design of complex and noise-sensitive Mixed-Signal SoCs ?



Min. Power 15

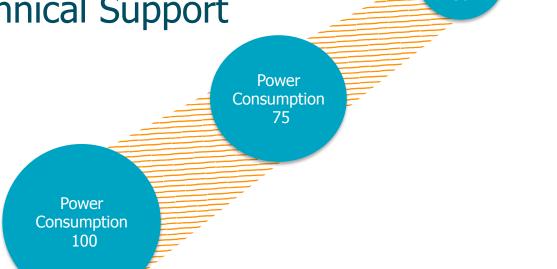
Power Cons. 50

Power Managements IPs Portfolio

Methodologies & Design Tools for SoC

Architecture Exploration

Expert Technical Support









Energy efficiency challenges

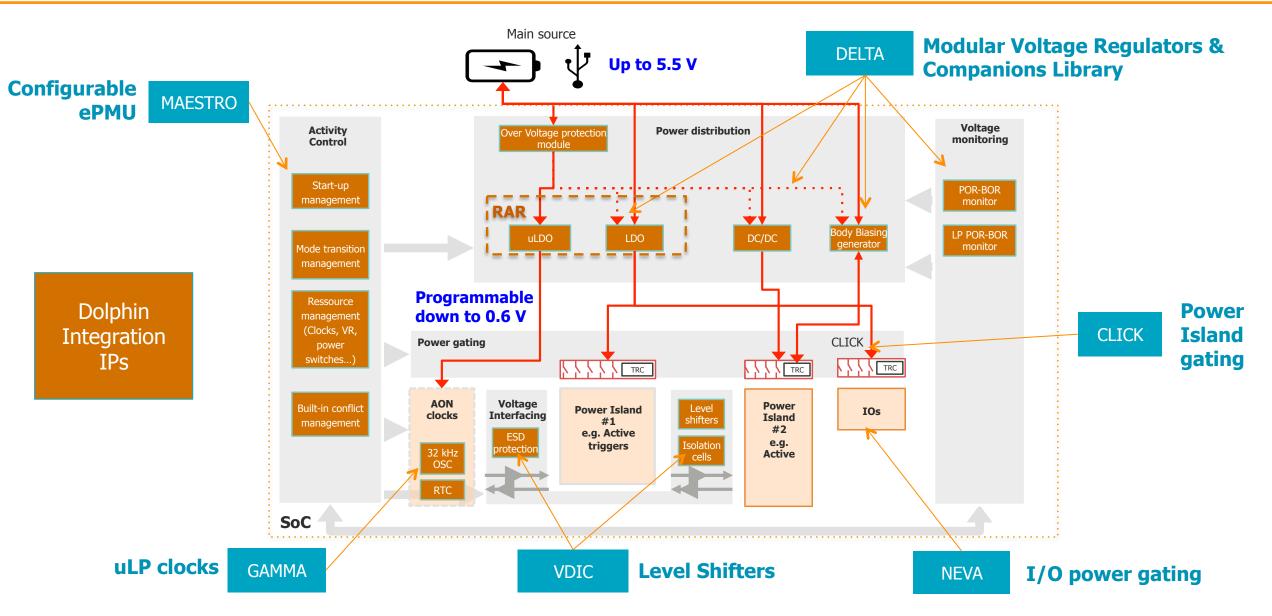
Breakthrough Power Managements IPs Portfolio

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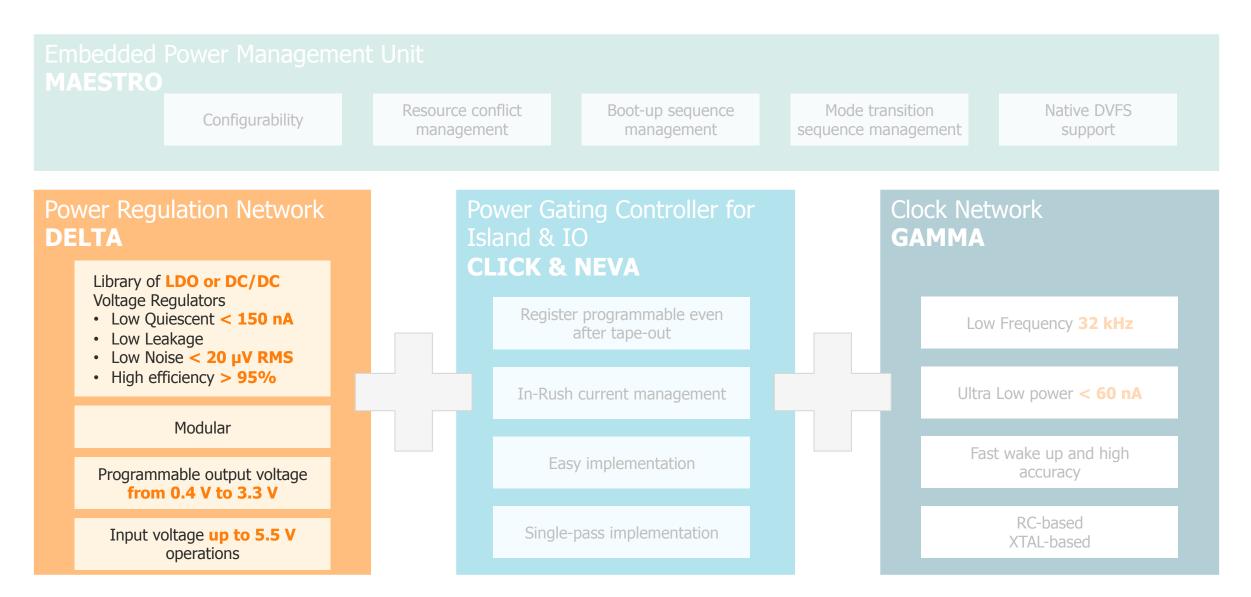


A COMPLETE POWER MANAGEMENT IPS PORTFOLIO

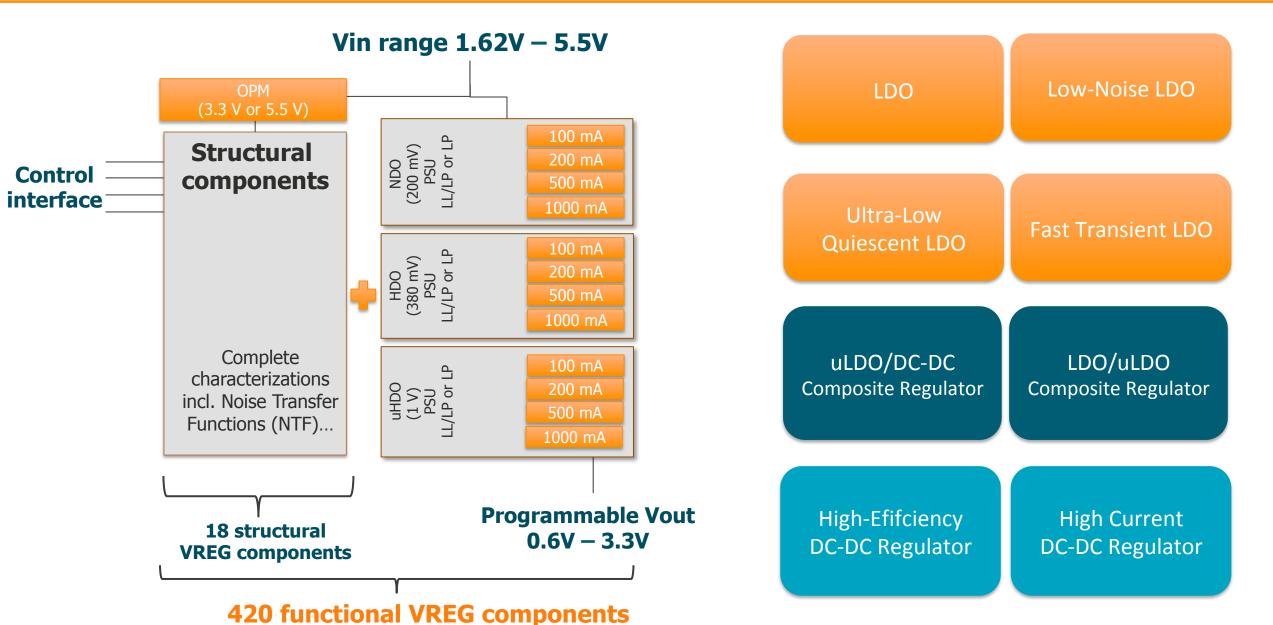




POWER MANAGEMENT IPS HIGHLIGHTS



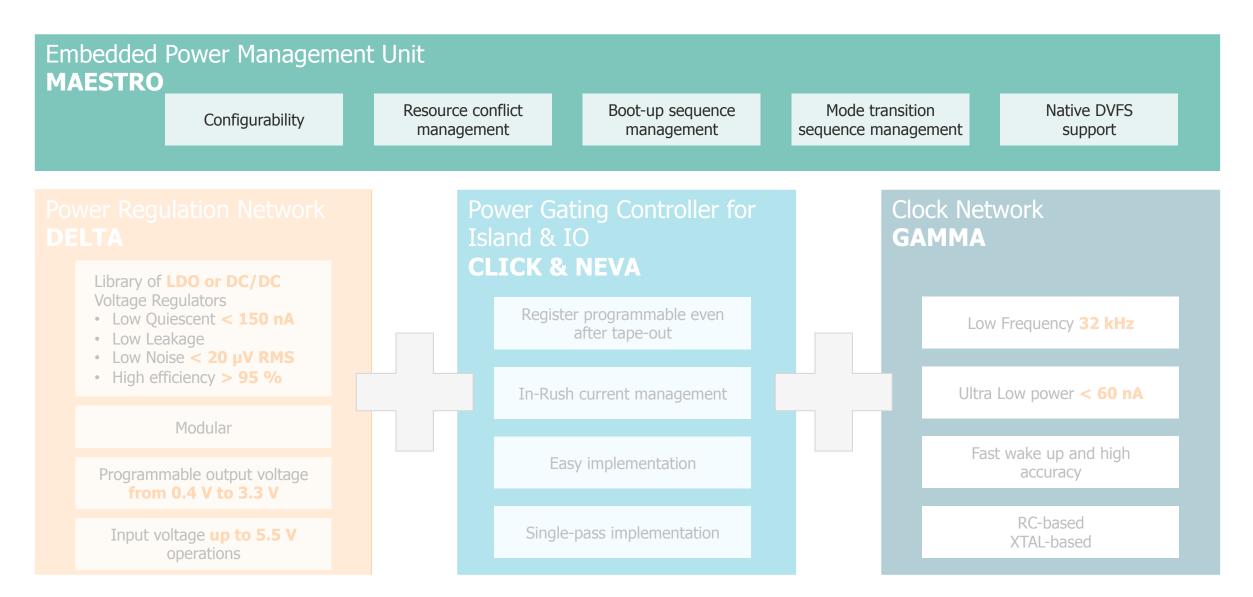




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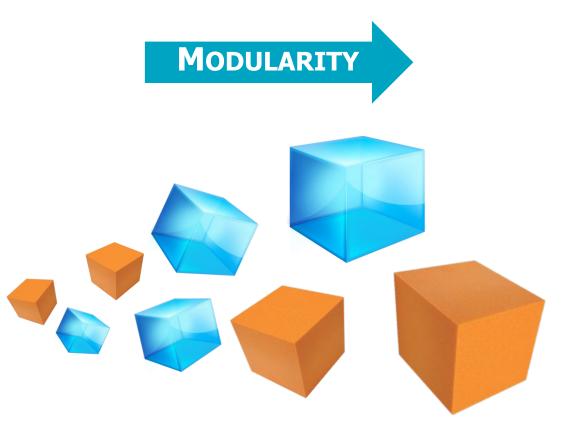
POWER MANAGEMENT IPS HIGHLIGHTS

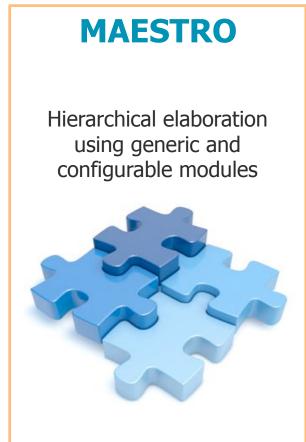




FROM CUSTOM PMU TO CONFIGURABLE EPMU

FULL CUSTOM Complex elaboration with unexpected oversights







MAESTRO EPMU GENERATOR

Power Island Mode Table

Defined bySoC Architect

SoC specifications and functionalities

SoC Functional operating mode			CPU Data SRAM	DMA / SPI I2C / WDT	ADC Data SRAM		
Active	0.7 V 32 KHz Active	0.7 V 32 KHz Active	1.1 V 32 MHz Active	1.1 V 32 MHz Active	1.1 V 32 MHz Active		
ADC monitor	0.7 V 32 KHz Active	0.7 V 32 KHz Active	0.9 V 32 MHz Active	0.9 V Retention	0.9 V 4 MHz Active		
Sleep	0.7 V 32 KHz Active	0.7 V 32 KHz Active	0.9 V Retention	0.9 V Retention	0.9 V Retention		
0.7 V <i>OFF</i> 32 KHz Active		OFF	OFF	OFF	OFF		

Mode transition sequences ADC Monitor -> DMA Boot-up sequence Sleep -> ADC Monito Island#1 Island #4 Island #4 (0.5V/Retention 08.7V/32XHz/Active Island #3 Island #0 (0.9V/4MHz/Active Island #2 Island#3 ELIV/22MHg/Active 10.9V/4MHz/Active (1.1V/32MHz/Activ Island #2 Island #3 (1.1V/32MHz/Active) Mand #4



Maestro ePMU RTL

Maestro SW drivers

Maestro core

Sits in the AON domain

Core controller

 Handles register programming, power-up sequence and mode change sequences

Event handler

Manages events to execute mode change sequence automatically

Resource controller

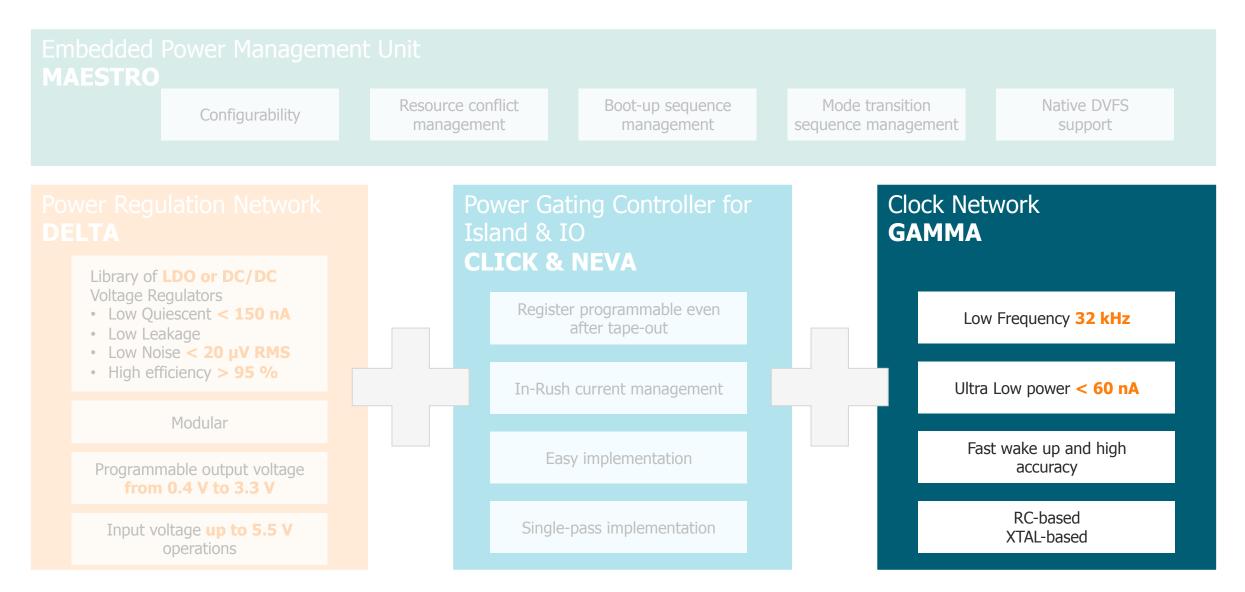
- Arbitration of island controller requests
- Voltage settings, voltage regulator modes, clocks

Island controller

- Split between AON and switchable domains
- Power domain states, isolation cells, in-rush current setting, wake-up time
- Request to resource controllers and power switch controller



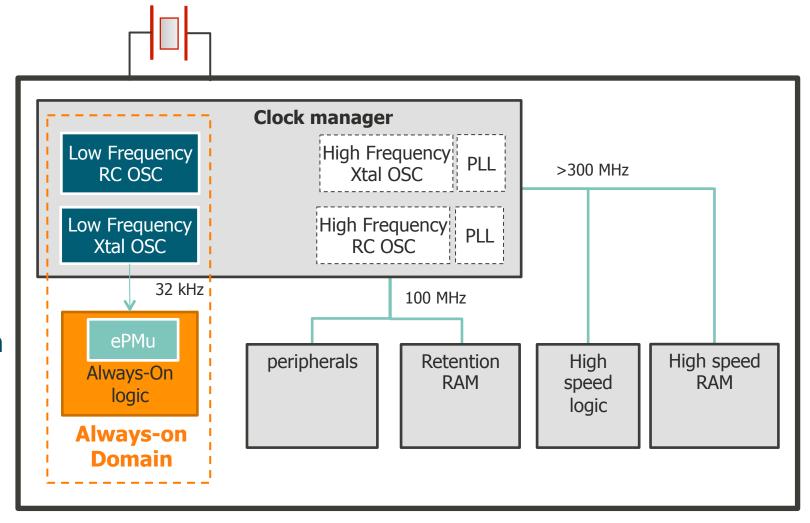
POWER MANAGEMENT IPS HIGHLIGHTS



CLOCK NETWORK IN AN SOC

Low frequency oscillators

- Count the time during sleep modes
- < 32 kHz
- In AON domain



High frequency oscillators:

- >1 MHz
- For a use in active mode

Our offering targets **low frequency oscillators** to optimize the power consumption of the Always-on domain



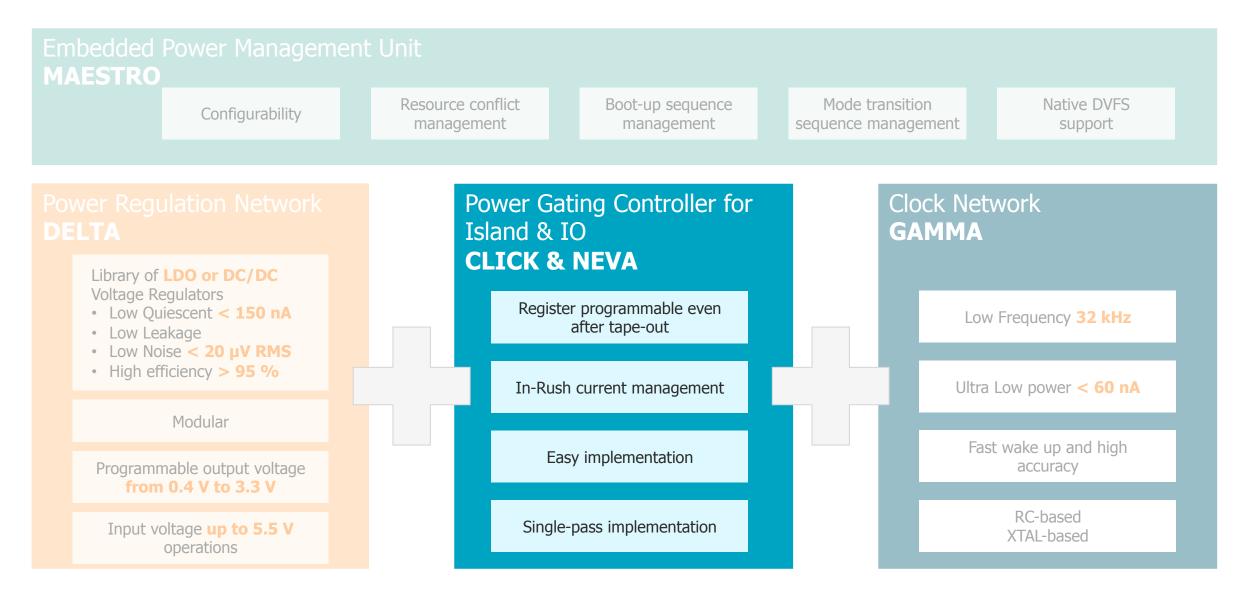
OUR OSCILLATORS FOR ALWAYS-ON DOMAIN

Oscillators	RC	XTAL						
Frequency	32 kHz	32.768 kHz						
Input voltage range	0.49 - 1.21 V	0.49 - 1.21 V						
Power consumption	~ 70 nA	~ 50 nA						
BoM Cost	No external component	External quartz needed						
Accuracy	Lower accuracy and stability +/- 5 % after trimming	Very precise and stable over a wide temperature range +/- 0.05 % without capacitor Could reach +/- 0.005 % with external capacitors						
Start-up Time	Fast startup time ~200 µs	Longer start-up time ~400 ms						
Frequency	programmable	Not programmable						
Silicon area	~ 0.040 mm ²	~ 0.042 mm ²						
Target Applications	Frequent awakenings	High accuracy						

Note: Performances data for 40 nm and 55 nm



POWER MANAGEMENT IPS HIGHLIGHTS







Energy efficiency challenges

Breakthrough Power Management IPs Portfolio

SoC Power Network Exploration

Example on NB-IoT

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NB-IoT Application Requirements



Activity Scenarios

RF transmit mode:

3 s/day

RF receive mode:

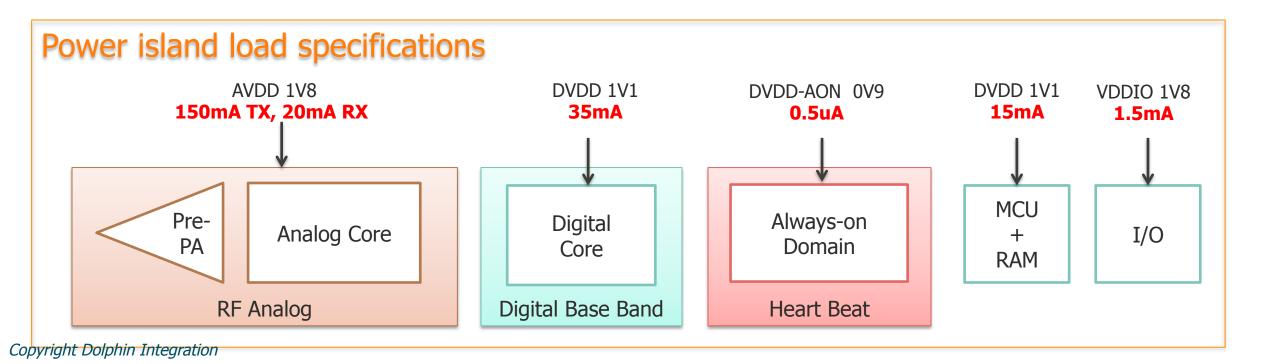
12 s/day

30 s/day Compute mode (RF off):

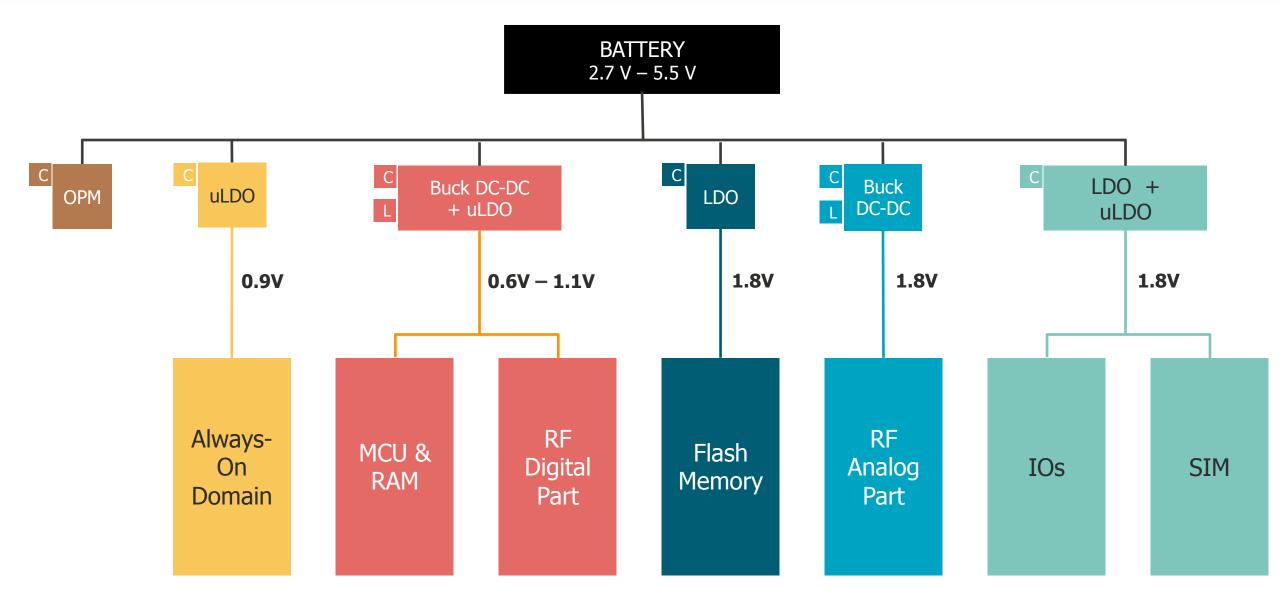
Deep sleep mode:

Rest of the day (99.99%)

Battery autonomy: 10 years

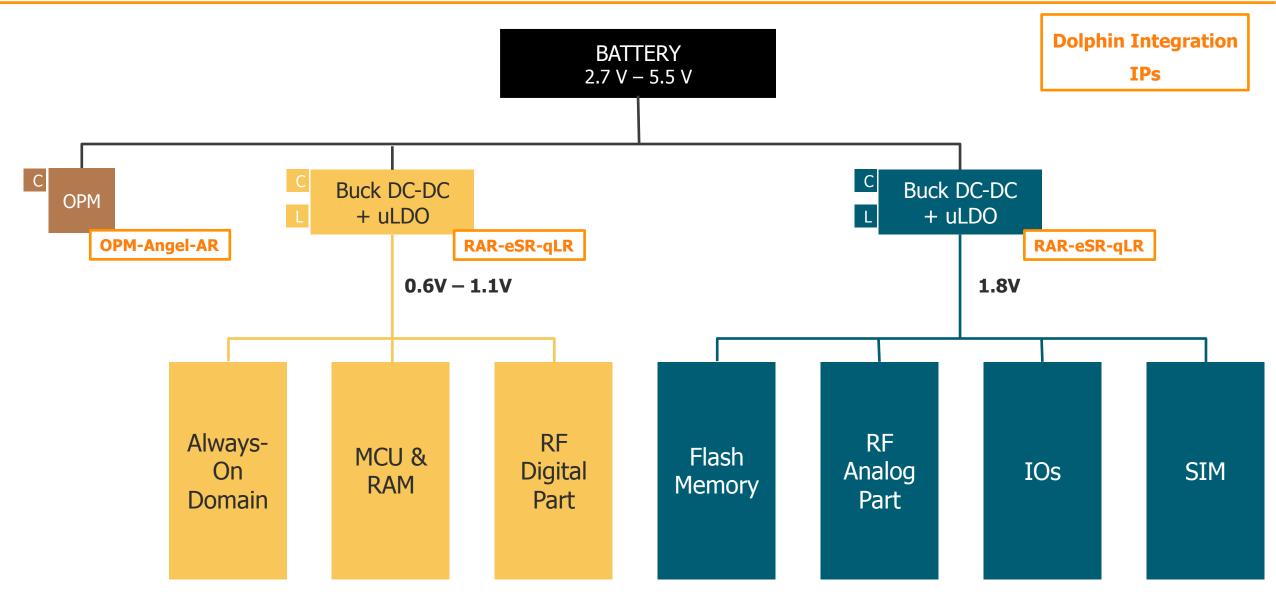








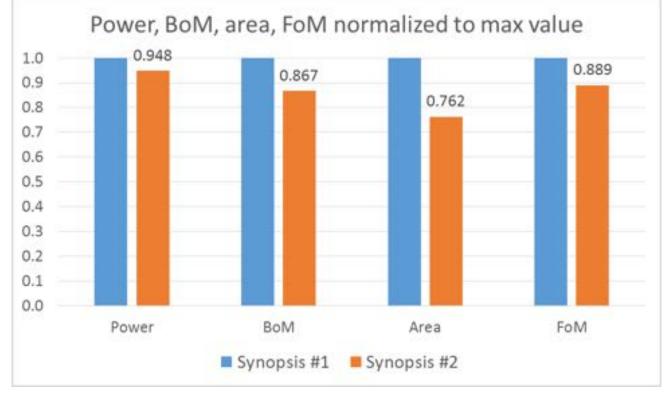
NB-IoT Architecture #2 : Optimization with Power Architect





ARCHITECTURE SELECTION WITH POWER ARCHITECT

	Current at battery source (A)			Relative contribution of each mode based on activity cycle			ВоМ	ВоМ	Area of VR	FoM	FoM, normalized	Lifetime @ 1000 mAh	I DODODO TOR III-I		
	Average at battery source	RF transmit RF receip	StandBy mode	Processing mode	RF Tx	RF Rx	StandBy mode	Processing mode	count	(weighted)	(mm2)			(years)	lifetime (mAh)
Synopsis #1	12,09E_6	88,75E_3 33,69E_	3 2,24E_6	6,02E_3	25,5%	38,7%	18,5%	17,3%	2L, 5C	30	2,962	1,000	1,124	9,441	1 059
	11 465 6	113,69E_	2 2 005 6	4.075.3	2.4.40/	22.20/	10 10/	1 = 10/	21 20	26	2.250	0.000	4.000	0.050	4.004
Synopsis #2	11,46E ₋ 6	3 26,69E	3 2,08E_6	4,97E ₋ 3	34,4%	32,3%	18,1%	15,1%	2L, 3C	26	2,258	0,889	1,000	9,960	1 004



Silicon Area is reduced by ~ 25%

& BoM is reduced by $\sim 15\%$

Without degrading battery lifetime



- Energy-efficient SoCs are mandatory to reach the IoT market requirements in terms of battery autonomy
- Dolphin provides a comprehensive Power Management IPs platform to speed-up the design of energy-efficient SoCs
 - → Consistent, modular, standardized Power Management IPs Portfolio
 - → Customer configurable ePMU for easy and safe control of the SoC power modes
 - → Design Tools for quickly exploring and deciding on the most optimal on-chip Power Regulation Network



