Addressing the Energy Efficiency Challenges of IoT end points

D&R IP-SoC DAYS, GRENOBLE – DECEMBER 5th 2018

PIERRE GAZULL – BUSINESS DEVELOPMENT & PRODUCT MARKETING MANAGER, IoT
• Since 1985

• About 150 highly qualified engineers

> 200 Silicon IPs available across multiple nodes and foundries

• HQ in Grenoble, France

• Subsidiaries in Canada & Israel

• Strong leadership in ultra-low power and energy-efficient SoC & IP design

> 500 customers worldwide
Bridging the Complexity Gap to Design Energy-Efficient SoCs

• Power Efficient **Silicon IPs Platform**
• Power Network Exploration & Design **Tools**
• ASIC Design & Supply **Services**
• Energy efficient products make better products
  ➔ Cheaper package
  ➔ Better BoM costs
  ➔ Higher reliability
  ➔ Longer battery operation
  ➔ Smaller form factor

ADDRESSING GROWING MARKETS

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Energy efficiency challenges

Breakthrough Power Management IPs Portfolio

SoC Power Network Exploration

Example on NB-IoT
## IoT Devices Mission Profiles

### Smart City IoT Devices
- Low-cost and small form factor
- Connect to the gateway or direct to cloud
- Mesh or Cellular (NB-IoT)
- **Battery powered in remote locations with 10 years operation**

**Use cases**
- Environment monitors, utilities metering, smart lighting, asset tracking,

### Consumer IoT Devices
- Connected device balancing performance & power
- Local data or audio processing capabilities
- Integrated BLE
- **Rechargeable battery powered**

**Use cases**
- Smart Home & Industrial gateway, surveillance cameras,

### Edge Computing IoT Devices
- IoT end points with high levels of data processing and context-based decision making such as AI at the edge
- Integrated BLE, WiFi or Cellular (NB-IoT or LTE-M)
- **Wall and battery powered**

**Uses cases**
- Asset monitoring, wearables,

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Market trends for battery-operated devices: Get the highest SoC energy efficiency

- Replacement frequency
- Battery Size
- SoC Complexity
- Heat dissipation
CHALLENGES FOR DESIGNING ENERGY EFFICIENT SOCs

How to speed-up the power architecture exploration and selection?
How to leverage on IP power modes and adopt more complex power architectures? How to streamline this adoption?
How to reduce design, fabrication and BoM costs?
How to safely speed-up the design of complex and noise-sensitive Mixed-Signal SoCs?

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• Power Managements IPs Portfolio
• Methodologies & Design Tools for SoC Architecture Exploration
• Expert Technical Support
Energy efficiency challenges

Breakthrough Power Managements IPs Portfolio

SoC Power Network Exploration

Example on NB-IoT
A COMPLETE POWER MANAGEMENT IPs PORTFOLIO

Configurable ePMU MAESTRO

Dolphin Integration IPs

Activity Control
- Start-up management
- Mode transition management
- Resource management (Clocks, VR, power switches...)
- Built-in conflict management

Main source
- Up to 5.5 V
- Voltage monitoring
- POR-BOR monitor
- Level shifters
- Isolation cells
- ESD protection

Power distribution
- Over Voltage protection module
- DC/DC
- Body Biasing generator
- Power Island #1 e.g. Active
- Power Island #2 e.g. Active
- Power Island gating

Programmable down to 0.6 V
- uLDO
- LDO

Power gating
- AON clocks
- Voltage Interfacing
- 32 kHz OSC
- RTC
- ESD protection
- Power Island #1 e.g. Active triggers
- Level shifters
- Isolation cells

Voltage monitoring
- POR-BOR monitor
- LP POR-BOR monitor

Built-in conflict management

Built-in resource management (Clocks, VR, power switches...)

Modular Voltage Regulators & Companions Library

CLICK Island gating

Power Island gating

CLICK

I/O power gating

NEVA

Level Shifters

VDIC

GAMMA

uLP clocks

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### Embedded Power Management Unit

**MAESTRO**
- Configurability
- Resource conflict management
- Boot-up sequence management
- Mode transition sequence management
- Native DVFS support

### Power Regulation Network

**DELTA**
- Library of LDO or DC/DC Voltage Regulators
  - Low Quiescent < 150 nA
  - Low Leakage
  - Low Noise < 20 µV RMS
  - High efficiency > 95%
- Modular
- Programmable output voltage from 0.4 V to 3.3 V
- Input voltage up to 5.5 V operations

### Power Gating Controller for Island & IO

**CLICK & NEVA**
- Register programmable even after tape-out
- In-Rush current management
- Easy implementation
- Single-pass implementation

### Clock Network

**GAMMA**
- Low Frequency 32 kHz
- Ultra Low power < 60 nA
- Fast wake up and high accuracy
- RC-based XTAL-based

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*Copyright Dolphin Integration*
Voltage Regulators built upon reusable and common IP components

Vin range 1.62V – 5.5V

Structural components

- OPM (3.3 V or 5.5 V)
- Complete characterizations incl. Noise Transfer Functions (NTF)

Control interface

Programmable Vout 0.6V – 3.3V

18 structural VREG components

420 functional VREG components

LDO

Low-Noise LDO

Ultra-Low Quiescent LDO

Fast Transient LDO

uLDO/DC-DC Composite Regulator

LDO/uLDO Composite Regulator

High-Efficiency DC-DC Regulator

High Current DC-DC Regulator

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FROM CUSTOM PMU TO CONFIGURABLE ePMU

FULL CUSTOM
Complex elaboration with unexpected oversights

MODULARITY

MAESTRO
Hierarchical elaboration using generic and configurable modules

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### Maestro ePMU Generator

#### Power Island Mode Table

<table>
<thead>
<tr>
<th>SoC Functional operating mode</th>
<th>AON</th>
<th>Island #1</th>
<th>Island #2</th>
<th>Island #3</th>
<th>Island #4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>0.7 V 32 KHz Active</td>
<td>0.7 V 32 KHz Active</td>
<td>1.1 V 32 MHz Active</td>
<td>1.1 V 32 MHz Active</td>
<td>1.1 V 32 MHz Active</td>
</tr>
<tr>
<td>ADC monitor</td>
<td>0.7 V 32 KHz Active</td>
<td>0.7 V 32 KHz Active</td>
<td>0.9 V 32 MHz Active</td>
<td>0.9 V Retention</td>
<td>0.9 V 4 MHz Active</td>
</tr>
<tr>
<td>Sleep</td>
<td>0.7 V 32 KHz Active</td>
<td>0.7 V 32 KHz Active</td>
<td>0.9 V Retention</td>
<td>0.9 V Retention</td>
<td>0.9 V Retention</td>
</tr>
<tr>
<td>OFF</td>
<td>0.7 V 32 KHz Active</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

#### Mode transition sequences

- **Boot-up sequence**: 
  - Island #1 (1V, 1MHz, Active) -> Island #2 (1V, 1MHz, Active) -> Island #3 (1V, 1MHz, Active) -> Island #4 (1V, 1MHz, Active)
- **Active -> Sleep**: 
  - Island #1 (1V, 1MHz, Active) -> Island #2 (0.9 V, 1MHz, Retention) -> Island #3 (0.9 V, 1MHz, Retention) -> Island #4 (0.9 V, 1MHz, Retention)
- **Sleep -> ADC Monitor**: 
  - Island #1 (0.9 V, 1MHz, Retention) -> Island #2 (0.9 V, 1MHz, Retention) -> Island #3 (0.9 V, 1MHz, Retention) -> Island #4 (0.9 V, 1MHz, Retention)
- **ADC Monitor -> QMA**: 
  - Island #1 (0.9 V, 1MHz, Retention) -> Island #2 (0.9 V, 1MHz, Retention) -> Island #3 (0.9 V, 1MHz, Retention) -> Island #4 (0.9 V, 1MHz, Retention)

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**Maestro core**
- Sits in the AON domain

**Core controller**
- Handles register programming, power-up sequence and mode change sequences

**Event handler**
- Manages events to execute mode change sequence automatically

**Resource controller**
- Arbitration of island controller requests
- Voltage settings, voltage regulator modes, clocks

**Island controller**
- Split between AON and switchable domains
- Power domain states, isolation cells, in-rush current setting, wake-up time
- Request to resource controllers and power switch controller
# Power Management IPs Highlights

## Embedded Power Management Unit

**MAESTRO**

- **Configurability**
- **Resource conflict management**
- **Boot-up sequence management**
- **Mode transition sequence management**
- **Native DVFS support**

## Power Regulation Network

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Our offering targets **low frequency oscillators** to optimize the power consumption of the Always-on domain.

**Low frequency oscillators**
- Count the time during sleep modes
- < 32 kHz
- In AON domain

**High frequency oscillators**:
- > 1 MHz
- For a use in active mode
## OUR OSCILLATORS FOR ALWAYS-ON DOMAIN

<table>
<thead>
<tr>
<th>Oscillators</th>
<th>RC</th>
<th>XTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>32 kHz</td>
<td>32.768 kHz</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>0.49 – 1.21 V</td>
<td>0.49 – 1.21 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>~ 70 nA</td>
<td>~ 50 nA</td>
</tr>
<tr>
<td>BoM Cost</td>
<td>No external component</td>
<td>External quartz needed</td>
</tr>
<tr>
<td>Accuracy</td>
<td>Lower accuracy and stability +/- 5 % after trimming</td>
<td>Very precise and stable over a wide temperature range +/- 0.05 % without capacitor Could reach +/- 0.005 % with external capacitors</td>
</tr>
<tr>
<td>Start-up Time</td>
<td>Fast startup time ~200 µs</td>
<td>Longer start-up time ~400 ms</td>
</tr>
<tr>
<td>Frequency</td>
<td>programmable</td>
<td>Not programmable</td>
</tr>
<tr>
<td>Silicon area</td>
<td>~ 0.040 mm²</td>
<td>~ 0.042 mm²</td>
</tr>
<tr>
<td>Target Applications</td>
<td>Frequent awakenings</td>
<td>High accuracy</td>
</tr>
</tbody>
</table>

*Note: Performances data for 40 nm and 55 nm*
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MAESTRO

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Power Regulation Network
DELTA

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Energy efficiency challenges

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Example on NB-IoT
**NB-IoT Application Requirements**

**Battery**

- **VBAT 2.7 - 5.5V**

**Activity Scenarios**

- RF transmit mode: 3 s/day
- RF receive mode: 12 s/day
- Compute mode (RF off): 30 s/day
- Deep sleep mode: Rest of the day (99.99%)
- **Battery autonomy:** 10 years

**Power island load specifications**

- **AVDD 1V8**
  - 150mA TX, 20mA RX

- **DVDD 1V1**
  - 35mA

- **DVDD-AON 0V9**
  - 0.5uA

- **DVDD 1V1**
  - 15mA

- **VDDIO 1V8**
  - 1.5mA

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NB-IoT Architecture #1

Battery: 2.7 V – 5.5 V

- OPM
- uLDO
- Buck DC-DC + uLDO
- LDO
- Buck DC-DC
- LDO + uLDO

Always-On Domain
MCU & RAM
RF Digital Part
Flash Memory
RF Analog Part
IOs
SIM

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NB-IoT Architecture #2: Optimization with Power Architect

**BATTERY**
2.7 V – 5.5 V

- **OPM**
  - **OPM-Angel-AR**

- **Buck DC-DC + uLDO**
  - **RAR-eSR-qLR**

- **Always-On Domain**
  - **MCU & RAM**
  - **RF Digital Part**

- **Flash Memory**

- **RF Analog Part**

- **IOs**

- **SIM**

- **Dolphin Integration IPs**
## Architecture Selection with Power Architect

### Table 1: Relative Contribution of Each Mode Based on Activity Cycle

<table>
<thead>
<tr>
<th>Mode</th>
<th>RF Transmit</th>
<th>RF Receipt</th>
<th>Standby Mode</th>
<th>Processing Mode</th>
<th>RF Tx</th>
<th>RF Rx</th>
<th>Standby Mode</th>
<th>Processing Mode</th>
<th>BoM Count (weighted)</th>
<th>BoM (mm²)</th>
<th>Area of VR</th>
<th>FoM</th>
<th>FoM, Normalized</th>
<th>Lifetime @ 1000 mAh</th>
<th>Battery Size Needed for 10-Year Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synopsis 1</td>
<td>12.09E-6</td>
<td>88.75E-3</td>
<td>33.69E-3</td>
<td>2.24E-3</td>
<td>6.02E-3</td>
<td>25.5%</td>
<td>38.7%</td>
<td>18.5%</td>
<td>17.3%</td>
<td>30</td>
<td>2.962</td>
<td>1.000</td>
<td>1.124</td>
<td>9.441</td>
<td>1.059</td>
</tr>
<tr>
<td>Synopsis 2</td>
<td>11.46E-6</td>
<td>113.69E-3</td>
<td>26.69E-3</td>
<td>2.08E-3</td>
<td>4.97E-3</td>
<td>34.4%</td>
<td>32.3%</td>
<td>18.1%</td>
<td>15.1%</td>
<td>26</td>
<td>2.258</td>
<td>0.889</td>
<td>1.000</td>
<td>9.960</td>
<td>1.004</td>
</tr>
</tbody>
</table>

### Summary

- Silicon Area is reduced by ~ 25%
- BoM is reduced by ~ 15%
- Without degrading battery lifetime

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Energy-efficient SoCs are mandatory to reach the IoT market requirements in terms of battery autonomy.

Dolphin provides a comprehensive Power Management IPs platform to speed-up the design of energy-efficient SoCs:

- Consistent, modular, standardized Power Management IPs Portfolio
- Customer configurable ePMU for easy and safe control of the SoC power modes
- Design Tools for quickly exploring and deciding on the most optimal on-chip Power Regulation Network
Thank you