The Lifeblood of SoC Design Today

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Agenda

- Market Dynamics
- Silvaco IP Overview
- IP Cores
  - Peripheral Controllers
  - Automotive IP
  - Foundation IP
- IP Subsystems
- IP Services
- IP Management
- Summary
• Market Dynamics
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Advent of AI and Multi-cores: IP Proliferation and Reuse

Apple A12 Bionic chip APL1W81 in iPhone XS
- Die Size 9.89 mm X 8.42 mm= 83.27 mm²
- TSMC 7nm – 6.9 B transistors
- 5% smaller ;15% faster , 40% more efficient than A11
- Micron MT53D512M64D4SB-046 XT:
  - E 4GB Mobile LPDDR4x SDRAM
  - ISP for camera
  - Apple GPU (4X)
  - NPU – Neural Engine Quin-5 Tr Ops/s
  - A12 is $72 of $453 total BOM cost

Samsung Galaxy S9+ SM-G965F/DS Costs* (Source: Tech Insights)
- Teardown Date: March-2018
- Applications/Baseband Processor $68.00
- Battery $5.50
- Camera / Image $48.00
- Connectivity $12.00
- Display / Touchscreen $72.50
- Memory: Non-Volatile $12.00
- Memory: Volatile $39.00
- Non-Electronics $29.00
- Other $15.00
- Power Management / Audio $8.50
- RF Component $23.50
- Sensor $5.00
- Substrates $19.50
- Supporting Materials $9.00
- Final Assembly & Test $12.50
- Total $379.00

(Source: Tech Insights)
Demand for Semiconductor IP

Source: Semico Research Corp. June 2018

IP use in Multicore SoCs

*Forecast

IP Categories

- Microprocessors (CPU/GPU/DSP)
- Communication IP
- Interface IP
- Memory & Memory Interfaces
- Fabric
- Peripheral Interconnect Controllers
- Power Management
- Analog IP (ADCs, PLLs)
- Foundation IP (std cells, SRAMs, I/O)

SoC Design Complexity and Time to market Require Use and Reuse of 3rd Party IP
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Silvaco IP Overview

- **IP-related Services**
  - Services around Silvaco IP including turnkey subsystems including embedded software

- **IP Management**
  - Enterprise grade platform for managing internal IP and 3rd-party IP compliance with patent-pending fingerprinting technology

- **Processor Subsystems**
  - Processor agnostic hardware/software subsystems including common peripherals, bus fabrics, and embedded software

- **IP Cores**
  - More than 100 production proven Verilog and VHDL IP cores
    - Foundation IP

- **IP Commercialization**
  - Collaboration with Tier 1 semiconductor companies
    - Silicon Proven IP in volume production
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Standard Functions and Interface Controllers

Motor Control
- GPIO
- PWM
- Timer/Counter

Computer-Computer Communication
- LCD Controller
- USB
- USART

Memory Interfaces
- SPI
- Octal SPI
- Quad SPI
- Parallel Flash
- SmartCard
- SRAM/ROM

Sensor Interfaces
- I3C
- I2C
- I2S

Audio Interfaces
- AES
- DES
- RTC
- USB
- UART

AHB Multi-layer Fabric
- 8 masters / 12 slaves
- Instruction SRAM
- APB Bridge
- User AHB Slaves
- Power Management Unit
- Internal Mem Ctrl
- CPU Cortex M3
- APB Channel
- Digital Subsystem
- OTP ROM
- Internal Mem Ctrl
- WatchDog Timer
- Timers
- GPIO
- User APB Slaves
- D Master
- M Masters
- Master
- User AHB Masters
- Slave
- Serial Flash Controller Slave
- Slave
- Slave
- Slave
- Slave
- I Master
- Data SRAM
- Internal Mem Ctrl Slave
- Directive Memory Access Controllers
- Timer/Counter
- AHB Performance Subsystem
- AES
- DES
- RTC
- LCD Controller
Automotive Networking Portfolio

Automotive Network Backbone

Gateway 1 (Powertrain)
- Engine
- Transmission
FlexRay / CAN-FD

Gateway 2 (Body/Comfort)
- Door Locks
- Climate
- Seatbelts
- Sunroof
LIN / CAN

Gateway 3 (Chassis)
- Steer-by-Wire
- Brake-by-Wire
- Safety
FlexRay

Capability
- Distributed timebase: Lin No, CAN No, CAN-FD No, FlexRay Yes
- Speed: Lin 115Kbps, CAN 1 Mbps, CAN-FD 12 Mbps, FlexRay 10 Mbps
- Channels: Lin Single, CAN Single, CAN-FD Single, FlexRay Dual
- Arbitration: Lin CSMA, CAN CSMA, CAN-FD CSMA, FlexRay TDMA

Silvaco Products
- LinFlex
- FullCAN
- MultiCAN
- FlexCAN
- FlexRay
Foundation IP

• **Foundry Sponsored**
  - Global Foundries 55LPx, ULP, 28nm SLP/ULP

• **Foundry Libraries**
  - Several foundries offer Silvaco libraries under their own name.

• **Library Services**
  - Custom Library development or Optimize your existing library
    - Core, ECO, Power Management and Retention libraries
    - Area, Speed or power optimized libraries.
    - Internal fab, special process.
  - High voltage libraries
  - Near Threshold libraries
Leverage existing silicon proven standard cell library IP

Extend and develop new IP using Cello™ migration and optimization

Foundry Process

Library Variants, DFM, Automotive, IoT, etc.

Multiple Track Heights

Ultra Low Power, High Density & High Performance Options

Custom Libraries

Design & Application Specific

Add-on cells GPU/DSP/CPU

Available libraries ready to use
(130nm/55nm/40nm/28nm GF, TSMC, SMIC)
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Arm-based Processor Subsystems

• Standard Products
  • AHB Low Power
  • AHB Performance
  • AXI High Performance
  • I3C Sensor
  • IoT Edge

• Include fabric + common peripherals + power mgmt.

• Customization available
### AXI Performance Subsystem

**Target Applications**
- Gateway / Routers
- Automotive
- IoT
- Wireless
- Medical Instrumentation
- Instrumentation / Display
- Home / Office
- Surveillance / Monitoring
- Automation Controllers
- Industrial Controllers
- System Controllers
- System Analysis
- Avionics
- Displays
- Communication

**Features**
- High Performance
- Linux Support
- RTOS / Kernel Support
- AMBA AXI4 Fabric
- AMBA APB 3.0
- Standard APB Peripherals
- Serial Flash Controller
- DMA
- AXI - AHBLite Bridge (optional)

### I3C Sensor Subsystem

**Target Applications**
- IoT Edge Devices
- Small Controllers
- **Smart Sensors**
- Smart Lighting
- I3C Connected Devices

**Features**
- Low Power
- RTOS / Kernel Support
- AMBA AHB 2.0
- AMBA APB 3.0
- MIPI I3C Connectivity

**IP Cores**
- Power Management Unit
- Internal SRAM Controller
- Watchdog Timer
- Timer(s)
- GPIO
- SPI Master/Slave
- UART
- **I3C Master**
- **I3C Slave (APB)**

**Software**
- Boot Code
- Basic Kernel
- HAL / Drivers
- SPI
- **I3C / I2C**
- GPIO
Processor Independence
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SoC Design Services

**SOC Architectural Services**
- System architecture design
- Chip interconnect, datapath, performance analysis

**SOC Design**
- RTL design and behavioral modeling
- Custom SOC development (Verilog or VHDL)
- C, C++ embedded software development

**System level verification and prototyping**
- Test environments using Bus Functional Models (BFMs)
- System Verilog, UVM

**Emulation and prototyping**
- FPGA prototyping / development and emulation
- C test software
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Leveraging Your Company’s IP Assets

**Accounts**
- Sites
- Users
- Privileges
- Access

**Products**
- Suppliers
- Catalog
- Releases
- Errata
- Collateral

**Contracts**
- Terms
- Use rights
- Restrictions
- Maintenance
- Support
- Warranty
- Milestone Payments

**Devices**
- Releases
- Milestones
- Foundry
- Process

**Support**
- Tickets
- Bug-reporting
- Effort tracking
- File sharing
- Bulletins
- Notifications

**Compliance**
- Fingerprinting
- DNA Analysis
- Reporting

**Reporting**
- Charts
- Queries
- Tracking
IP Compliance Through Fingerprinting

IP Database

Design Files

Fingerprint Program

IP Fingerprint File

DNA Analyzer

Chip Database

Design Files

Fingerprint Program

Chip Fingerprint File

DNA Report
High level summary includes:
- IP title detected, versions detected, provider
- Score representing confidence level
- Whether GDSII tags were detected
- List of files with no matching fingerprints
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• Time to Market is exponentially faster with Silicon Proven IP and Reuse
• Silvaco brings a vast set of technology and expertise to your company
• Silicon proven IP cores applicable to almost any design
• Hardware/Software expertise in building complex SoC designs
• Enterprise-level IP management software for organizing your assets
THANK YOU!