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Thalia Design Automation

Analog IP Reuse & Process Migration:
Challenges & An Innovative Methodology to Address Them
December, 2018





Analog IP Reuse – Why is it difficult ?

- Analog circuit design is impacted by a number of factors
 - Device performance,
 - Technology characteristics,
 - Functional requirements,
 - Inefficient design methodology
- Migrating an Analog circuit into a new technology is almost a redesign of an existing IP – custom requirements
 - Even a bandgap requires design redo !!!
- Limited solutions in the market and a shortage of analog designers exacerbates the problem
- Is efficient Analog IP reuse a dream?



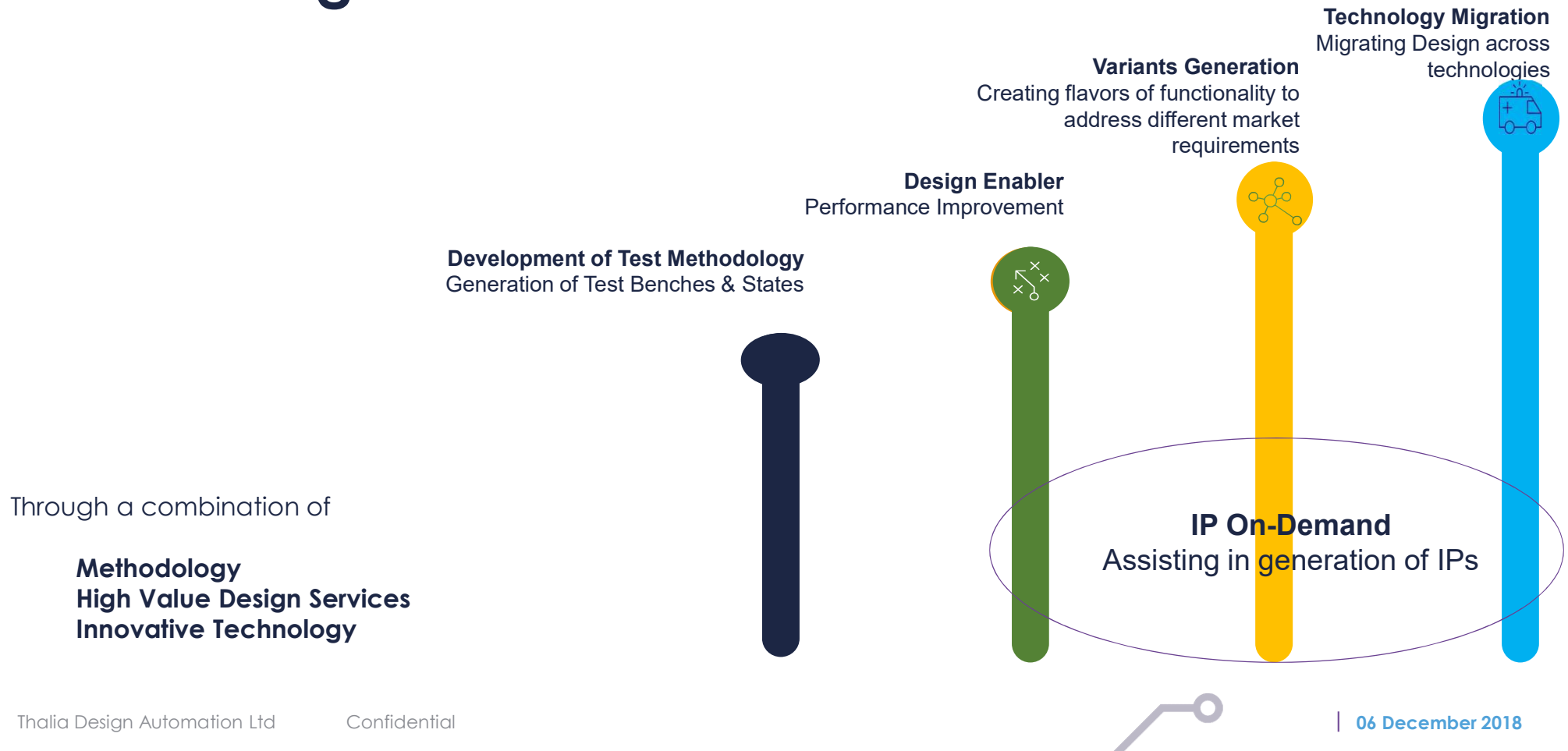


Thalia at a glance



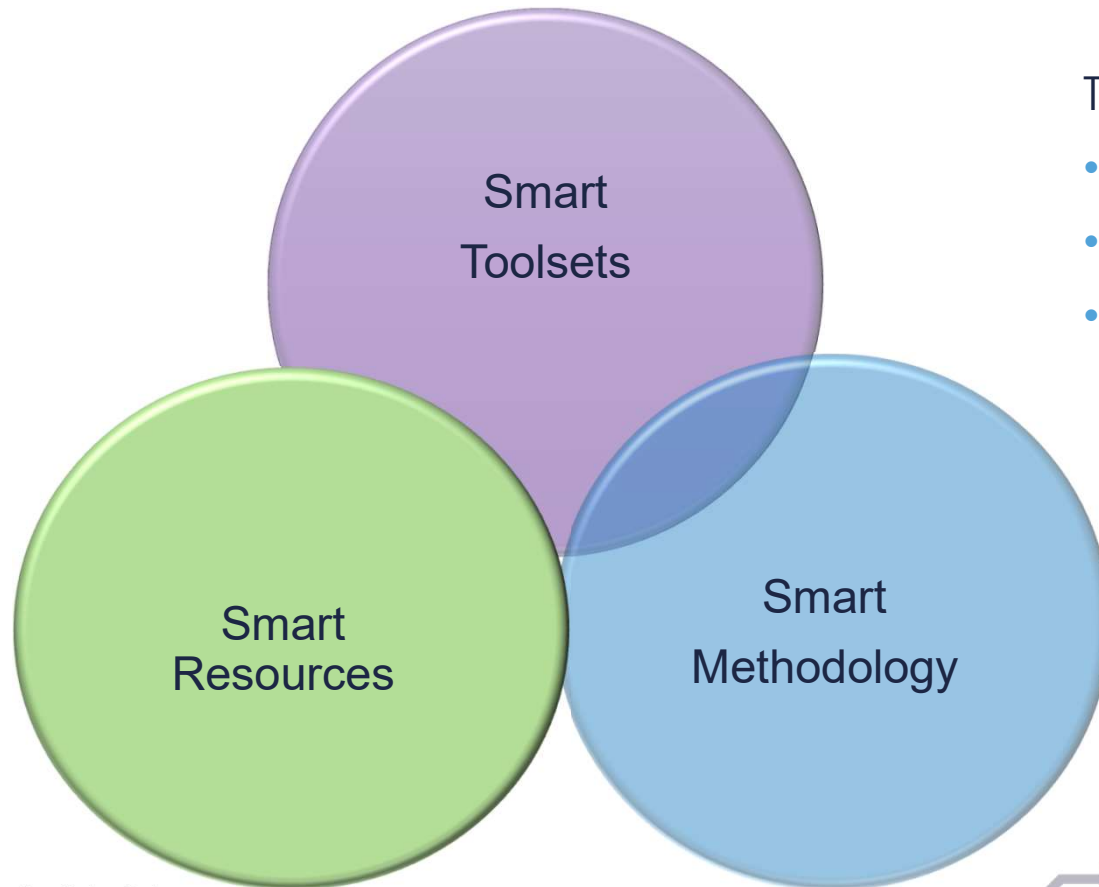


Thalia's target solutions





Why are we different?



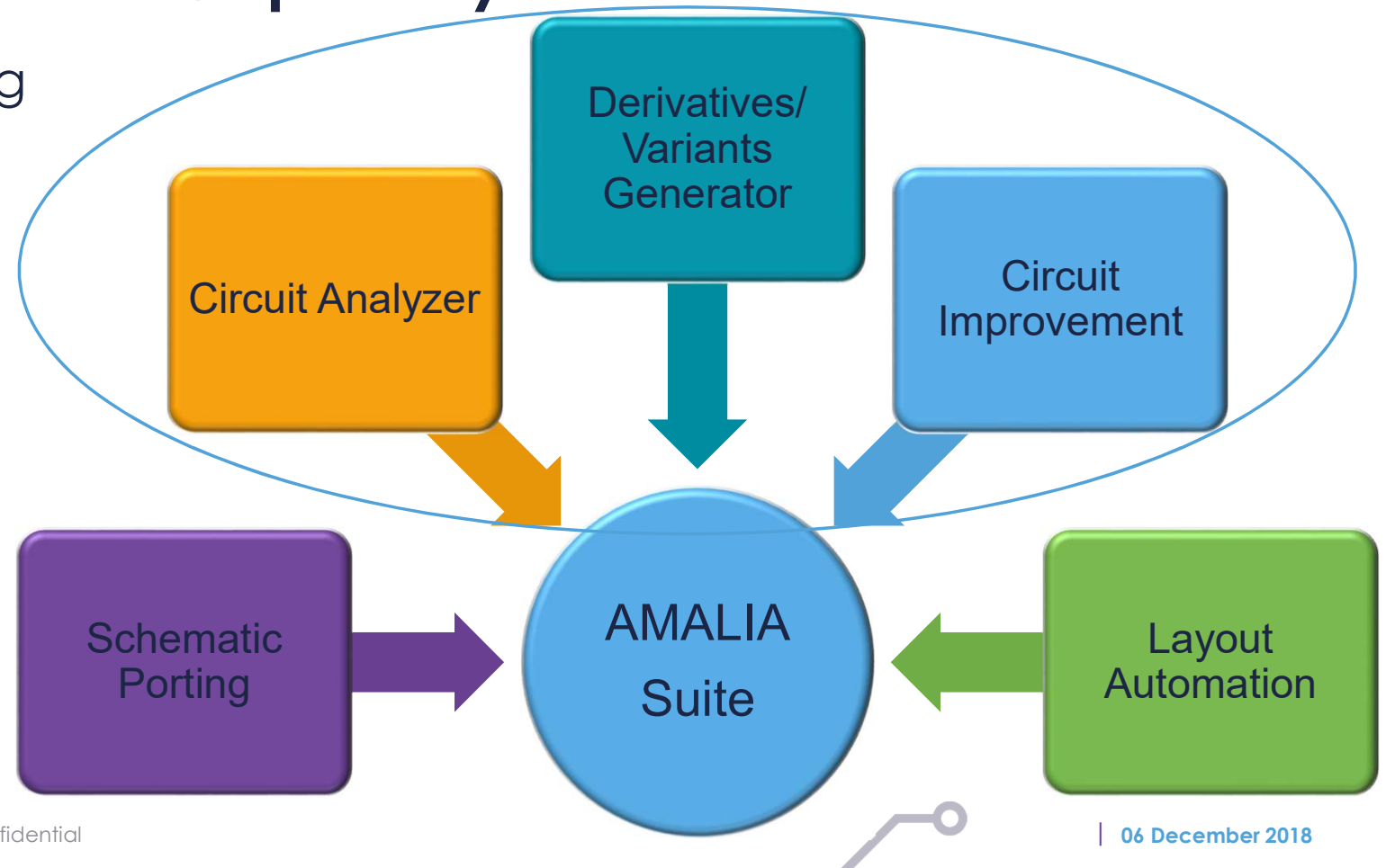
Thalia unique approach

- Speed
- Efficiency
- Cost

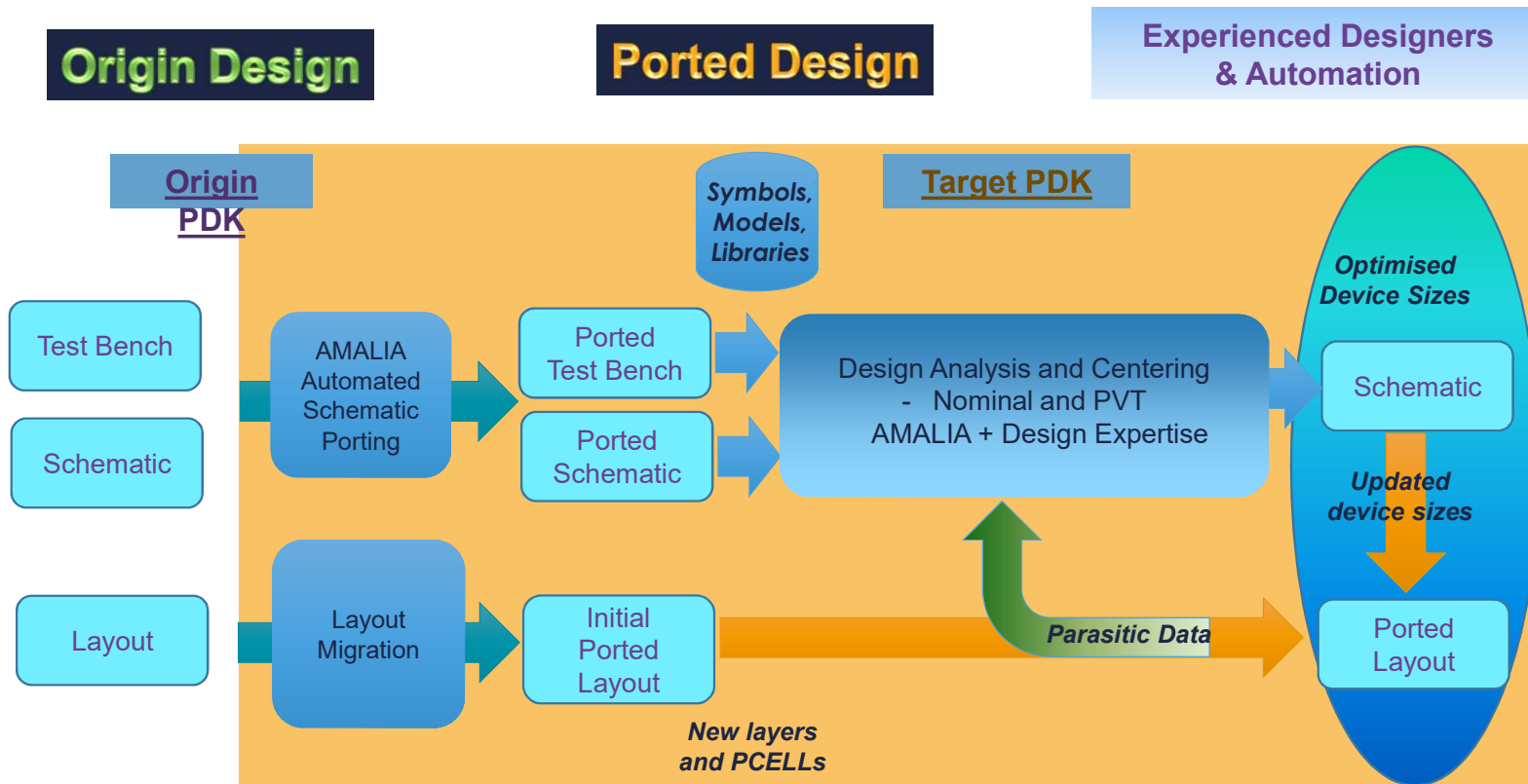


Toolsets Amalia™ Capability

- Design enabling

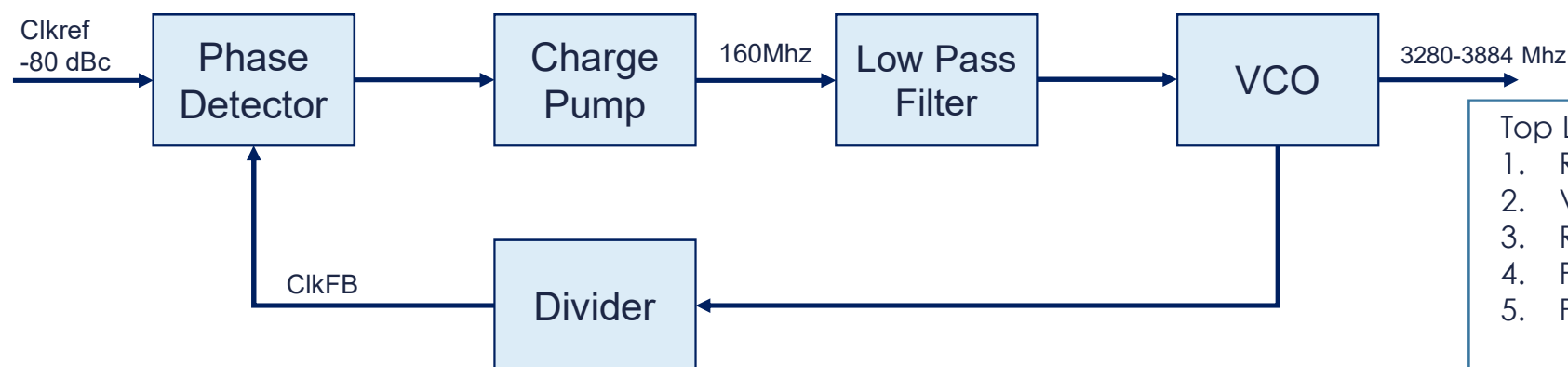


Thalia's Analog Porting Flow





Design Example – PLL Application in Wi-Fi Migration



- Top Level Specifications
1. Ref Frequency=40MHz
 2. VCO Out Freq=3.2G -4GHz
 3. Reference spur <-50dBc
 4. Programmable divider
 5. Power consumption: 3mA

Others: PD & MMD = -9dB => -12dB each
@160 MHz: -12 dB => -40-12-31 = -83dBc





Design Example: Clk PLL

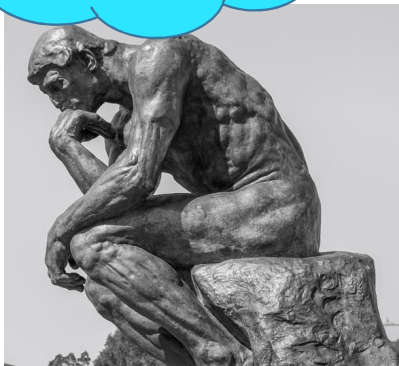
VCO(LC based)		Programmable Feedback divider	
Centre frequency	3.86GHz	Operat freque	6.4GHz
Current consumption	1.5mA	Current consumption	1.0mA
Tuning range with band selection	3GHz-4GH	Output swing	Rail to
Phase noise	-120dBc/Hz @1MHz offset	Charge Pump	
		Full differential design with 3bits programmability	40uA-200uA

Schedule

Loop stability,
Parasitics etc

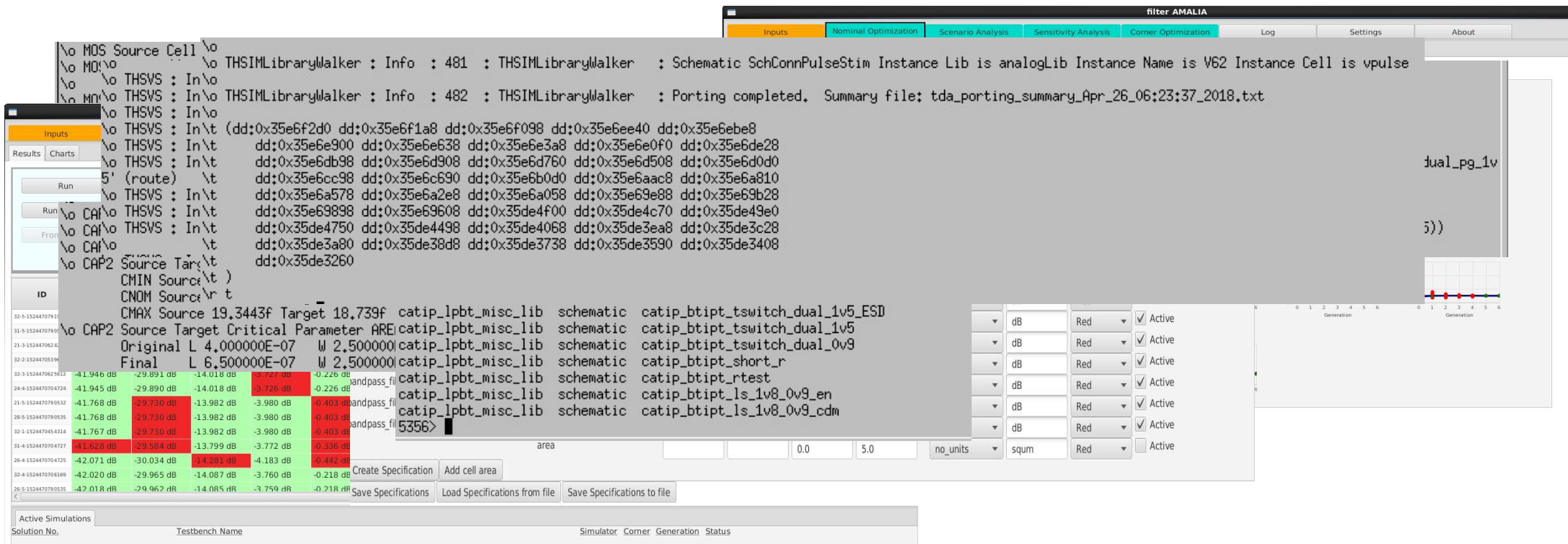
Topology

Technology Differences

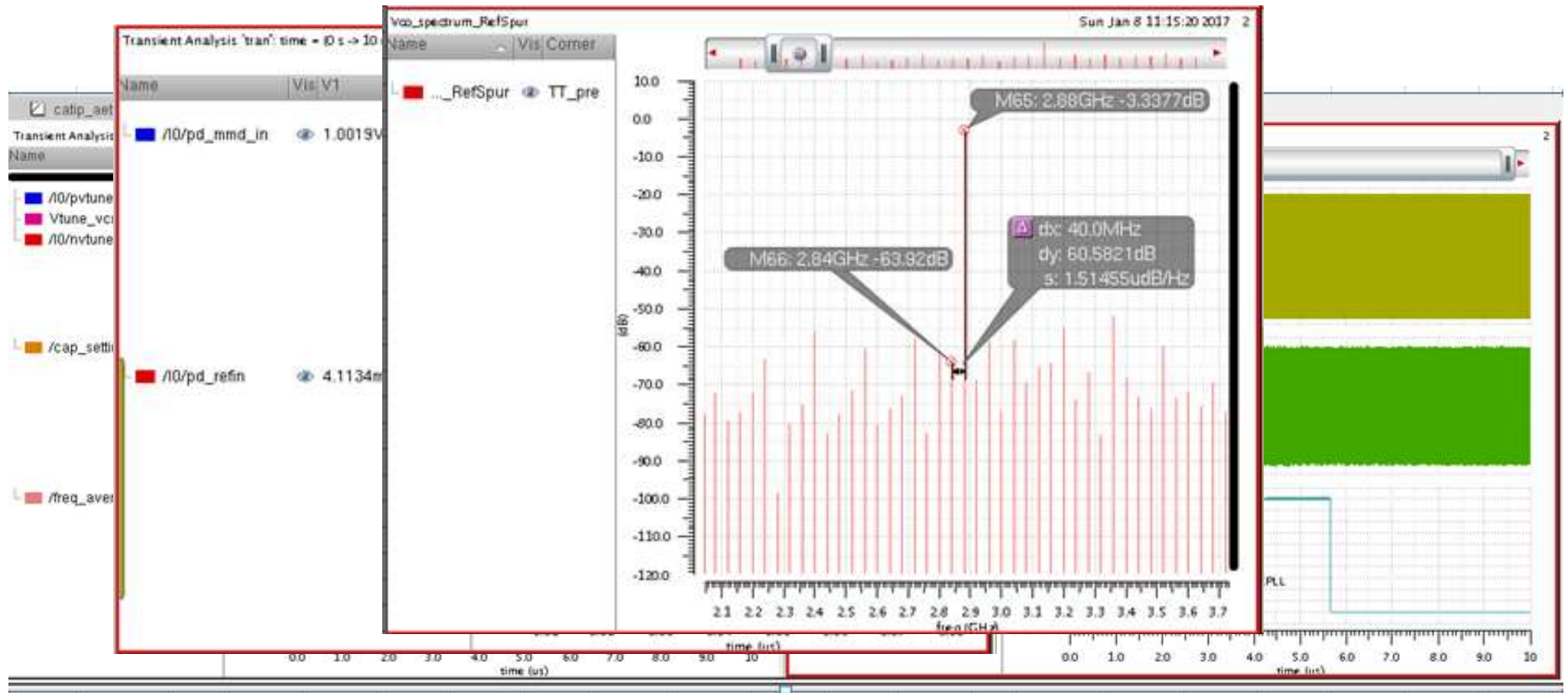


Design Example: Clk PLL – Thalia's Solution

- Targeted automation to provide incremental time and cost savings – full automation doesn't work in Analog



Design Example: CLK PLL – Migration Results





Business Value: Analog Migration

Design	Parameter	Conditions	Verified Specification			Min	Typ	Max	Units
			min	nom	max				
CLK-PLL	Functional requirements								
	PLL comparison frequency	Same as the XO frequency		40			40		MHz
	Output frequencies to the LB and HB PLL's (low noise)			160			160		MHz
	Other output frequencies	To frequency counter		40			40		MHz
				960			960		MHz
		Test-output		40			40		MHz
		To ADC/DAC		160			160		MHz
	Parametric requirements								
	EVM from Integrated phase noise at the 160MHz output	Integrated from 10kHz to 2MHz and referred to 5.9GHz	?	-42.9			-43.6		dB

- Ref Frequency=40MHz
- Clock output : 2.88GHz
- VCO phase noise =-121dBc/Hz @1MHZ.
- Programmable loop filter AND Programmable divider.
- EVM for Integrated PHASE NOISE @160MHZ should be better than -42dB.
- Ref spur =-90dB
- TSMC to GF 28nm
- Migrated, Design changes and layout in < 6-7 weeks





Rapid Analog Porting - Reuse Customer Examples

Classification	Examples	Redesign Cycle Time*	Thalia's Cycle Time*
Standard Analog IP	DAC, ADC, PLL	12-16 weeks [2-3 FTE]**	4-8 weeks [2 FTE]**
Complex Analog IP	PHY (E, MIPI-D, HDMI, USB, PCI)	40-50 weeks [4-5 FTE]**	16-20 weeks [4 FTE]**
Application Analog IP	Bluetooth	>40-50 weeks [4-6 FTE]**	16-24 weeks [4-5 FTE]**
Application Analog IP	Dual Band WLAN	>50 weeks [4-6 FTE]**	20-28 weeks [4-5 FTE]**

(*) Elapsed calendar time to Specification Compliant Design

(**) FTE : Full Time Equivalent

Timescales will be impacted by Circuit complexity and process node differences





Customer Testimonial

Kave Kianush, Catena Vice President and Chief Technology Officer

- “We’re taking a new approach, which represents a fundamental shift in the way analog IP is created and delivered.
 - Our relationship with Thalia helps us to deliver exactly the right feature and performance combination for our customers, against ever more demanding time-to-market and cost requirements.
 - Thalia’s combination of novel design automation technology and analog design expertise is unique in the market.
 - We’ve already seen a positive impact on our ability to deliver against tight customer deadlines.”
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- <https://www.thalia-da.com/catena-selects-thalia-da-to-facilitate-analog-ip-re-use/>





Solutions delivered by Thalia

Unique combination of Experienced Resources and Innovative Technologies

Application	Technologies
Dual Band WIFI	TSMC 28nm, 40nm, GF 28nm
Bluetooth IP	TSMC 28nm, 40nm, GF 28nm, Samsung 28nm
Home IoT Radio Applications	SMIC 40nm
SAR ADC, Baseband filters	GF 28nm, TSMC 40nm, GF 130, Tier 1 In-house Technologies
Low Power LNA, PA	SMIC 40nm, GF 28nm, TSMC 40nm
PMIC Derivatives, sub-blocks	UMC, TSMC, GF, AMS →28-350nm
PLLs	TSMC 28, 40nm, GF 28nm

Wide range of Technologies and nodes from 350nm down to 16FF

Proven Track Record delivering designs in cutting edge applications and in newest technologies





Summary: Re-inventing Analog Reuse

- Unique combination of toolsets, methodology and design experience
 - Proven track record – 16FF to 350nm; TSMC, UMC, GF, Tower, SMIC, AMS, Tier 1 Technologies
 - Direct application in migrating IPs – Off the shelf IPs
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- Contact us sales@thalia-da.com

