Customizing Future Low Power IP Innovation

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When Power is Paramount
Overview

- Headquartered Sheffield (UK)
  - Design Centres Sheffield & Leuven
- World class SRAM development team
- Industry leading low power SRAM technology
- Technology scales to (at least) 7nm FinFET
- Patented and silicon proven
- Power is the #1 issue for many markets
- sureCore meets AI, ML, IoT, Wearables & Medical low power memory needs

New & Evolving Markets Demand Power Efficient IP
“With low voltage, the first limitation customers are aware of is the lack of SRAM IP” - Rainer Herberholz, Director Emerging Technology, ARM
– SRAM Characteristics - Power, Performance, Area
  – Traditional compilers “High Density” or “High Speed”
  – sureCore focus is “Low Power”
  – Implemented by powerful in-house compiler technology

– Disruptive Low Power Memory Architectures
  – Process-independent optimisation
  – Based on foundry bit cells & standard processes
  – Augmented by enhanced low power verification methodologies
  – Industry leading tooling delivers flexible characterization solution
Market Leading Products

- **“EverOn” Product Family**
  - Single port ultra wide operating voltage range SRAM
  - Silicon proven
  - $V_{nom}$ to near threshold operation (0.6V)
  - Available in 40ULP, 28HPC+, 22ULL

Near Threshold Operation is Unique in the Industry

- **“PowerMiser” Product Family**
  - Low Power, saves >50% dynamic power, >20% static power
  - Compared to foundry & leading industry providers
  - Demonstrated in 28FDSOI & 40nm Bulk CMOS
  - Available in 28FDSOI, 28HPC+, 22ULL

Offers Compelling Dynamic & Static Power Savings
Power Savings:
PowerMiser: 20% Standby, 55% Dynamic Power
EverOn: 60% Standby, 40% Shutdown, 60% Dynamic Power (@0.7V)
Challenge: Deliver Shrinking SoC Power Budgets

Off-The-Shelf SRAM IP Increasingly Misses The Target

It’s One More Headache For The System Architect
Challenges System Designers Face

• “We want to run at low voltage”

• “We need a multi-port RAM that runs at high speed, but with low power”

• “We want to put 10s of Mbytes on a chip, but the power looks prohibitive”

• “We need really low leakage”

All Real Problems With No Off-The-Shelf Solution
Multi-Port Example

- Full custom implementation
  - Tier-1 Comms Application
  - 16 FinFET Process

- Multi-port design
  - 1 Write Port, 8 Read Port
  - Double pumped

Key achievements
- >40% write power saving
- >60% read power saving
- Timing marginality >6sigma
- Achieved fmax >1GHz
- Met area budget
• ACSRAM – Custom Designed Memory Meets Your Requirements
  – Specifically tuned to application needs
  – Delivers optimal power profile & feature set

• Target Markets
  – Networking (down to 7nm)
  – Machine Learning/AI (Large memory subsystems – down to 7nm)
  – IoT/Medical/Wearable – Ultra Low Operating Voltage (Bulk/FDSOI)

• Engagement
  – System level review to understand feature set & power profile
  – SRAM specification preparation - agreed with customer
  – Compiler or Instance development
  – Test chip development & characterisation service
Summary

- **Industry Leading Ultra Low Power SRAM IP**
  - Dynamic power savings exceeding 50%
  - Near Threshold, Ultra Low voltage operation (down to 0.6V)
  - Silicon Proven
  - PowerMiser & EverOn standard products available NOW

- **Application Centric SRAM Development**
  - SRAM power is critical to your system power budget
  - You have a specific feature set allowing system level optimization
  - You need best-in-class static and dynamic power performance
  - You need low-voltage operation

**ACSRAM – Meet Tomorrows Power Targets Today**
Questions?

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