Embedded FPGA enabling 5G Infrastructure

Mike Fitton
Achronix Overview

- Achronix develops FPGA-based, data acceleration products for compute-intensive infrastructure applications:
  - Data Center - Compute, Networking and Storage
  - 5G Wireless Infrastructure
  - Wireline Networking
  - Automotive
- All Achronix products are supported by proven, comprehensive ACE design tools with >100 man-years of development
- Financials: $100M in 2018
  - Voted “Company of the Year” at UBM ACE Awards
- Executive management/engineering with extensive experience in the FPGA industry
- Office locations:
  - Development centers in US and India
  - Sales and technical support in US, Europe and China

Timeline:

- 2004
  - Achronix Founded
- 2010
  - First semiconductor company on Intel Custom Foundry
- 2012
  - Shipped ACE with support for Speedster22i FPGAs
- 2013
  - Shipped Speedster22i FPGAs
  - First company to ship FPGAs built with FinFET technology
- 2015
  - First Speedcore design win
  - Speedster22i moved into volume production
- 2016
  - Multiple Speedcore design wins
  - Began shipping PCIe acceleration board
- 2018
  - $100M in revenues
  - Large Speedcore pipeline
  - Plans to grow headcount by 30% - 50%
Achronix Builds Customer-Defined FPGA Products for High-Performance Applications

**Speedster**
- Standalone packaged FPGA devices
- Highest density
- Optimized for compute and network acceleration
- 22nm: shipping since 2013
- 7nm: in development

**Speedcore**
- Embedded (eFPGA) IP for integration in SoC
- Customized by customer
- High-performance
- Low-power
- 16nm: available today
- 7nm: in development

**Speedchip**
- FPGA Chiplets
- 2.5D or MCM integration
- Low-latency, USR interconnect
- High-performance and low-power
- 16nm: available today
- 7nm: in development

All Products Supported by Achronix ACE Design Tools
5G: what is it?

10x increase in throughput

~10x increase in data and devices by 2025

Wide variety of emerging applications

Source: ITU-R IMT-2020
5G challenges

~10x increase in data and devices by 2025
Necessitates portfolio scalability

10x increase in throughput
Needs high-throughput hardware data pipeline

Wide variety of emerging applications
Requires solution flexibility

Source: ITU-R IMT-2020

Enhanced Mobile Broadband
- Gigabytes in a second
- 3D Video, UHD Screens
- Work and Play in the Cloud
- Augmented Reality
- Industry Automation
- Mission critical application
- Self Driving Car

Future IMT

Massive machine type communications
Ultra-reliable and low latency communications
Aggressive 5G roadmap

- High throughput and low latency demands **hardware accelerated** solution
- Changing standards complicate **System-on-Chip** development lifecycle
- Emerging applications require **programmability** for flexibility/future-proofing

**Clear need for programmable, hardware accelerators tightly coupled to SoC**

Source: Electronic Design, “5G—It’s Not Here Yet, But Closer Than You Think”, October 31 2017
An Introduction to Embedded FPGA

eFPGA: Alternative to standalone FPGA

- High density, high-performance eFPGA integrated into SoC
  - Programmability for vendor and/or end-customer

- AXI/ACE-Lite Interfaces
  - Integrates like any other SOC IP core
  - High-throughput and low-latency
  - Enables Coherent Programmable Acceleration

- Extremely Customizable
  - Number of LUTs and FFs
  - Memory density and size
  - DSP block density and features
Any Granularity for All Functional Blocks

- Speedcore resources are designed as “building block” structures that can easily be combined to build any size Speedcore eFPGA
- Customer defines resource count for their Speedcore eFPGA
- The Speedcore IP and supporting files are delivered to the customer shortly after specification is completed

Examples of different Speedcore eFPGA Configurations

- LUT: 0 - 2M
- BRAM: 0 - 300 Mbits
- LRAM: 0 - 100 Mbits
- DSP64: 0 - 20K
- Custom: 0 - n
Applicability in 5G Digital Front End

- **Future-proofing Radio Digital Frontend**
  - Fine-grained programmability for addressing new algorithmic requirements, emerging standards and changing protocols

- **Algorithmic acceleration**
  - Address new Digital Predistortion (DPD) adaptation requirements
  - Migrating L1 functions from Baseband requires scalable/flexible solution

- **IO diversity**
  - Proliferation of wireless interface standards requires flexible solution

- **Scalable solution to address other markets, e.g.**
  - Cellular evolution for V2X, Ultra-Reliable Low Latency Connectivity and mMTC
  - Cable DOCSIS 3.1 and FDX
DFE Architecture: Baseline

- Standalone FPGA used for initial prototyping and early volume
- ASIC to reduce power/cost
  - Programmable filtering and/or vector signal processing for the uplink and downlink processing
- FPGA still used for variants and new requirements

Objective with eFPGA: reduce number of variants – address with common architecture
eFPGA for fronthaul

- IO diversity and news protocol support for BB-Radio interface
- Common logic for CPRI, eCPRI, IEEE1914, X-haul, etc
  - JESD204B/C for M-MIMO
- Negligible die area
DFE Architecture: Scenario 2 (Acceleration)

eFPGA for algorithmic flexibility

- Speedcore for future-proofing algorithms and flexibility
- eCPRI Split 7 requirements
  - PRACH Random Access
  - FFT for mMTC waveform
- DPD adaptation logic
  - New waveform, traffic or amplifier requirements
- Can also include Scenario 1
eFPGA for spec expansion

- Replace or augment baseline functionality
  - Extract/sum before/after each function

- New market support
  - More carriers
  - New waveform, e.g. for mMTC

- High bandwidth interconnect by Speedcore
  - ~500Gbps I/O required for 100MHz 4x4
eFPGA for spec expansion and IO flexibility

- Single or multiple Speedcore regions
- Loose or tight integration with hardened functions
  - Adjacent processing or
  - Custom columns in Speedcore (e.g. integrated VSP)
Future-proofing 5G Baseband

- **Accelerating Physical Layer and Layer 2/3**
  - Algorithmic acceleration
    - E.g. FEC, ROHC, Ciphering
  - Packet processing and Traffic Management
  - Edge Analytics and Mobile Edge Computing
    - Machine Learning Inferencing and Edge Training

- **Accelerating Time-to-Market**
  - Address emerging requirements with eFPGA instead of delaying ASIC Tapeout
    - especially for Rel16 (URLLC and mMTC)
eFPGA addresses the challenges of 5G

- 5G creates unique challenges of high throughput and rapidly changing requirements
  - Many more devices and a plethora of usage models require flexibility

- Cost and power are likely to drive the need for cost-optimized system-on-chip solutions rather than general purpose silicon
  - Need to retain as much programmability as possible, to ensure future-proofing of SoC

- Here we propose a heterogeneous multi-core solution comprising CPU, hard accelerators and Embedded FPGA
  - Optimal mapping of processing increases throughput/reduces power
  - Reduce cost and size compared to discrete devices
  - Quantifiable improvement in time-to-market
Thank you!