Efficient Design Of Multi-Format Video Decoders

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Agenda

- The Increasing Challenge Of Video Decoding
- Video Decoder Implementation Options
- Hardware Technology Comparison
- Top-Level Video Decoder Design Considerations
- System Level Challenges
- Designing A Robust Decoder
- Verification Methodology
- Summary

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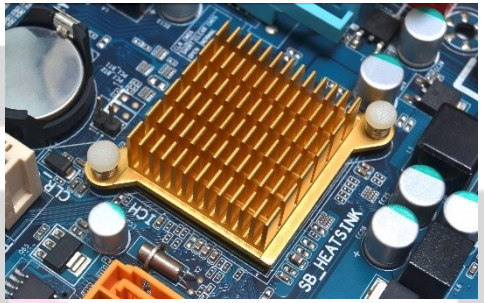
The Increasing Challenge Of Video Decoding

Video traffic and applications are becoming pervasive

Video resolutions and frame rates are quickly increasing – UHD is 480Mpixels/sec



Silicon area and power consumption are key cost factors

Time to market pressures push SoC companies to license IP

Cannot afford to miss market window – no re-spins, must trust IP supplier

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Video Decoder Implementation Options

- Fully SW-based decoder running on fast multi-core processors
  - Highly flexible and portable
  - Need very large, power hungry processors
- Fully HW-based implementation running in dedicated HW
  - Lowest cost, lowest power
  - Completely inflexible
- A spectrum of mixed HW/SW architectures in between
  - Optimum point on spectrum driven by many variables
    - Target technology
    - Achievable clock rate
    - Formats to be supported
    - Resolution and frame rate

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Hardware Technology Comparison

- FPGA implementation
  - Clock rate of around 200MHz achievable
  - Many on-chip memory & DSP resources available
  - Hardware bug not normally catastrophic
    - Generally fixable with an HDL change
- SoC implementation
  - Clock rate potentially >600MHz
    - More cycles to utilize and more opportunity for logic re-use
  - Hardware bug potentially catastrophic
    - SoC re-spin can incur huge time and cost penalties

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Top-Level Video Decoder Design Considerations

- Power & silicon area always important
  - Not just in mobile and low cost applications e.g. VR headsets
  - Packaging and cooling costs significant in all SoCs
- Silicon area grows as a result of increased flexibility in the solution
  - Multi-format
  - Multi-stream
  - Image resolution
  - Frame rate
- Sample applications
  - VR headset
    - Closed system allows more flexibility
    - Ultra low latency required
    - Ultra low power required
  - Set top box
    - Multi-format and multi-stream needed
    - High, mid a

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System Level Challenges

- Decoding video bitstream alone is not enough
  - Decoder design needs to consider real use cases
- Use case examples
  - Multi-stream decoding with single decoder
    - Need to context switch between streams
      - Need ability to save lots of context
      - Need ability to switch frame store management settings
  - Dynamic resolution change handling
  - Low power modes
    - Disable blocks when not needed
    - Completely power down decoder when idle
  - Handle seek, fast forward & fast rewind operation
    - Smooth fast forward needs faster than real-time decode
- All of these require software level control of the decoder

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Designing A Robust Decoder

- Robust to system integration differences
  - E.g. Memory system latencies
- Robust to corrupted streams
  - Cannot hang under any circumstances
  - Needs to have good error concealment
- Robust to non-compliant streams
  - Spec/standards ambiguities for example
- Decoder architecture can help with robustness and flexibility
  - Dedicated HW for area/power reasons
  - SW control to be able to handle these aspects
- These things must all be covered in the verification methodology
- Robust decoder comes from years of experience of practical deployments

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Verification Methodology

- Simulation only methodology is not an option for video codec verification
  - FPGA prototyping or emulation is necessary
- Needs an automated regression system
  - In case of multi-format decoder, complexity scales
    - Each format requires testing with thousands of streams
    - Each stream contains hundreds of frames
    - Test set can become huge
- Range of test data
  - Standards compliance, commercial stress streams, corrupt streams, known issue streams

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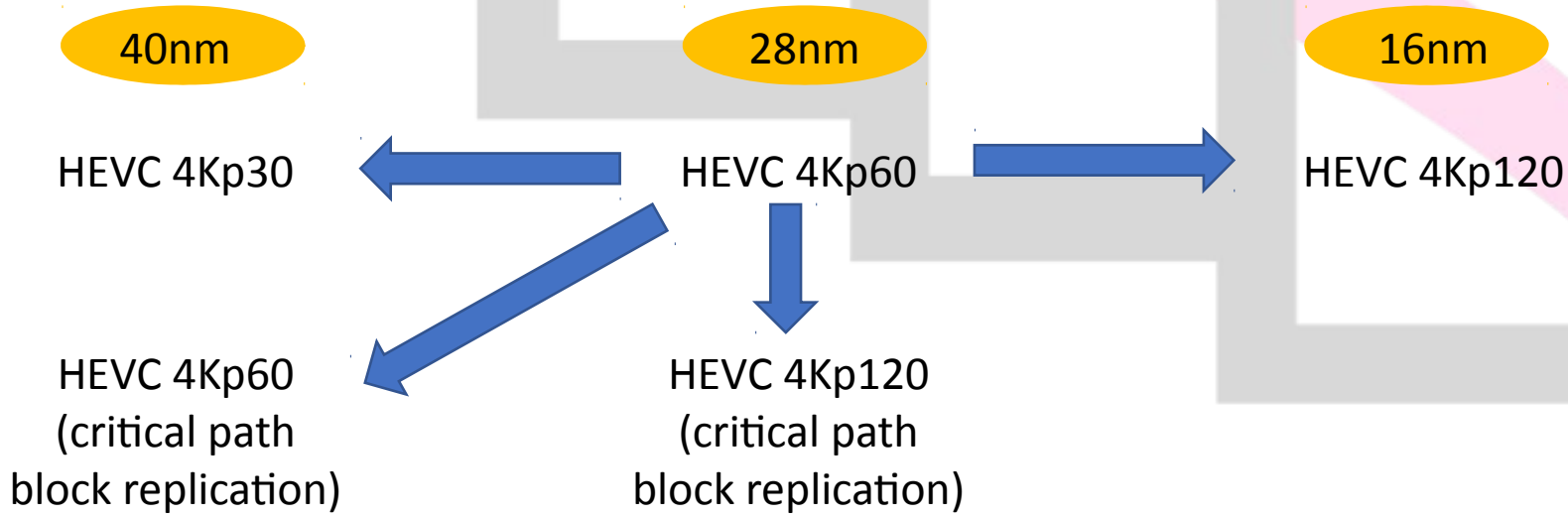
Example: CS8141 ‘Malone’ Video Decoder

- Consideration given for TSMC 28nm process due to target of many end customers
- Tradeoffs can be made to determine best process fit
  - Cost analysis
  - Factor in other IP in the system



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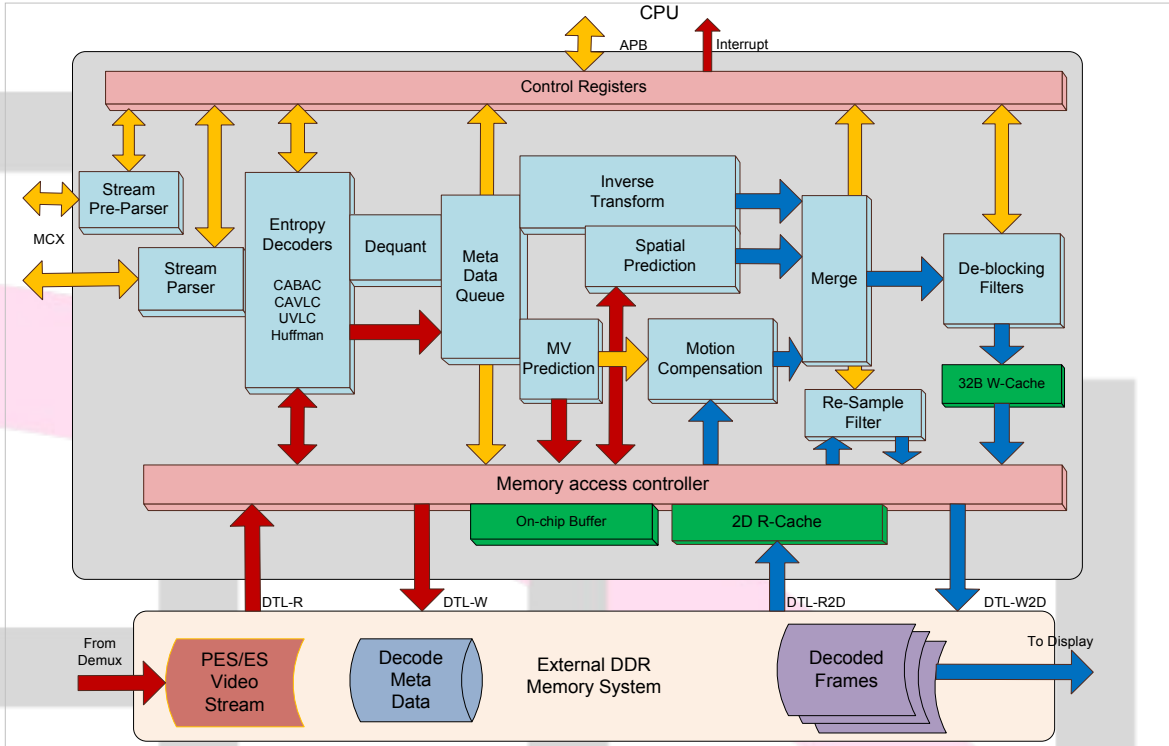
Example: CS8141 ‘Malone’ Video Decoder

- Multi-format, multi-stream video decoder
- Supported formats
  - VP9 Profile 0, 2 @L5.1
  - H.265 HEVC MP@L5.1
  - H.264 AVC/MVC BP/MP/HP @L4.2
  - VC-1 SP/MP/AP
  - MPEG-2 MP/HL
  - MPEG-4.2 SP/ASP
  - H.263 / Sorenson Spark
  - DivX 3.11 + GMC
  - China AVS-1 up to L6.1, AVS+
  - Real Media RV8/RV9/RV10
  - ON2 / Google VP6 / VP8
  - BL JPEG / MJPEG
- Technology is silicon proven in SoCs down to 16nm



- Performance
  - VP9 & HEVC @ 4Kp60, AVC @ 4Kp30
  - Other formats @ 1.5 - 2x HDp60
  - JPEG ~80Mpixels/sec 4:2:0
  - Optimized for area, but scalable to support higher rates

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Summary

- Architecture needs to be defined with capabilities of target technology in mind
- Best architectures are result of end-application experience
  - Architected at a system level rather than a functional level
- Building on existing architectures minimizes both time-to-market and silicon area
- Flexible architecture allows trade-offs to be made for target technology

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