IP Reuse for the Masses

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Elements for Mass Acceptance

SIMPLE

ACCESSIBLE

SCALABLE

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Innovating! Together.
More Complex Than Ever!

Transistor Count (for largest MPUs & GPUs)

Continued Complexity

Productivity Gap
Affects all designs!

System Design Automation

Design Productivity
IP reuse required!

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Non-Critical Path IP Development

Parameterized IP Design

IP Imports
C / C++ / RTL Verification

Protected Functional IP Sharing

New IP Requests

Ultra-High IP Reuse

Customized Parameters

SoC Design Integration

No-Touch! Integration Ready

SDA PLAYERS IP Management

non-critical path

Innovating! Together.
Automated Critical Path Design

Parameterized IP Design

- IP Imports
- C / C++ / RTL Verification

- New IP Requests
- Protected Functional IP Sharing
- Ultra-High IP Reuse
- Customized Parameters
- SoC Design Integration

ZERO EFFORT Automation On-Demand!

- Design & Test Bench Generation

REQUIRES:

- Methods of Operation
- Architecture Topology
- Tools

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Integrated Simulation Environment

- New IP Requests
- Parameterized IP Design
- IP Imports
  - C / C++ / RTL Verification
- Ultra-High IP Reuse
- Customized Parameters
- SoC Design Integration
- Protected Functional IP Sharing
- Synthesizable Full-Chip RTL Export
- Parameter Optimization
- Inherited IP and SoC Design Verification
- Automated Critical Path
- Non-critical Path
- IP Management
- Parameterized IP Design

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How Simple?

- Orchestrate designs by just adding IP and auto building simulation ready RTL design with test bench.
- Not simply IP stitching. Designs built upon a highly flexible and configurable method of operation and efficient architecture.
- Designs may be simply tuned by defining configuration settings and limiting flexibility as desired.
- IP wrappers translate IP to SDA method of operation.
- Integrated compiled simulation engine allows for inherited IP scripts for verifying IP in it’s integrated form.
- Automatic user guide documentation.
How Simple?

- Integrated compiled simulation engine allows for inherited IP scripts for verifying IP in its integrated form.
- Inherited foundation and IP specific tasks for aiding system simulation and UVM build environments.
- Interactive TCL based scripting environment.
- C/C++ model capable.

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How Accessible?

- Web secure accessible – no software installs!
  - ORCHESTRATE SoC Developer – full hands-off SoC/FPGA design from PLAYERS IP library elements.
  - AUDITION IP Developer – IP specification and import of IP and IP test benches.
  - REHEARSE Simulation – interactive and TCL script based simulation environment
- All SDA accomplished server side
  - IP source code protected until export.
  - Controlled IP and SoC design sharing.
- SDA ecosystem available to all project stakeholders.
• SIMPLIFY AND ACCELERATE
• UNIQUELY COMPLIMENTARY
• STRONGER TOGETHER
• CONSISTENT QUALITY
• EXPERIENCED EXPERTS
IP Reuse for the Masses!

Automated front-end SoC/FPGA design through IP reuse

Secure web-based accessibility for IP providers and SoC/FPGA developers

Scalable infrastructure and community
THANK YOU!

Q & A