



Concertal Systems, Inc.

System Design Automation

Innovating!
Together.

IP Reuse for the Masses

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SIMPLE



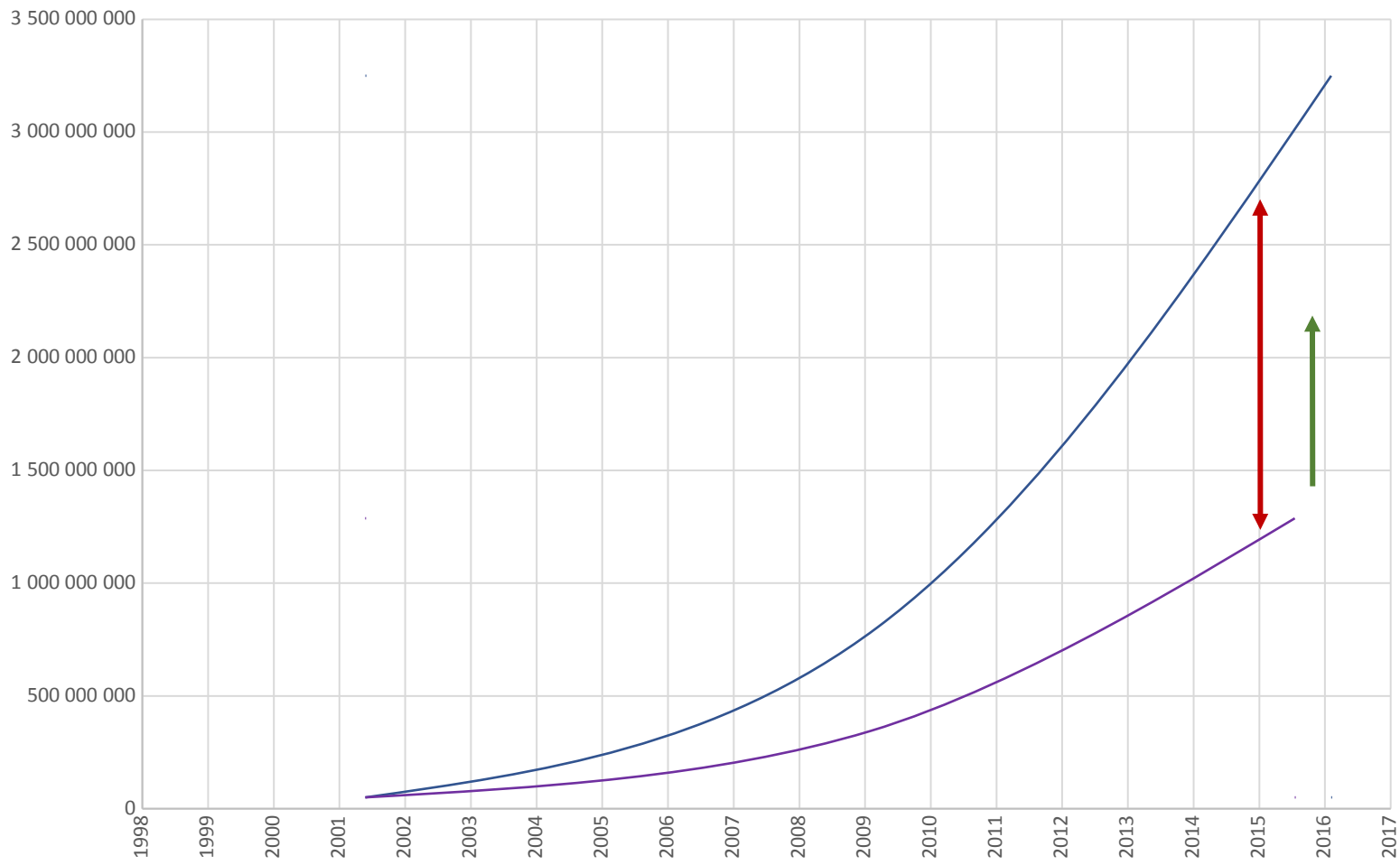
SCALABLE



ACCESSIBLE



Transistor Count (for largest MPUs & GPUs)

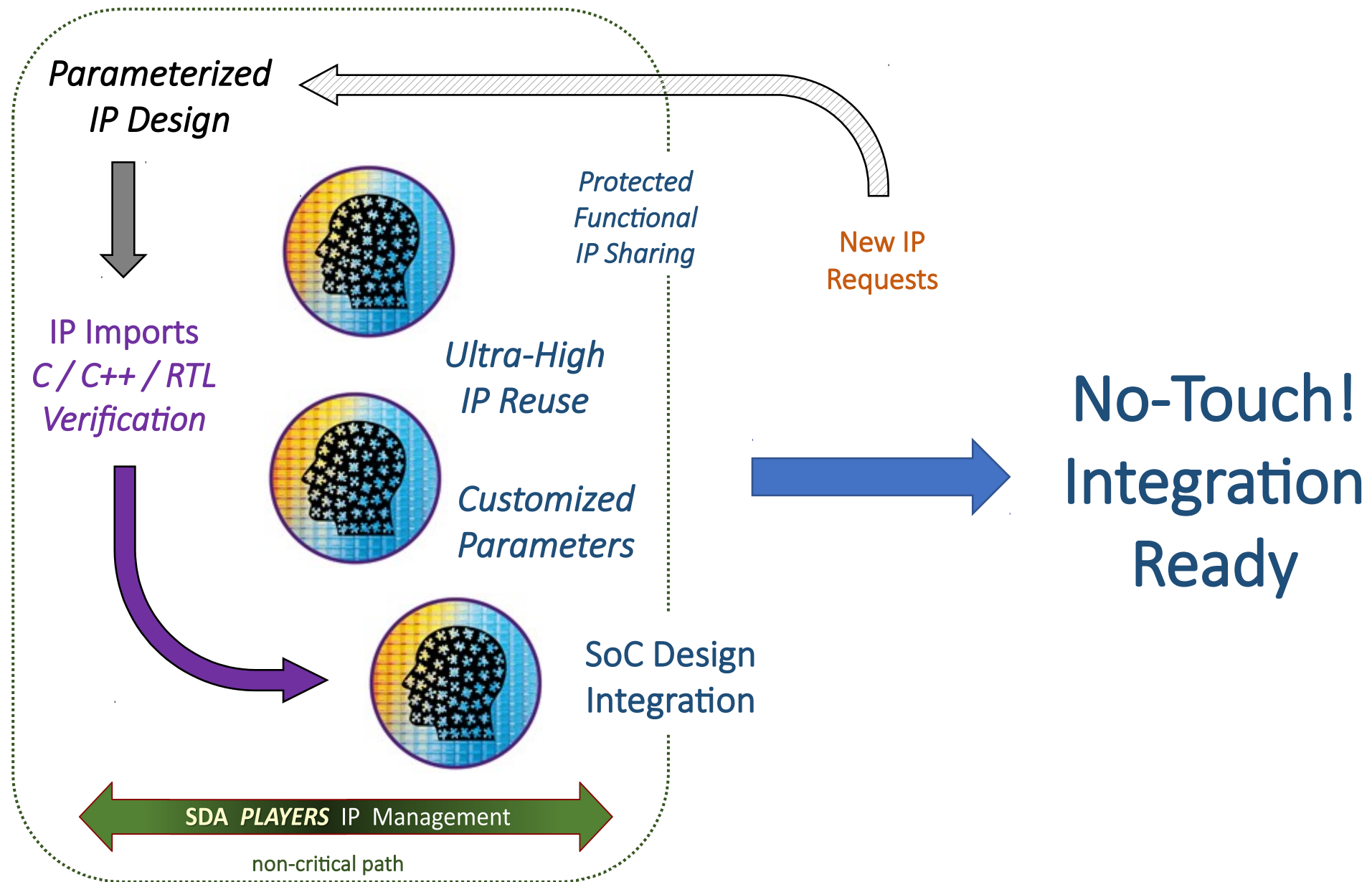


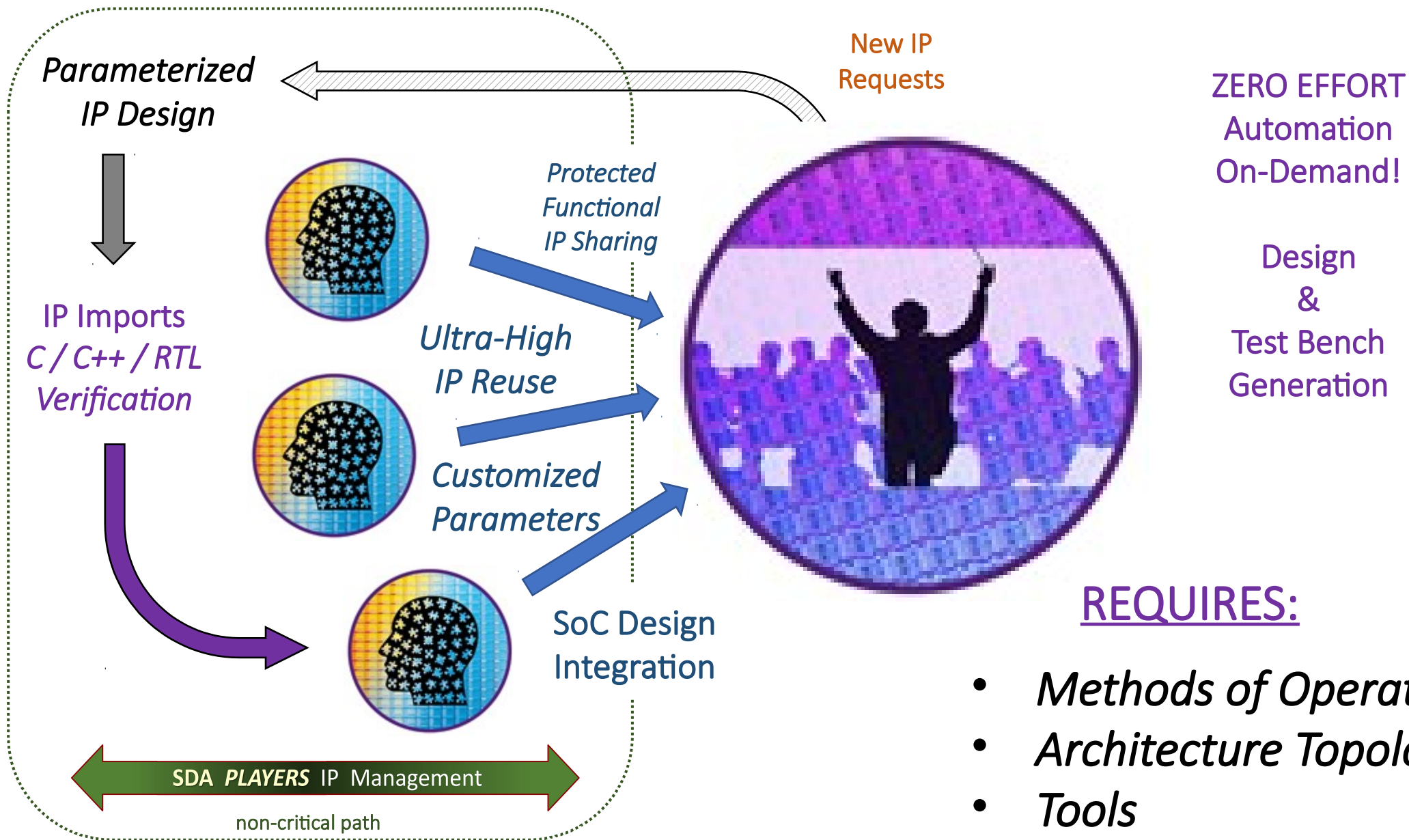
Continued Complexity

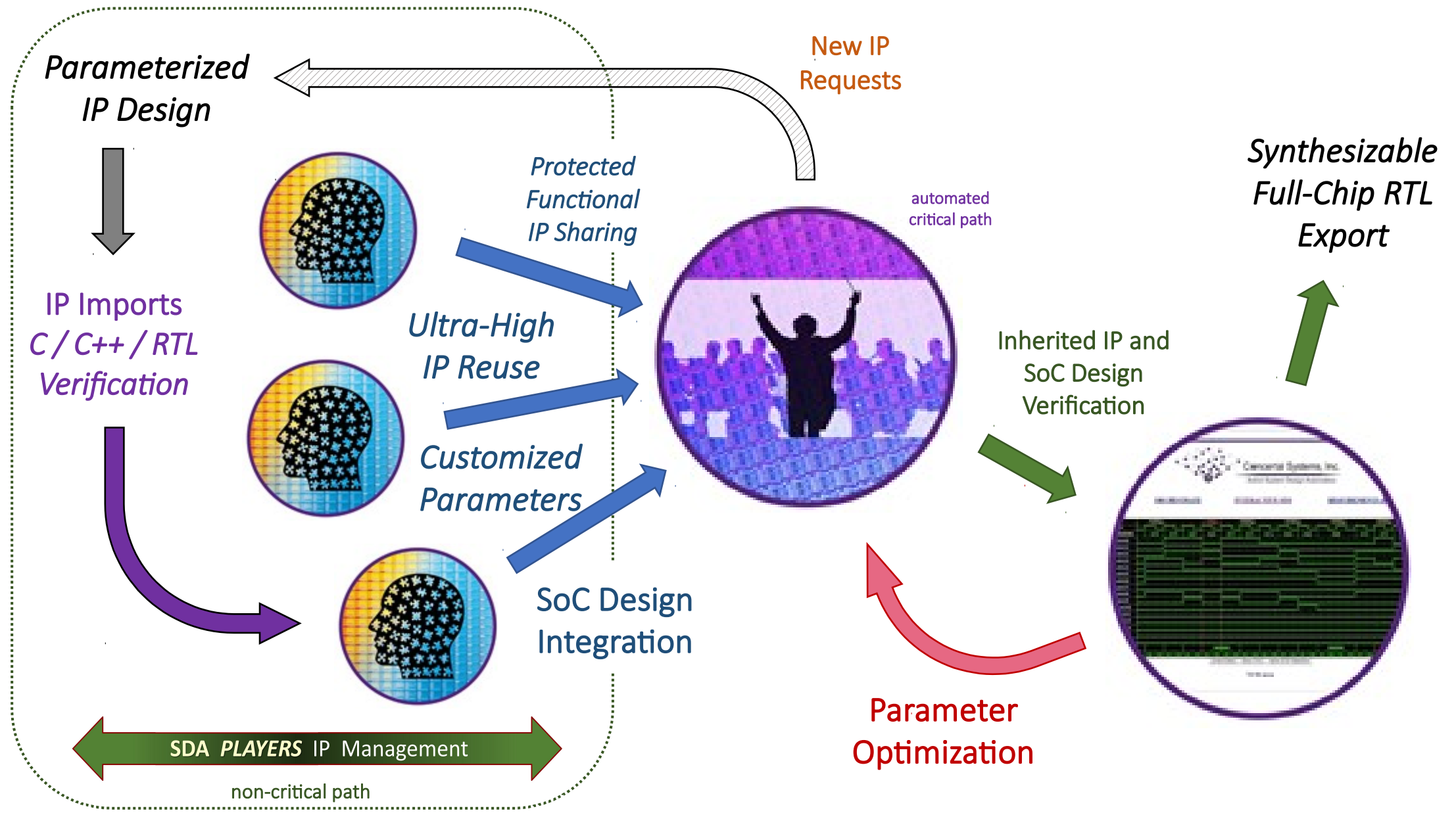
Productivity Gap
Affects all designs!

System Design Automation

Design Productivity
IP reuse required!









Component	Type	UPL	CFU	URU	PUL	SS	Count
0 Handler	Specification	UPL	CFU	URU	PUL	SS	1
1 SPIX16CH	Specification	UPL	CFU	URU	PUL	SS	2
2 COM0	Specification	UPL	CFU	URU	PUL	SS	3
3 COM1	Specification	UPL	CFU	URU	PUL	SS	4
4 COM2	Specification	UPL	CFU	URU	PUL	SS	5
5 COM3	Specification	UPL	CFU	URU	PUL	SS	6
6 PDM0	Prototype	UPL	CFU	URU	PUL	SS	7
7 PDM1	Prototype	UPL	CFU	URU	PUL	SS	8
8 PDM2	Prototype	UPL	CFU	URU	PUL	SS	9
9 PDM3	Prototype	UPL	CFU	URU	PUL	SS	10
10 PWM4	Data Release	UPL	CFU	URU	PUL	SS	11
11 ARMM0A	Specification	UPL	CFU	URU	PUL	SS	11

- Orchestrate designs by just adding IP and auto building simulation ready RTL design with test bench.
- Not simply IP stitching. Designs built upon a highly flexible and configurable method of operation and efficient architecture.
- Designs may be simply tuned by defining configuration settings and limiting flexibility as desired.
- IP wrappers translate IP to SDA method of operation.
- Integrated compiled simulation engine allows for inherited IP scripts for verifying IP in it's integrated form.
- Automatic user guide documentation.

How Simple?



Concertal Systems Design Portal

Dashboard / WPdesign1 / Rehearse / Simulation

Save VCD Standard Graph Color Palette

Command:

Script Category: Scripts
Select type of script to display list for

Available category items

The below scripts are bundled at build time. These scripts may not reflect edits completed after the build was generated

- image.hex
- run.do
- ini.waveviews
- demo1_handler_event_dividers
- demo4_COMB4_PDMreceivers
- demo3_console_sinewave_generators
- demo5_PDM4_transmitters
- demo2_mirror_DU7events_to_TBevents

Simulation waiting for input...

```

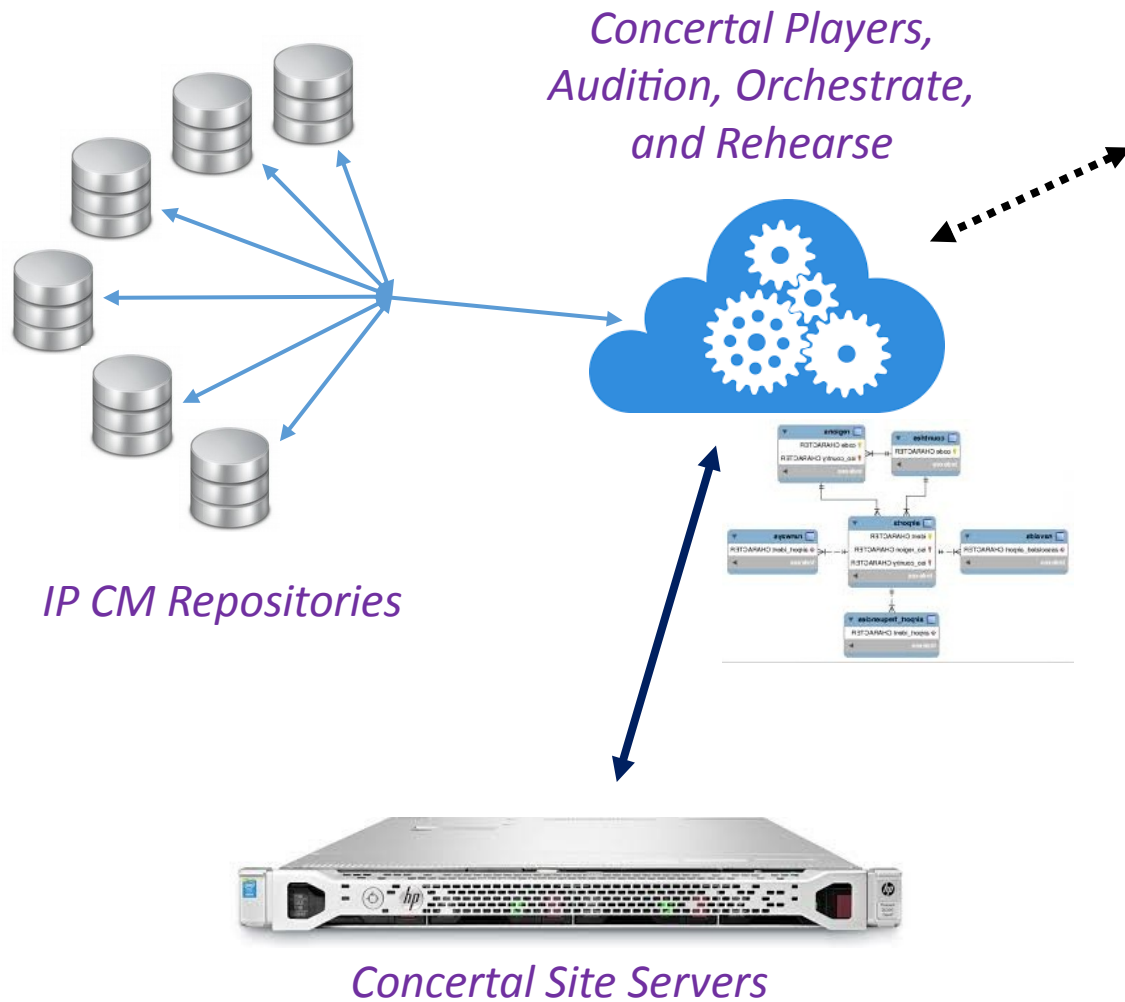
* ..loading: bus_1shot
* ..loading: readDirect <addr>
* ..loading: writeDirect <addr> <data>
* ..loading: captureSource <addr> <signalname>
* ..loading: T_bus_1shot
* ..loading: T_readDirect <addr>
* ..loading: T_writeDirect <addr> <data>
* ..loading: T_captureSource <addr> <signalname>

Finished loading system handler procedures.
* Finished loading Test Bench system handler procedures.

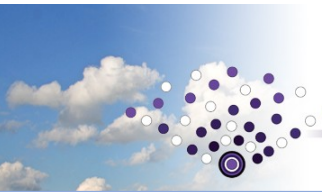
In SinTrigger constructor.
Instituted a 4360 Hertz sine wave generator going out to source address 2001 on signal Fs
    
```

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- Integrated compiled simulation engine allows for inherited IP scripts for verifying IP in it's integrated form.
- Inherited foundation and IP specific tasks for aiding system simulation and UVM build environments
- Interactive TCL based scripting environment.
- C/C++ model capable



- Web secure accessible – no software installs!
 - ORCHESTRATE SoC Developer – full hands-off SoC/FPGA design from PLAYERS IP library elements.
 - AUDITION IP Developer – IP specification and import of IP and IP test benches.
 - REHEARSE Simulation – interactive and TCL script based simulation environment
- All SDA accomplished server side
 - IP source code protected until export.
 - Controlled IP and SoC design sharing.
- SDA ecosystem available to all project stakeholders.



- SIMPLIFY AND ACCELERATE
- UNIQUELY COMPLIMENTARY
- STRONGER TOGETHER
- CONSISTENT QUALITY
- EXPERIENCED EXPERTS



Automated front-end
SoC/FPGA design
through IP reuse



Scalable infrastructure
and community



Secure web-based
accessibility for IP providers
and SoC/FPGA developers



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THANK YOU!

Q & A

