CurrentRF
On-Chip Super Capacitor IP
(Power Optimizer)

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IP Product Offerings

CC_100 Super Cap IP Test Chip

CC_100 Super Cap IP Cell

Patent Pending
Super Capacitor IP Test Chip (Theory)

CC_100 Super Cap IP Test Chip

V_{plus} = \frac{V_{plus}}{2} + \text{Base Capacitance Increase}

Effective Capacitance Increase

Patent Pending
Super Capacitor IP Test Chip (Example)

The Effective Capacitance Increase Follows the Base Input Capacitance
CC_100 Super Capacitor IP (Theory)

\[ V_{\text{plus}} = \text{Base Capacitance} + \text{Effective Capacitance Increase} \]

Patent Pending
CC_100 Super Capacitor IP (Example)

The Effective Capacitance Increase Follows the Base Input Capacitance
RF Amplifier Sensitivity Enhanced with the CC_100 Super Capacitor IP

Patent Pending
Super Capacitor IP Integration
CC_100 Super Cap IP Benefits/Features

- Energy Harvesting (Up to 20% Reduction in Dynamic Current)
- RF Emissions Reduction (Up to 20% over Standard DCAPs)
- At least a 2X Effective Capacitance increase over standard DCAPs
- A 25% reduction in Effective Series Inductance (ESL)
- Enhanced System PSRR (Cleaner System Spectral Outputs)
- Draws No Operational DC Power
- CC_100 IP can be shaped into any form factor
- CC_100 IP used as a standard DCAP
- Customizable Design
CC_100 IP Equals PowerStic/Exodus

CC_100 IP in USB PowerStic Packaging
CC-100 IP Dynamic Power and Emissions Reduction

Missing/Suppressed Frequencies
Equals Cancelled Emissions and Power Saved
1 Watt/25 Watts=4% Minimum Power Reduction
(1/5 the total power of a Supermicro Server or
Roughly Equivalent to an Average Laptop)
CC-100 IP High Frequency Dynamic Emissions Reduction

RF Emissions - CC-100 IP Disengaged

RF Emissions - CC-100 IP Engaged
10mA Current Reduction
CC_100 IP Low Frequency Dynamic Emissions Reduction

20% Dynamic Power Reduction

CC_100IP Disengaged

CC_100IP Engaged
CC_100 Flash Memory Power and Emissions Reduction

Flash Memory RF Emissions Reduction

- **Green Plot** -- CC-100 IP Disengaged
- **Blue Plot** -- CC-100 IP Engaged -- 2mA current reduction
CC_100 IP S11 Input Reflection Performance

- Almost Perfect S11 Reflection Performance—SWR=1.00
- Lowest Impedance Point-370 MHz
- Tracks an 11μF Capacitive Impedance Curve
CC_100 IP S11 Total Reflection Performance

- Network Analyzer Detectors Activated By CC_100 IP
- Return Current—Slight Reduction In Overall SWR
- Lowest Impedance Point-170 MHz
- Tracks a 22uF Capacitive Impedance Curve
CC_100 IP System PSRR Enhancement

- Same Dynamic Current Reduction
- Spectral Bandwidth Noise Reduction With Multiple CC_100 IP Super Capacitor Cells.
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