Virtual Array Architecture for eFPGA

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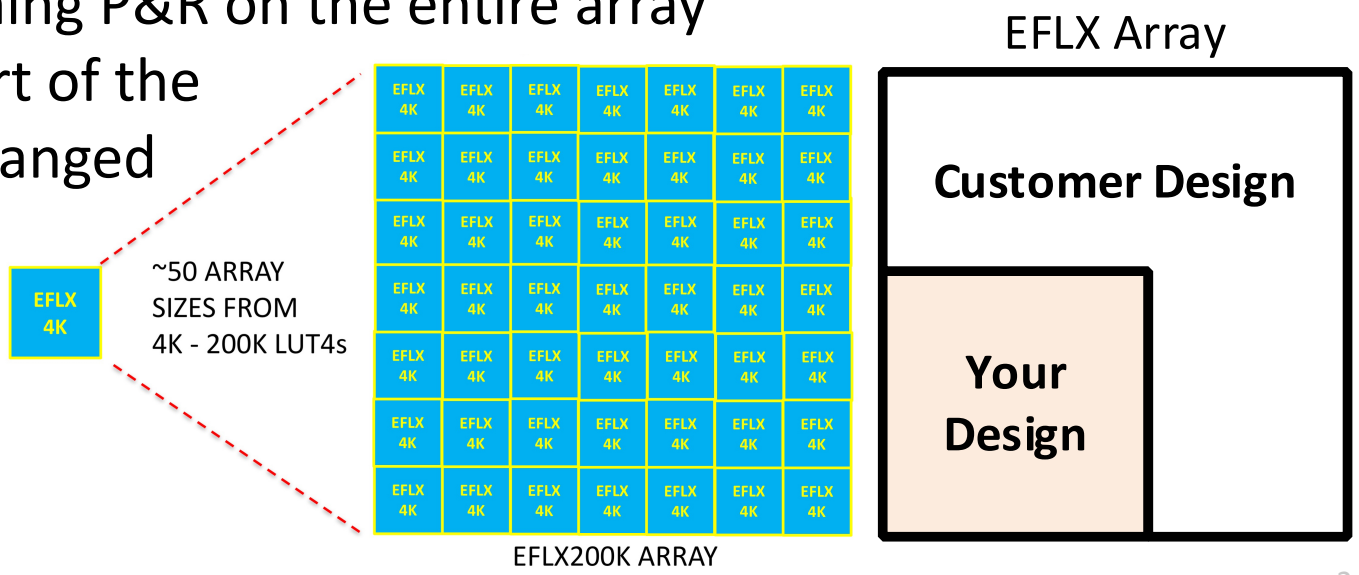
Cheng C. Wang – SVP of Engineering

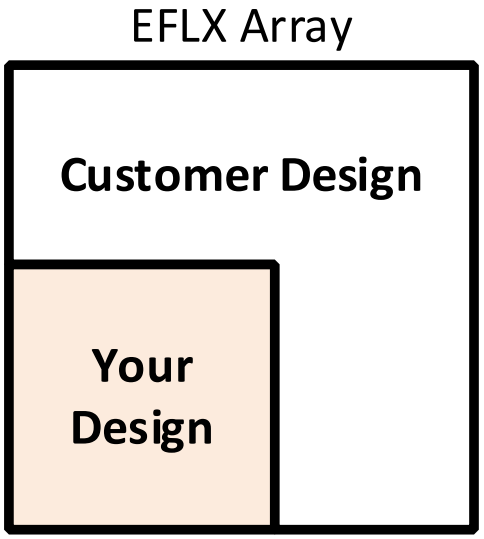
Why the Need for Virtual Arrays?

- Security:
  - Keep your “secret sauce” design masked from the customer
- Preserve Performance & Density:
  - “Harden” your optimized design for best performance & density on EFLX arrays, even when the rest of the design changes
- Runtime:
  - Avoid performing P&R on the entire array when your part of the design is unchanged



Virtual Array Solution

- Have your “secret sauce” IP and customer design on one EFLX array
  - Designs inside black-box tiles are not visible by end-user
  - Remaining EFLX tiles remain user-programmable



- Maintain optimal performance and density of EFLX designs
  - Preserve P&R performance in black-box tiles
  - Black-box bitstream is merged directly into the final bitstream
- Improve EFLX Compiler runtime
  - Designs in black-box tiles are not P&R’ed again

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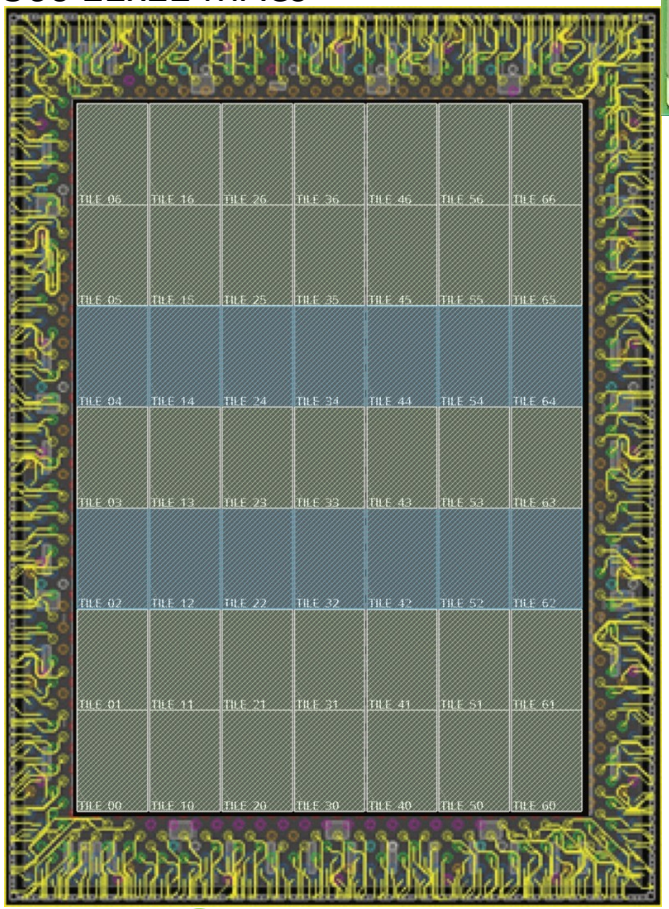
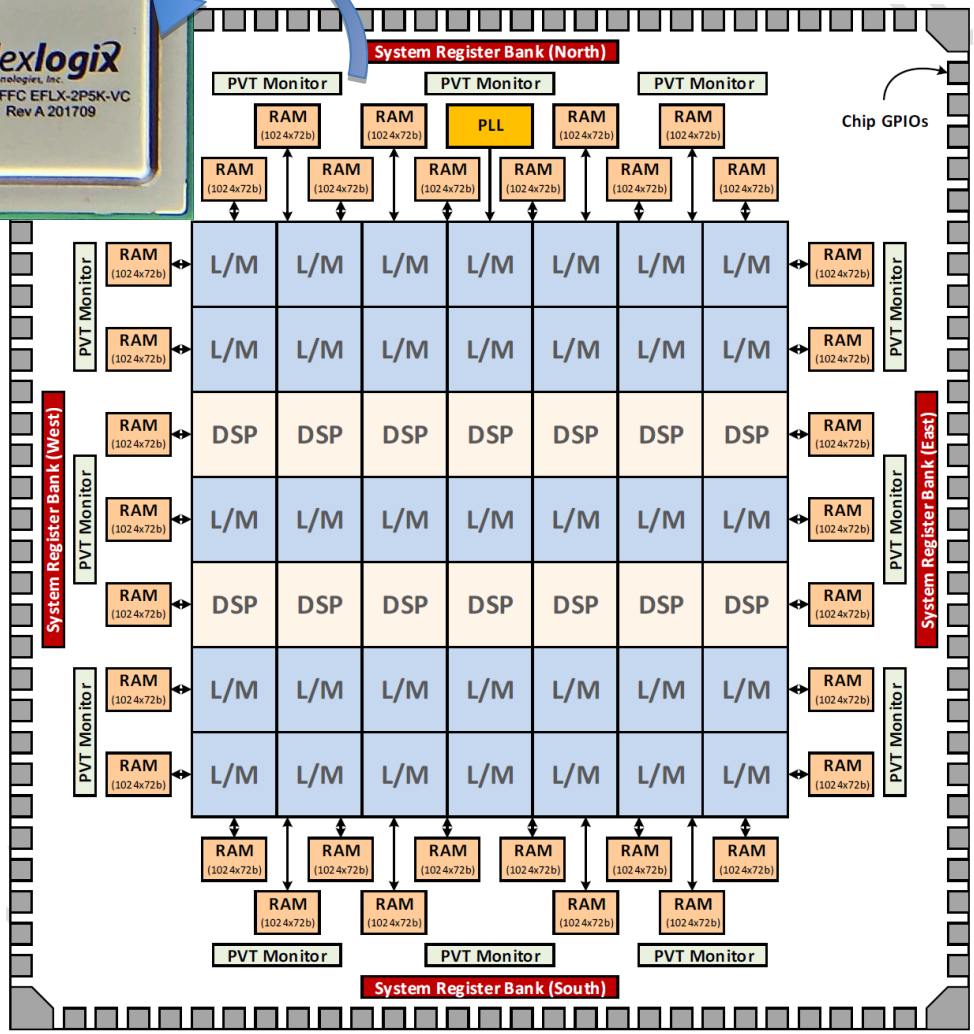
Patent Pending on EFLX Virtual Array Technology

Example: EFLX200K Test Chip in TSMC16FFC

- 7x7 Array
  - 114,240 6-LUTs (~183K LUT4s)
  - 560 22x22 MACs





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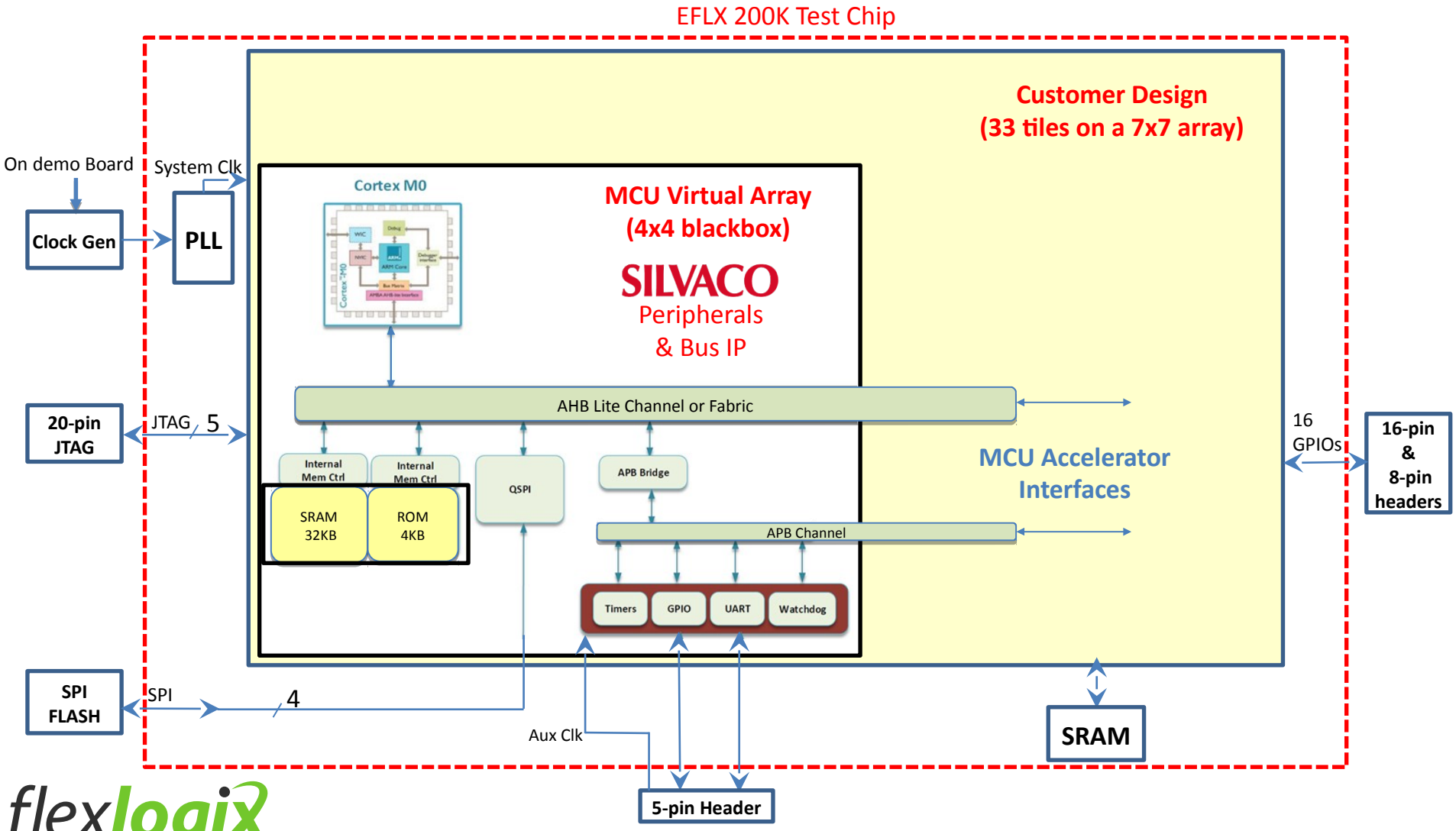
MCU Virtual Array on EFLX 200K Test Chip



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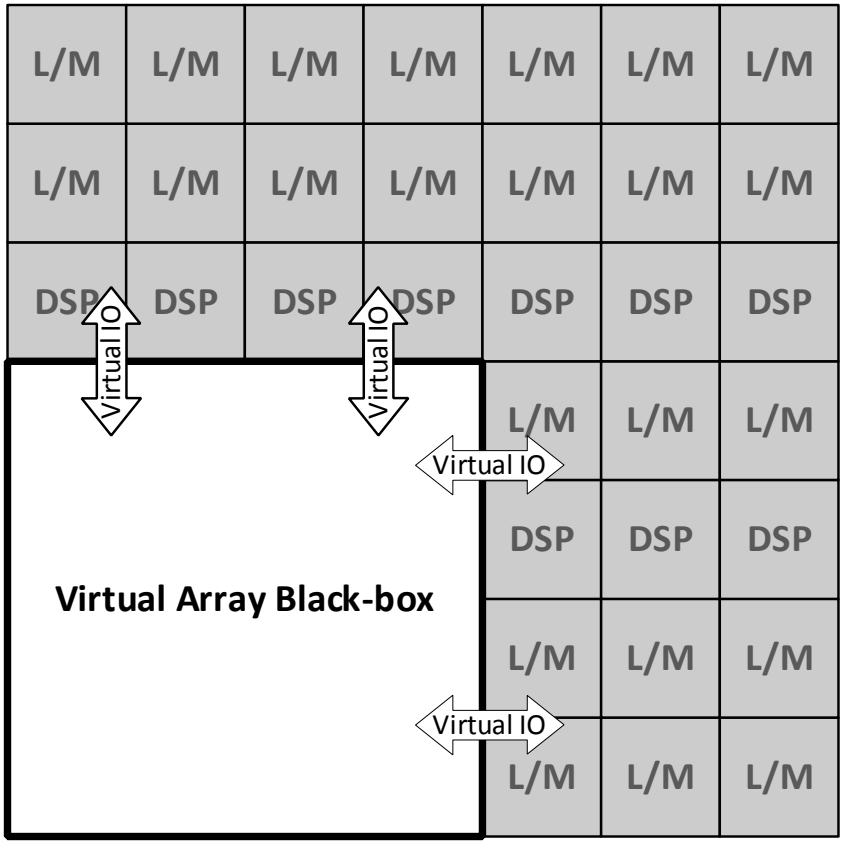
Virtual Array Definition

Each EFLX array can have one or more black-box virtual arrays

- Each virtual array is a sub-module of the top-level, no direct IO access is needed
- Each virtual array should have its virtual I/Os placed towards the other tiles of the EFLX array



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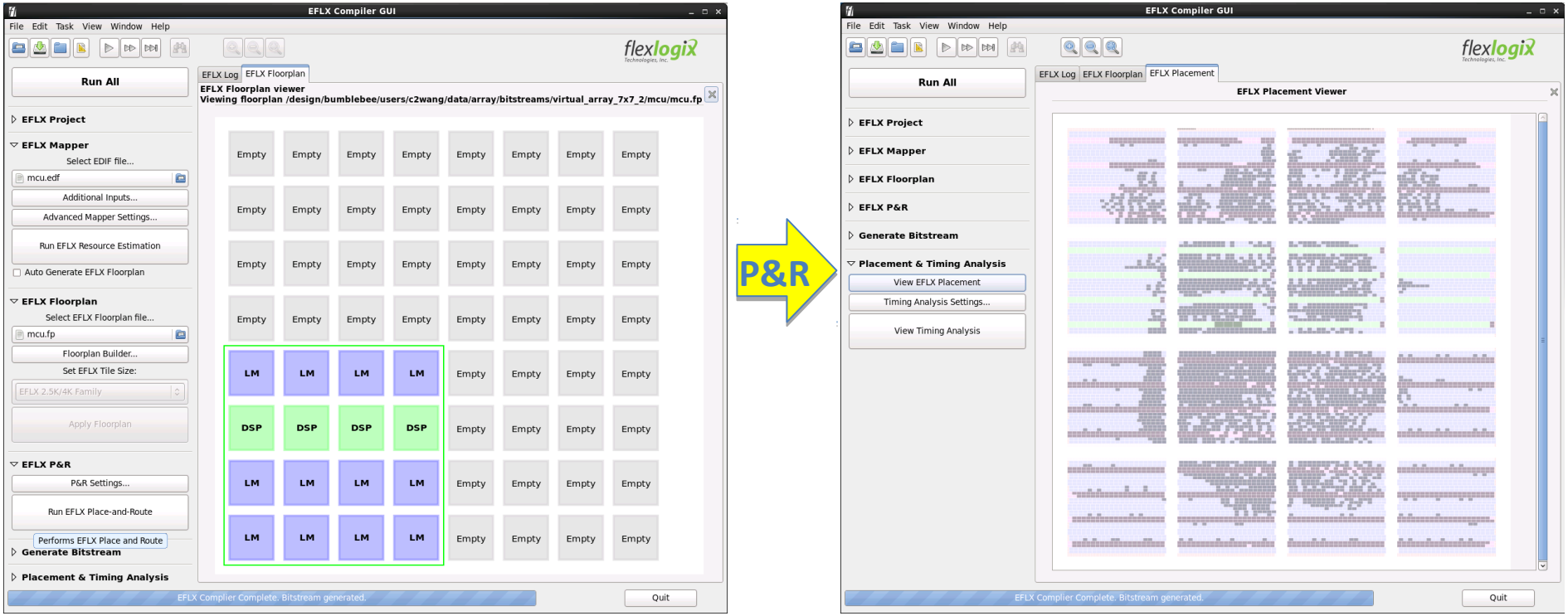
Virtual Array Compilation

Other than pin placement, compiling a 4x4 black-box virtual array is no different from a regular 4x4 array

- EFLX Compiler offers complete netlist-to-bitstream solution



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Black-box Definition (Auto-Generated)

A black-box definition: EFLX Precompiled Macro (.epm)

- Defines black-box essentials: module name, footprint, IO location, clock utilization
- The epm is auto-generated with "`-GENERATE VIRTUAL ARRAY`" flag

File Edit Options Buffers Tools Help

```
# EFLX Precompiled Macro Specification File
# This file was auto-generated and may be missing some fields. Such fields will be marked for user intervention.
# Order does not matter and un-quoted whitespace does not matter. Field names (left-hand side) are case-sensitive.
# Anything after a `#` character is ignored until the next line.

# Dimensions of the design, given as [tile x (North), tile y (East)]
tile_array_dimensions=[4,4]

# Offset of this virtual array in the top-level design, given as [tile x (North), tile y (East)] from [0,0] in the top-level design
tile_offset=[0,0]

# The virtual array's module's name
module_name="MCU_Top_EFLX"

# The virtual array's bitstream file path
bitstream="MCU_Top_EFLX.bin"

# Clock routing information used when compiling the top-level design.
# clock domain name followed by a list of coordinates and which CLK TILE needs the clock.
clock_info="extClk",[[0,0,0],[1,0,0],[2,0,0],[3,0,0],[0,1,0],[1,1,0],[2,1,0],[3,1,0],[0,2,0],[1,2,0],[2,2,0],[3,2,0],[0,3,0],[1,3,0],[2,3,0],[3,3,0]]

# The virtual array's IO Specification file path
io_spec="MCU_Top_EFLX.io"

# The top-level design's Floorplan file
top_level_fp="top_level.fp"

# The virtual array's Floorplan file
virtual_array_fp="MCU_Top_EFLX.fp"
```

-(Unix)--- MCU_Top_EFLX.epm All L19 (Fundamental)

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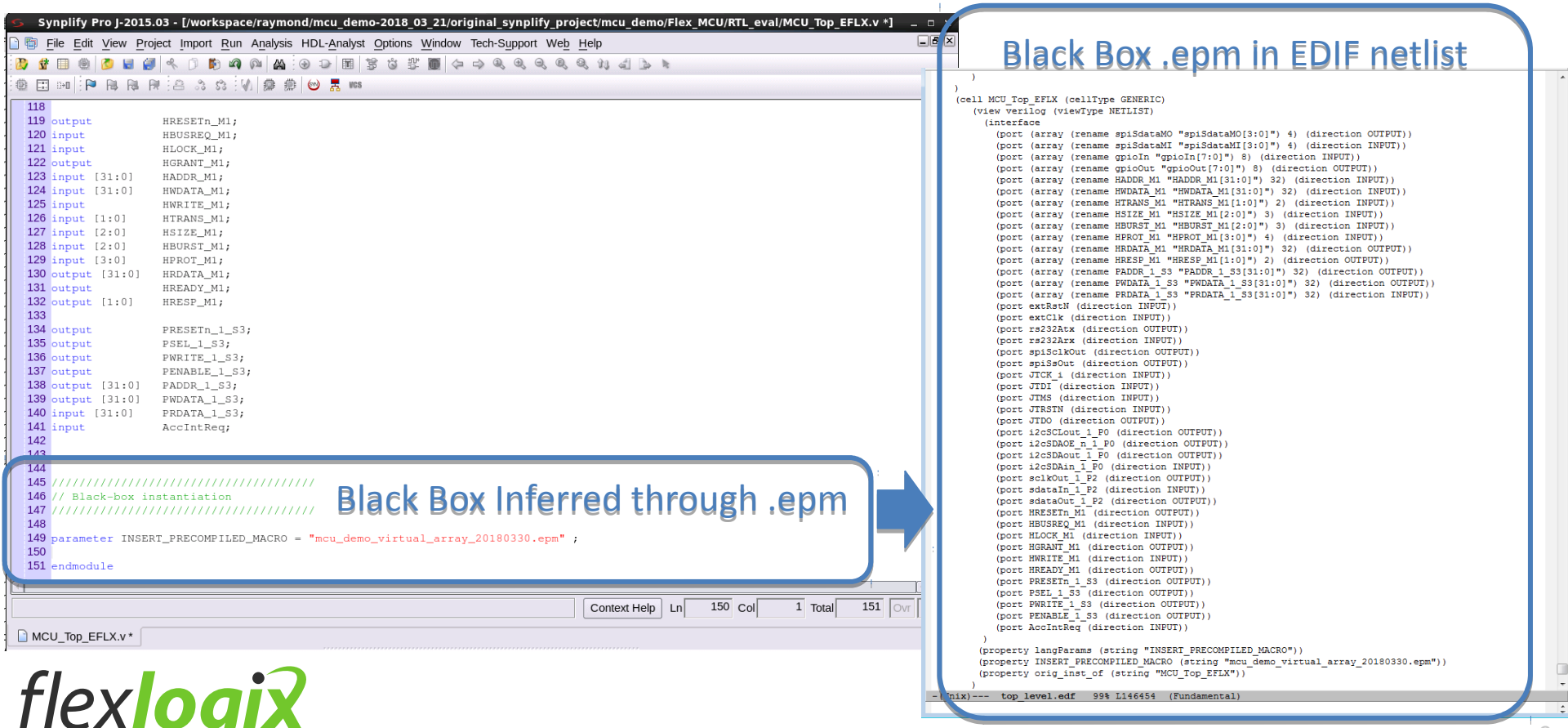
Instantiating a Black-box in Customer Design

The black-box module content is removed from the customer design, and replaced with the .epm inference

- .epm black box is automatically preserved through Synplify



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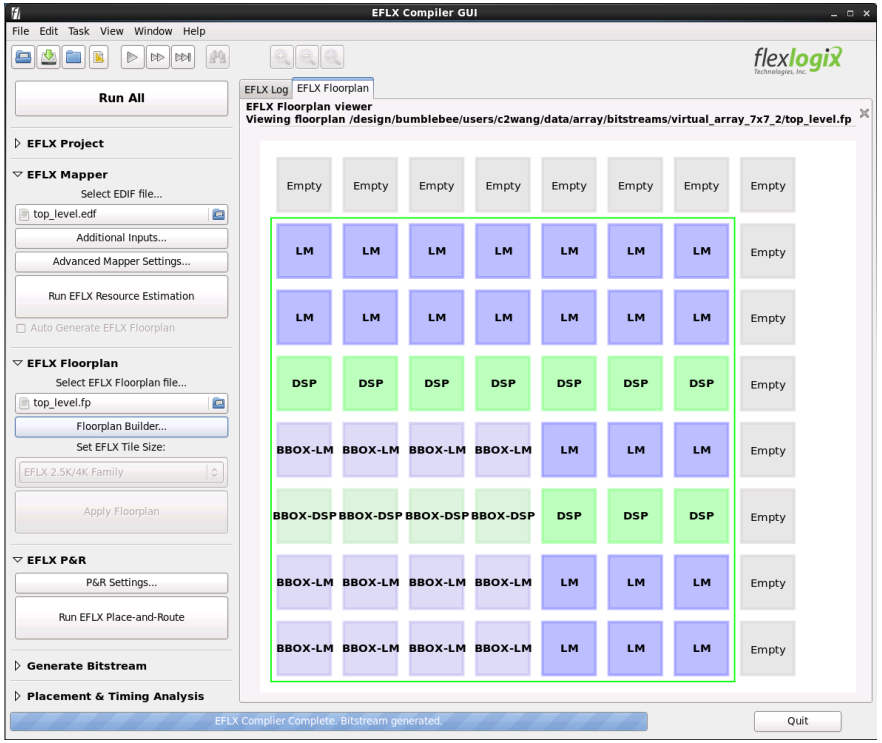
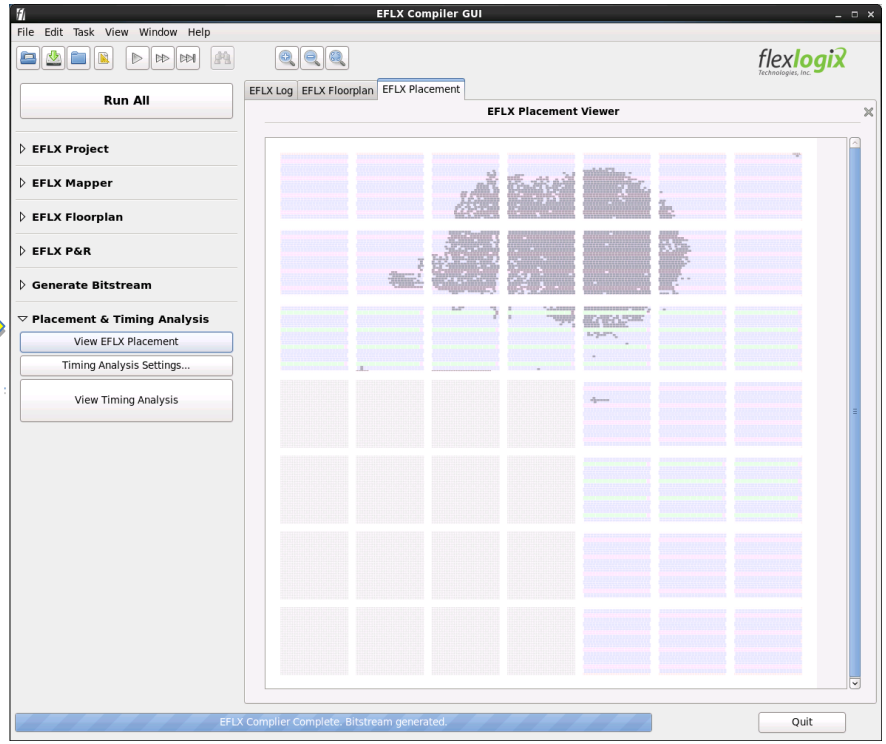
Running Black-box Design in EFLX Compiler

Load a top-level floorplan with the black-box tiles labeled

- EFLX Compiler connects top-level design with black-box design during P&R
- No user visibility into what's inside the black-box



P&R



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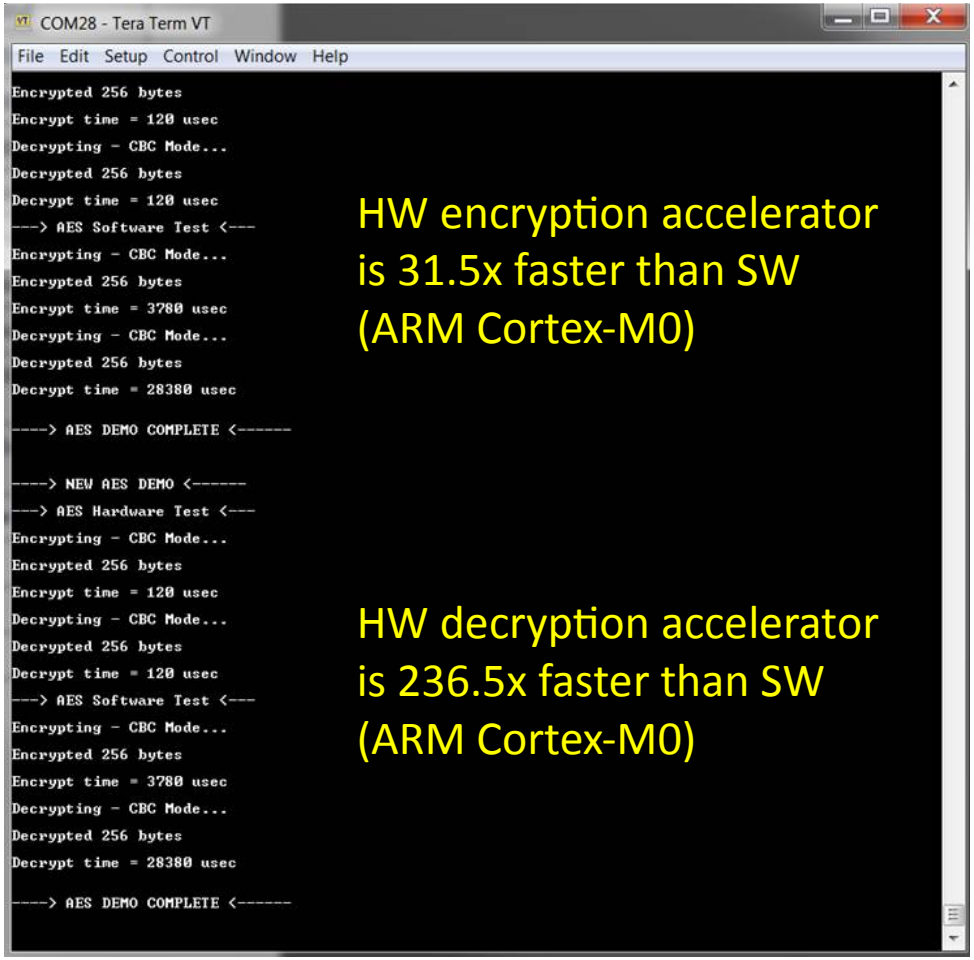
Running Blackbox Designs in Silicon

Black-box MCU (CM0) executes the AES enc/decryption in SW

Custom accelerator executes the same enc/decryption in HW



HW encryption accelerator is 31.5x faster than SW (ARM Cortex-M0)

HW decryption accelerator is 236.5x faster than SW (ARM Cortex-M0)

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Conclusion: Virtual Array Benefits

- Virtual array is a simple way to insert a pre-compiled black-box in to the customer design
- **Secure**: User has no visibility into the black-box design
- **Predictable**: Pre-compiled design is frozen, preserves PPA
- **Fast**: Pre-compiled design portion is not P&R'ed again
- **Flexible**:
  - Maintain user-programmability in the rest of the designs
  - User can choose to instantiate the black-box or not
  - Updates to .epm can be downloaded as an image file
- **One of many ways to build a flexible, secure, and high-quality EFLX IP ecosystem**

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