Optimizing selection of GLOBALFOUNDRIES ASIC and Foundry to achieve optimal IC Solutions

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Problem Statement

- Design costs are rising dramatically as nodes advance\(^1\)
  - 28nm - $30M  14nm - $80M  7nm - $271M
- Complex technology driving skill requirements, higher risks\(^2\)
  - Highly complex IP and ballooning IC content drives integration and verification complexities
  - Routing congestion and timing closure challenges due to increased IP content and longer thinner wires
  - Tighter design margins, power supply noise sensitivity, overdesign risk to address variations . . .
- Program budgets spread over multiple years
  - Limits scope in any given year, drives phased projects, increases total cost
- GlobalFoundries’ engagement models allow tradeoff to help optimize each program
  - Foundry / Customer owned tools (COT) \(^3\)
  - GlobalFoundries ASIC flow \(^4\)

\(^1\) [https://semiengineering.com/racing-to-107nm/](https://semiengineering.com/racing-to-107nm/)
\(^2\) [https://semiengineering.com/design-for-silicon-success-at-7nm/](https://semiengineering.com/design-for-silicon-success-at-7nm/)
\(^3\) [https://www.globalfoundries.com/technology-solutions/cmos/performance](https://www.globalfoundries.com/technology-solutions/cmos/performance)
\(^4\) [https://www.globalfoundries.com/technology-solutions/asics](https://www.globalfoundries.com/technology-solutions/asics)
Multi-dimensional Solution Approach

Focus on systems and solutions for the end-space markets

Integrate value with platforms, collaborative partnerships and ecosystems

Differentiate through a rich portfolio of Intelligent Technologies to meet customer needs

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Technologies and Solutions Focus

Extensive suite of offerings and services fully enable customers across a range of markets

**CMOS**
Broad technology portfolio across leading-edge and mainstream nodes

**RF**
Comprehensive enablement and extensive, optimized RF portfolio including RF SOI and SiGe

**Aerospace & Defense**
Leverages offerings across the GLOBALFOUNDRIES portfolio to provide solutions for Trusted and Aerospace and Defense applications for both government and commercial markets

**ASIC**
Deep expertise and richest portfolio of best-in-class IP for wireless/wired network and data center applications in the foundry industry

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Typical IC Development Activities

High Level Design → Logical Design → Synthesis → Physical Design → Verification → Checking/Release → Mask Fab → Wafer Fab → Bump

- Timing Closure
- Stress and Qual.
- Bring up & Debug
- Test Development
- Module Test
- Bond Assembly
- Dice
- Wafer Test

Design Kits → EDA Tools → IP / Cores

Re-Spin (As Needed)
## Technology Portfolio Focus

<table>
<thead>
<tr>
<th>Technology</th>
<th>Logic</th>
<th>RF CMOS</th>
<th>mmWave RF CMOS</th>
<th>Embedded Memory</th>
<th>BCDLite® / BCD</th>
<th>High Voltage CMOS</th>
<th>RF SOI</th>
<th>SiGe PA</th>
<th>High Performance SiGe</th>
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</tbody>
</table>

- 🟢: Available
- 🟢: In development

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Dual Track Roadmap

Applications
- Servers
- HPC / Core Networking
- Graphics
- High-end smartphones

Features
- High-performance
- Balanced-cost

Premium Tier

High Performance Computing
FinFET
- EUV
- 7LP
- 7.5T
- RF
- Auto
- 12/14nm FinFET

Wireless, Battery-Powered Computing
FD-SOI
- eNVM
- eMRAM
- 12FDX™
- 22FDX®
- 28nm
- 40/55nm

Applications
- Low & mid-end smartphones
- Wireless
- IoT
- Autonomous vehicles
- Mobile camera

Volume Tier

Features
- Low-power
- Cost-effective performance
- RF
- Embedded memory

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Typical COT / Foundry Scope Ownership

- High Level Design
  - Logical Design
    - Synthesis
      - Timing Closure
        - Physical Design
          - Verification
            - Checking / Release
              - Mask Fab
                - Wafer Fab
                  - Bump
- Bring up & Debug
  - Stress and Qual.
  - Module Test
  - Bond Assembly
  - Dice
  - Wafer Test

- Design Kits
- EDA Tools
- IP / Cores

Customer

GlobalFoundries

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Vertically Integrated Solutions Provider = Your Advantage

- Improved time to market
- Lower risk
- Fully optimized solutions

Over 2,000 designs successfully executed

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Typical ASIC Scope Ownership

- High Level Design
- Logical Design
  - Synthesis
- Bring up & Debug
  - Re-Spin (As Needed)
- Stress and Qual.
- Module Test
- Bond Assembly
  - Test Development
- Mask Fab
- Wafer Fab
- Bump

- Checking/Release
- Timing Closure
- Verification

- Design Kits
- EDA Tools
- IP / Cores

- Customer
- GlobalFoundries

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## COT and ASIC Characteristics Compared

<table>
<thead>
<tr>
<th>Metric</th>
<th>COT</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flexibility</td>
<td>Greatest</td>
<td>ASIC methodology + Customer hard core(s)</td>
</tr>
<tr>
<td>Customer Effort &amp; skills</td>
<td>Greatest</td>
<td>Least</td>
</tr>
<tr>
<td>Deliverable to Customer</td>
<td>Untested Wafer</td>
<td>Tested, qualified, warranted Module</td>
</tr>
<tr>
<td>Product yield ownership</td>
<td>Customer owns Yield, wafer price</td>
<td>GF owns yield, firm fixed module price,</td>
</tr>
<tr>
<td></td>
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<td>committed supply line</td>
</tr>
<tr>
<td>Product Power</td>
<td>Neutral / Baseline</td>
<td>&gt;20% lower with integrated power</td>
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<tr>
<td></td>
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<td>methodology</td>
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<tr>
<td>Supply Chain Complexity</td>
<td>Greatest</td>
<td>Least</td>
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<tr>
<td>Development Cost</td>
<td>Higher</td>
<td>Lower</td>
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<tr>
<td>Schedule</td>
<td>Usually longer</td>
<td>Usually shorter</td>
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<tr>
<td>Production Cost</td>
<td>Potential to be lower</td>
<td>Can be higher</td>
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<tr>
<td>Risk</td>
<td>Highest</td>
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<td>Outgoing Quality</td>
<td>GF Owned</td>
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<tr>
<td>Product Reliability</td>
<td>Customer Owned and verified</td>
<td>GF Owned and warranted</td>
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</tbody>
</table>
GF IP EcoSystem

- Needs
- Value
- Function
- Supplier

- PDK
- Base IP
- flows

Focus on IP
Intelligent Asic Methodology (I-AM)

- Secure User Authentication
- Web Hosted
- Set of Vendor tools and Library
- SOC Set of Deliverables
- Secure Delivery
Floor Planner

User Netlist

IP Library Selection
PLL
HSS
SRAM
Processor Core
Generic Bus Protocol
PHY

Floor Planner

Global netlist

Floor Plan

Mode: Floor Planner  Example
Conclusions

- GF spans a broad Technologies from RF to FinFets
- GF spans from COT to full Turn Key solutions
- IP Ecosystem becoming Core to our business
- Exploring the Online Support model for our customers
Thank you