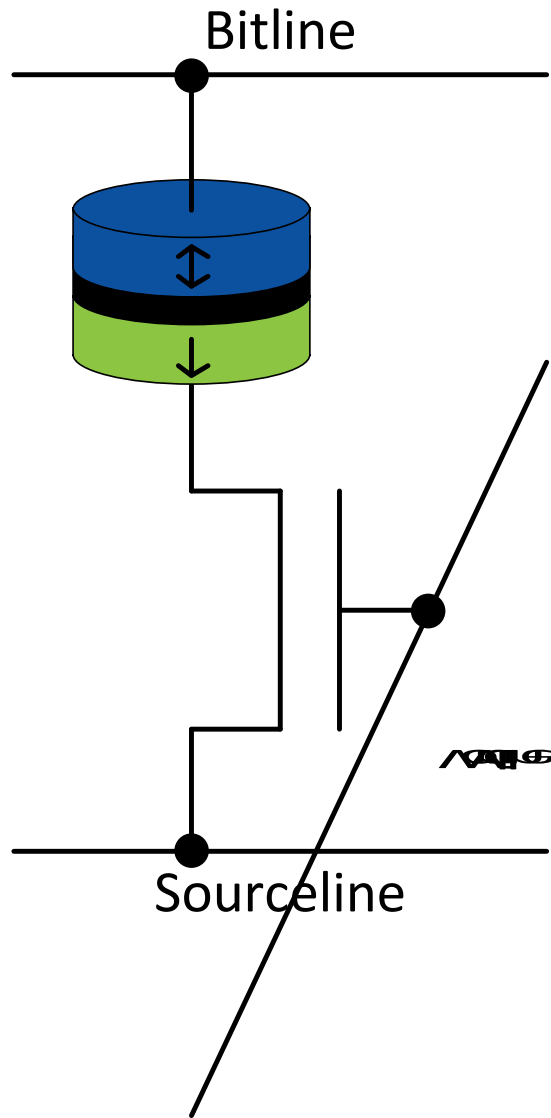


More Than Just eFlash

A Roadmap of How MRAM Will
Change SoC Architectures



Introduction



- For many years, MRAM has been “right around the corner.” Its been billed as:
 - SRAM killer
 - eFlash replacement
 - Enabler of instant on computers
- At least 3 major foundries are preparing to bring eMRAM into production
 - Production expected by end of 2018
 - Currently 28nm/22nm; roadmaps for 14FF/12FF and below
- So how exactly will MRAM fit into SoC architecture initially and as the technology continues to evolve?

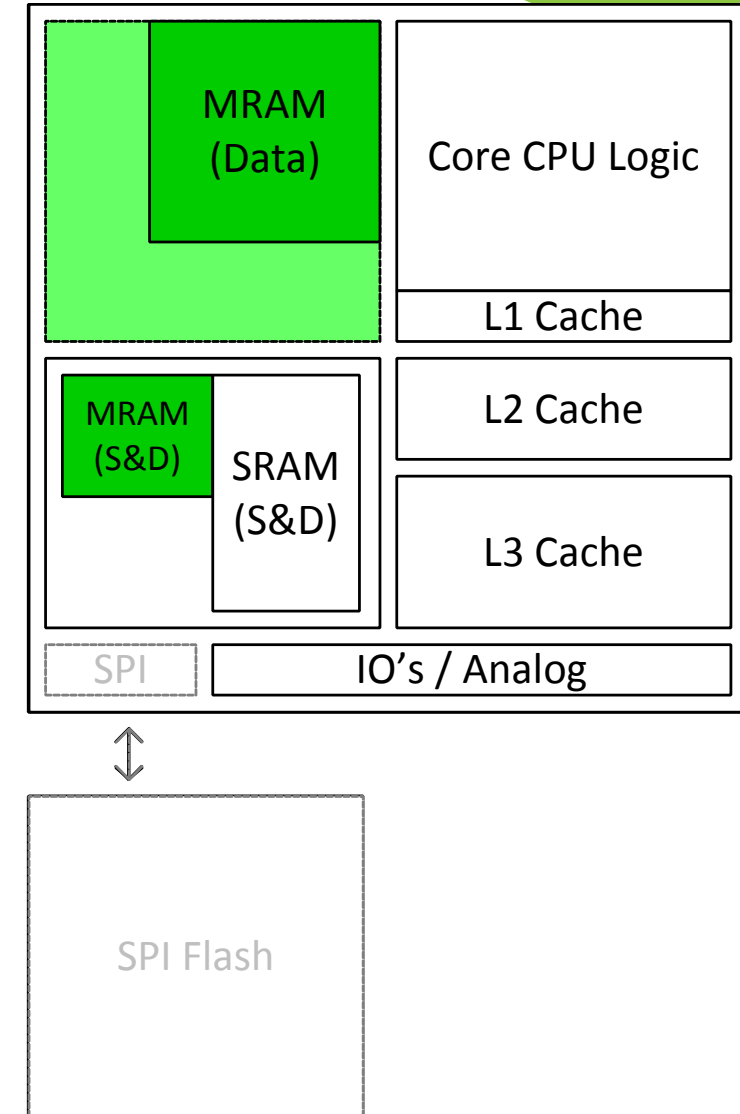
Comparison Overview

- Speed typically 10-100x faster than eFlash while still 2-10x slower than SRAM
- Active power typically 10-50x lower than eFlash
 - 2-4x higher than SRAM for Read
 - 4-200x higher than SRAM for Write
- Standby power near zero
 - No bitcell current unlike SRAM
 - Core voltage only reads unlike eFlash
- Significantly lower cost than either memory
 - ~½ the area of SRAM
 - Lower wafer cost and as much as 5x smaller than eFlash

	SRAM	MRAM	eFlash
Read Time	<1-2ns	2.0-20ns	10-100ns
Write Time	<1-2ns	10-1,000ns	10us-10ms
Read Power	0.1-0.4 uA/MHz/b	0.2-2.0 uA/ MHz/b	1-100 uA/MHz/b
Write Power	0.5-2.0 uA/MHz/b	2.0-400 uA/MHz/b	100-2000 uA/ MHz/b
Stdby Power	High	Low	Med / Low
Process Cost	Baseline	5-10%	15-25%
Area	6T + low overhead	2T + mid overhead	2T-10T + high overhead

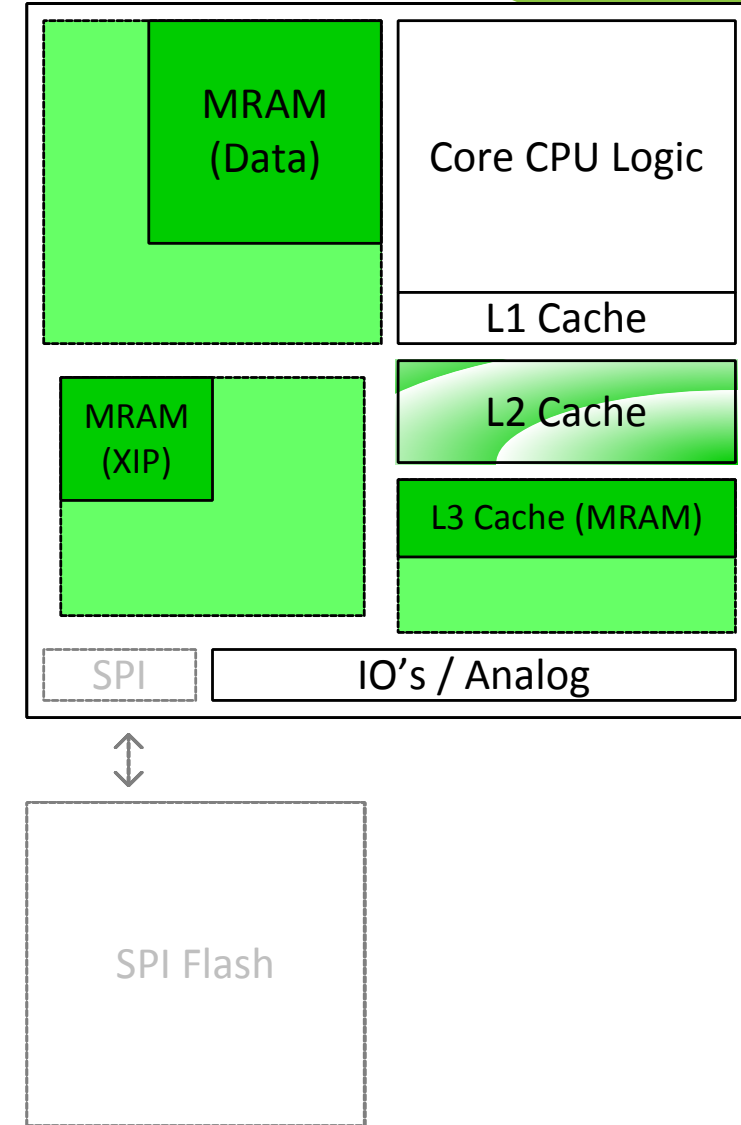
Cost Advantages: Displacing eFlash

- Preliminary driver of change is cost
 - 15-20% cost reduction expected (within scaling trend)
 - > ~10% wafer cost reduction due to larger geometry, backend layers
 - > ~5-10% die size reduction, depending on ratio of die spent on eFlash / MRAM
- Reduced cost/bit will shift boundary for internal / external NVM usage
 - Power savings
 - Board route reductions
 - Fewer pass-through costs

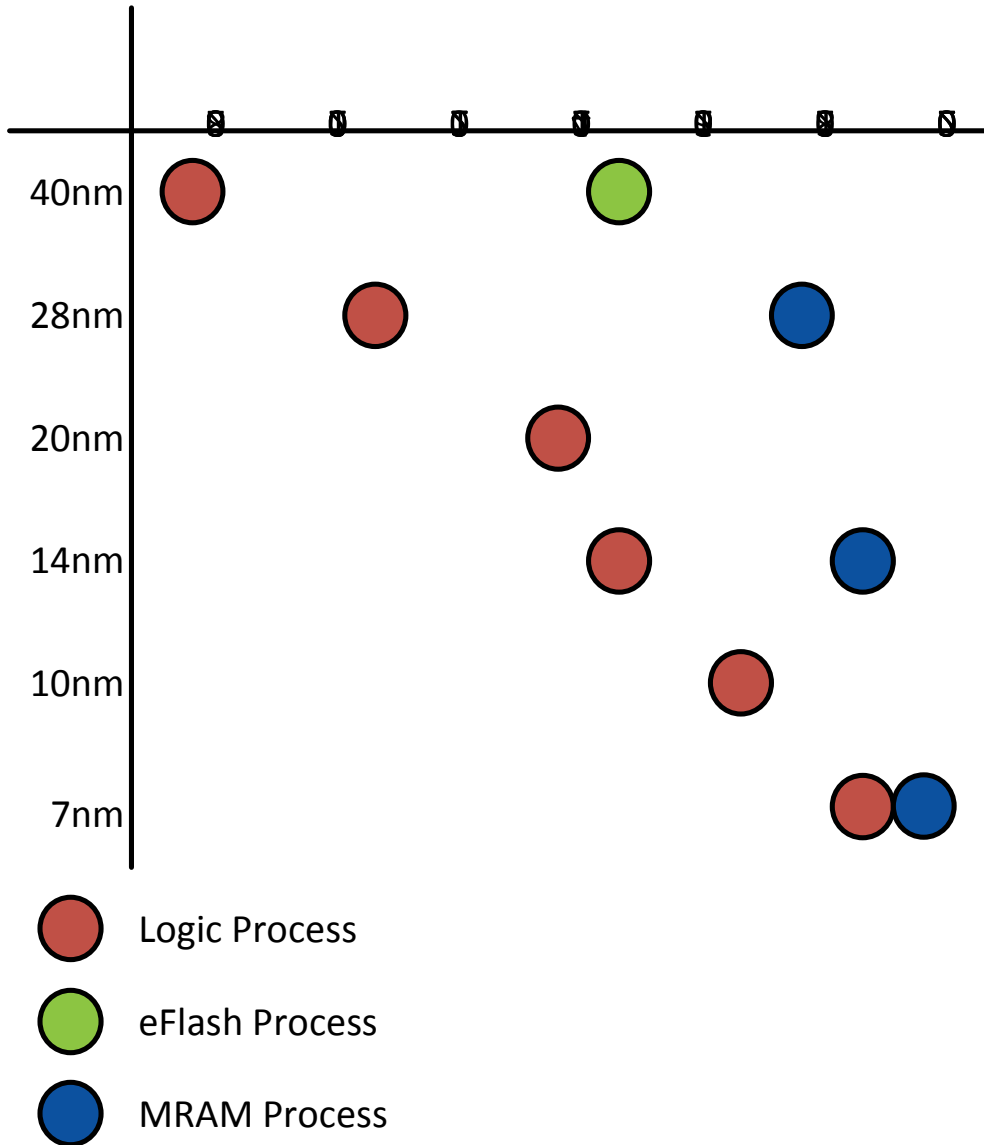


Performance Implications: MRAM v SRAM

- Store&Download Schemes Unnecessary
 - 2-4x Speed / Power of SRAM with no idle power
 - Savings can enable larger XIP area
- L3 Cache
 - Bit-Alterable design enables SRAM-type usage
 - No idle power
 - Area / Power savings can enable larger cache
- L2 Cache
 - IoT and other power sensitive applications will benefit
 - Performance differences will make this a tougher boundary to cross
- L1 Cache / Main SRAM
 - Low duty cycle applications (e.g. remote sensors)
 - "Instant On" valued over performance; NVM nature preserves state of cache when off
 - Limited application expected



Technology Availability



- eFlash has run ~3 technology generations behind logic
 - While some announcements have been made for 28nm eFlash, most foundries indicate that 40nm will be the last node
- MRAM will intersect on this same trend line, but accelerate from there
 - 2nd generation MRAM should shave 2-3 years off this trend
 - 3rd generation MRAM should be just 1 year behind the logic process

Closing

- 2018 will see the first broad availability of MRAM from major foundries
- Whether your priorities are cost, performance, or time to market, MRAM can enhance any SoC architecture
- Numem is ready to help companies lead in MRAM deployment
 - Over 45 years of experience in MRAM design
 - Leading edge density, performance, and power
 - Focus on helping customers bring their products to market

