Lower SoC Design Entry Barrier With RISC-V

以RISC-V核降低SoC设计的进入障碍

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总经理
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议程

- RISC-V为SoC设计带来新趋势
- Andes RISC-V 架构和 V5 AndesCore™处理器
- Andes V5处理器如何协助降低SoC设计的进入障碍
- 结语
An open processor architecture started by UC Berkeley
  • BSD license; David Patterson as an advisor
**RISC-V Foundation**: Formed in 2015 to govern its growth
A founding member of RISC-V Foundation
A major contributor to RISC-V tools, often as maintainer
Contributing architecture extensions
RISC-V worldwide promotion
Pushing RISC-V ecosystem forward with partners
Taking RISC-V mainstream:
  • To be a major application platform
Andes RISC-V 架构
和
V5 AndesCore™ 处理器
RISC-V:
- Concise (RV-I), Modular (RV-MACFD and more): good start
- Extensible: understanding that one size doesn’t fit all
- Profiles: no need to be compatible from MCU to servers

AndeStar™ V5 ISA architecture:
- Adopt RV-IMAC as its baseline
- Add basic performance extension instructions:
  - Path length reduction and further code size reduction (CoDense™)
- Add DSP/SIMD ext. based on GPR → P-extension proposal
- Provide custom-extension frameworks for DSA (or ASIP)
  - Powerful tool for SoC designers without CPU background

AndeStar™ V5 CSR extensions:
- Vectored PLIC with priority preemption → Fast interrupts proposal
- Stack protection mechanism (StackSafe™)
- Power throttling (PowerBrake)
- Cache management in finer granularity, write-back and write-thru
V5 AndesCores:25-系列Baseline处理器

- **N25: 32-bit, NX25: 64-bit**
  - From scratch for the best PPA
  - Very configurable

- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses

- **N25 sample configurations @TSMC 28HPC RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case)
  - Large config: 159K gates, 1.15GHz (worst case)
  - Best-in-class Coremark: 3.49/MHz
V5 AndesCores: 新25-系列处理器

► N25/NX25:
  - Fast-n-small for control tasks in AR/VR, networking, storage, AI

► N25F/NX25F: +FPU
  - +, −, ×, ×+, ×−: pipelined 4 cycles
  - ÷, √: run in the background
    −15 for SP, 29 for DP
  - FP load/store: support HP

► A25/AX25: +FP +Linux
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB

► Whetstone/MHz:
Andes V5处理器
如何协助降低SoC设计的进入障碍
- 电源管理
- DSP、SIMD提升媒体数据处理
- ACE加速DSA成功
- 开发环境
- 协议堆叠
- **PowerBrake** to digitally adjust power (via stalling pipeline)
- **QuickNap™**: logic power-down and SRAM in retention mode
  - Put dirty bits in tag SRAM instead of flops
  - Eliminate the need to flush data cache

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- **PowerBrake (frequency scaling)**
- **Clock off**
- **Minimum performance**
- **QuickNap™ (logic power-down and SRAM in retention)**
- **SRAM power-down**
- **Performance (frequency)**
- **Standby**
- **Dormant**
- **Shutdown**

**Power consumption**
Andes in RISC-V上的DSP/SIMD ISA的支持与特色

Background:
- >150 DSP ISA in the popular V3 processors D10 and D15
- Donated it as the basis for RV-P extension proposal (for RV32 & RV64)
- Ported CMSIS-NN and used CIFAR-10 for image classification:
  - Single-issue D10 is ~8% faster than a competing dual-issue core

Feature highlights:
- Efficient DSP based on existing GPRs
- Saturation and/or rounding
- Data types: integer (32b, 16b, 8b) and fractional (Q31, Q15, Q7)
- 16-bit and 8-bit SIMD instructions
- Most Sophisticated instructions: \( 64b += 16b \times 16b + 16b \times 16b \)

SW support:
- Compiler, intrinsic functions, >200 optimized DSP library functions

<table>
<thead>
<tr>
<th>Voice Codec</th>
<th>AMR-WB</th>
<th>G.729</th>
<th>Helix MP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encode</td>
<td>Decode</td>
<td>Encode</td>
<td>Decode</td>
</tr>
<tr>
<td>Speedup (over no DSP ISA)</td>
<td>&gt; 4x</td>
<td>&gt; 4x</td>
<td>&gt; 5x</td>
</tr>
</tbody>
</table>
Taking RISC-V Mainstream™

ACE框架

COPILOT
Custom-OPtimized Instruction deveLOpment Tools

- Extended Tools
- Extended ISS
- Extended RTL

Automated Env. For Cross Checking
Test Case Generator

- Compiler
  Asm/Disasm
  Debugger
  IDE
- CPU ISS
  (near-cycle accurate)
- CPU RTL

Concise RTL semantics, operands, test-case spec

script user.ace

Verilog user.v

Extensible Baseline Components

Executable or library

Source file
范例: 64个8-bit数据矢量的内积

```vhdl
reg CfReg { // Coef Registers
    num = 4;
    width = 512;
}

ram VMEM { // data memory
    interface = sram;
    address_bits = 3; // 8 elements
    width = 512;
}

insn innerp {
    operand = {out gpr IP,
                in CfReg C,
                in VMEM V};
    csim = %{
        // multi-precision lib. used
        IP = 0;
        for(uint i = 0; i < 64; ++i)
            IP += ((C >> (i*8)) & 0xff) * ((V >> (i*8)) & 0xff);
    };
    latency = 3; // enable multi-cycle ctrl
};

// ACE_BEGIN: innerp
assign IP = C[7:0] * V[7:0]
    + C[15:8] * V[15:8]
    ...
    + C[511:504] * V[511:504];
// ACE_END

Speedup: 85x

Intrinsic: long ace_innerp(CfReg_t, VMEM_t);
```
范例: CRC32 客制指令

<table>
<thead>
<tr>
<th>Mo...</th>
<th>InsC</th>
<th>CycC</th>
<th>Source Code</th>
<th>Line...</th>
<th>Instruction</th>
<th>I$Miss</th>
<th>D$Miss</th>
<th>BTB Miss</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>429</td>
<td>446</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>385</td>
<td>485</td>
<td>result = crc32_sw(Data);</td>
<td>46</td>
<td>addi a0,sp,12</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1,283</td>
<td>3,260</td>
<td></td>
<td>printf(&quot;CRC32 result = %x\n&quot;, result);</td>
<td>56</td>
<td>mv a1,a0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

162X Speedup

ACE Instruction

<table>
<thead>
<tr>
<th>Mo...</th>
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<th>D$Miss</th>
<th>BTB Miss</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>422</td>
<td>437</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>11</td>
<td>int main0 {</td>
<td>37</td>
<td>addi sp,sp,-16</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3</td>
<td>asm (&quot;nop&quot;);</td>
<td>50</td>
<td>nop</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3</td>
<td>result = ace_crc32(Data32);</td>
<td>52</td>
<td>lui a5,0x1020</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
AndeSight™: 专业的IDE

- Eclipse-based
- **Project Setup:**
  - Meta Linker Script Editor
  - Flash ISP configured through GUI
- **Debug Support:**
  - Script-Based RTOS Awareness
  - Virtual Hosting
  - Register Bitfield Viewing/Update
  - Break-n-Display on Exceptions
AndeSight™: 专业的IDE

- Program Analysis
  - Function Profiling
  - Performance Meter
  - Code Coverage
  - Function Code Size
  - (Static) Stack Size

- Debug/Analysis for Arduino

- Custom Plugin Intf
开发环境

► **AndeShape™ Development Boards**
  - Full-Featured ADP-XC7
  - Compact Corvette-F1 (Arduino-compatible)
    - With 802.15.4 and ICE on board

► **Qemu Virtual Board**
  - AX25 with AE350 SoC platform
  - Booted U-Boot and Linux
  - Used by openSUSE project for UEFI

► **AndeSoft™ SW Stack**
  - Bare metal projects for Andes-enhanced features
  - RTOS’es: FreeRTOS, ThreadX, Contiki, more
  - IoT Stack talking to the Cloud (next pages)

► **Special Support from 3rd Parties**
  - Imperas fast simulator
  - Trace32 debugger
  - UltraSoC trace support
Andes6 connectivity components

- Contiki RTOS for OS services
- An implementation of 6LoWPAN (IPv6 over 802.15.4)
- Commercial (e.g. InsideSecure) or open source TLS for security

Connecting to the Clouds (Microsoft Azure, Acer BYOC)
结语
晶心定位：全球领先的 RISC-V CPU IP 供货商

<table>
<thead>
<tr>
<th>Complete product portfolio</th>
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<tbody>
<tr>
<td>Reliable RISC-V core IP partner</td>
</tr>
<tr>
<td>RISC-V core that runs Linux</td>
</tr>
<tr>
<td>Extremely low power consumption, high computing efficiency</td>
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<tr>
<td>The leading RISC-V Cores capable of Custom Instruction Extension</td>
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RISC-V is emerging as a major application platform
RISC-V helps in lowering SoC design entry barrier
Andes offers comprehensive RISC-V solutions
  • V5 processors:
    – N25/NX25: Fast-n-small cores for control tasks
    – N25F/NX25F: FP cores for computation tasks such as AI and GPS
    – A25/AX25: Application Processors with high performance efficiency
  • ACE for AI or DSA Acceleration
    – A separate option available for all V5 cores
  • Rich development tools and SW stacks:
    – from Andes and partners

Experience and focus is very important for RISC-V

Andes is your best RISC-V partner!
谢谢！