



# Innovation in Design Service

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# 1

## Revolution in Business Model



# Paradigm Shift of the Semiconductor Industry

Before 1989 (Pre-PC ERA)

IDM (Integrated Device Manufacture)



System House

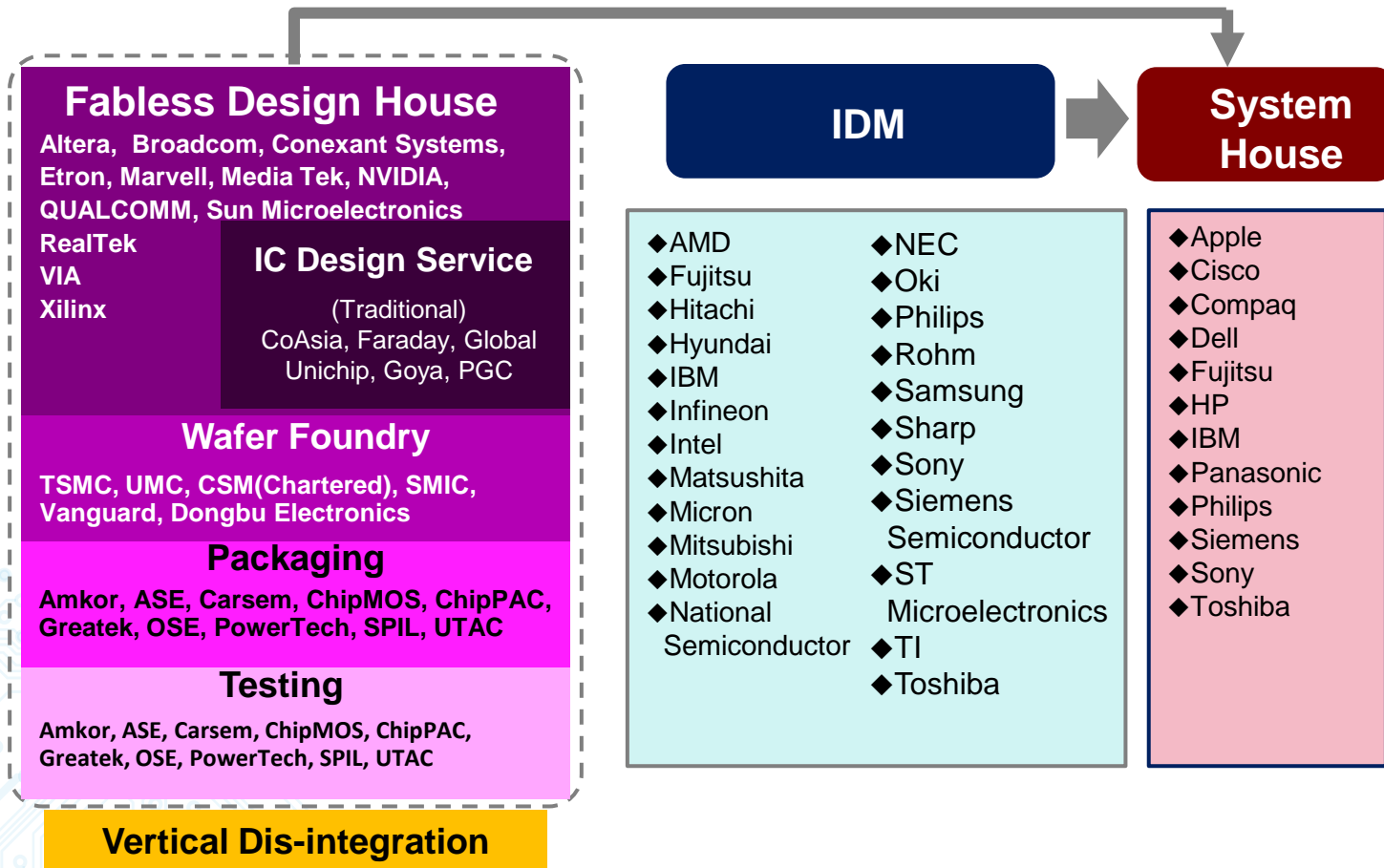
IC Definition  
Design Spec  
IC Design  
IC Fabrication  
Package  
Testing  
Sales & Support

◆ Fairchild Semiconductor	◆ Panasonic
◆ Fujitsu	◆ Philips
◆ Hitachi	◆ RCA
◆ IBM	◆ Siemens Semiconductor
◆ Intel	◆ SJ Thompson
◆ Mitsubishi	◆ TI
◆ Motorola	◆ Toshiba
◆ National Semiconductor	◆ Zilog
◆ Oki	

◆ Apple	◆ IBM
◆ Burroughs	◆ NCR
◆ Cisco	◆ Panasonic
◆ Compaq	◆ Philips
◆ Control Data Corp.	◆ Prime
◆ Data General	◆ Siemens
◆ Dell	◆ Sony
◆ Digital Equipment	◆ Sperry
◆ Fujitsu	◆ Toshiba
◆ General Micro Electronics	◆ Univac
◆ Honeywell	◆ Wang Labs
◆ HP	

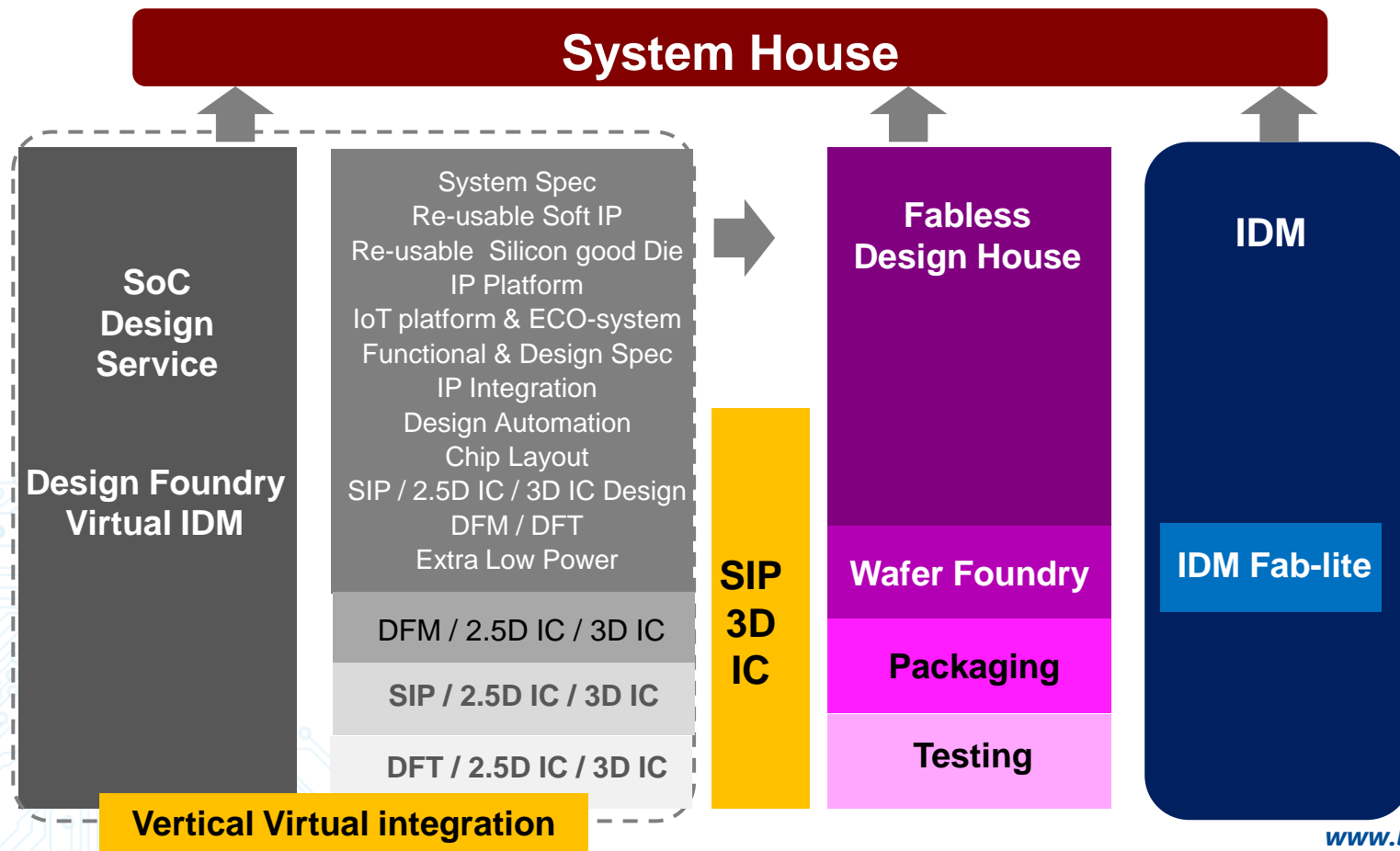
# Paradigm Shift of the Semiconductor Industry

1990-2000 PC ERA



# Paradigm Shift of the Semiconductor Industry

2013~ New SoC / IoT ERA



- More and more SoC will rely on KGD/3DIC to achieve the needed upgrade than pure process advancement.
- Silicon IPs will exist both as soft-core and KGD.
- Most Fabless and System Co. can not afford the heavy investment for in house 3DIC capability , but turn to SoC Design Service Co. who possess the 3DIC capability for design support.
- Design Lite Era (for Fabless and System House) is now begin to become reality.

**Fab- Lite**



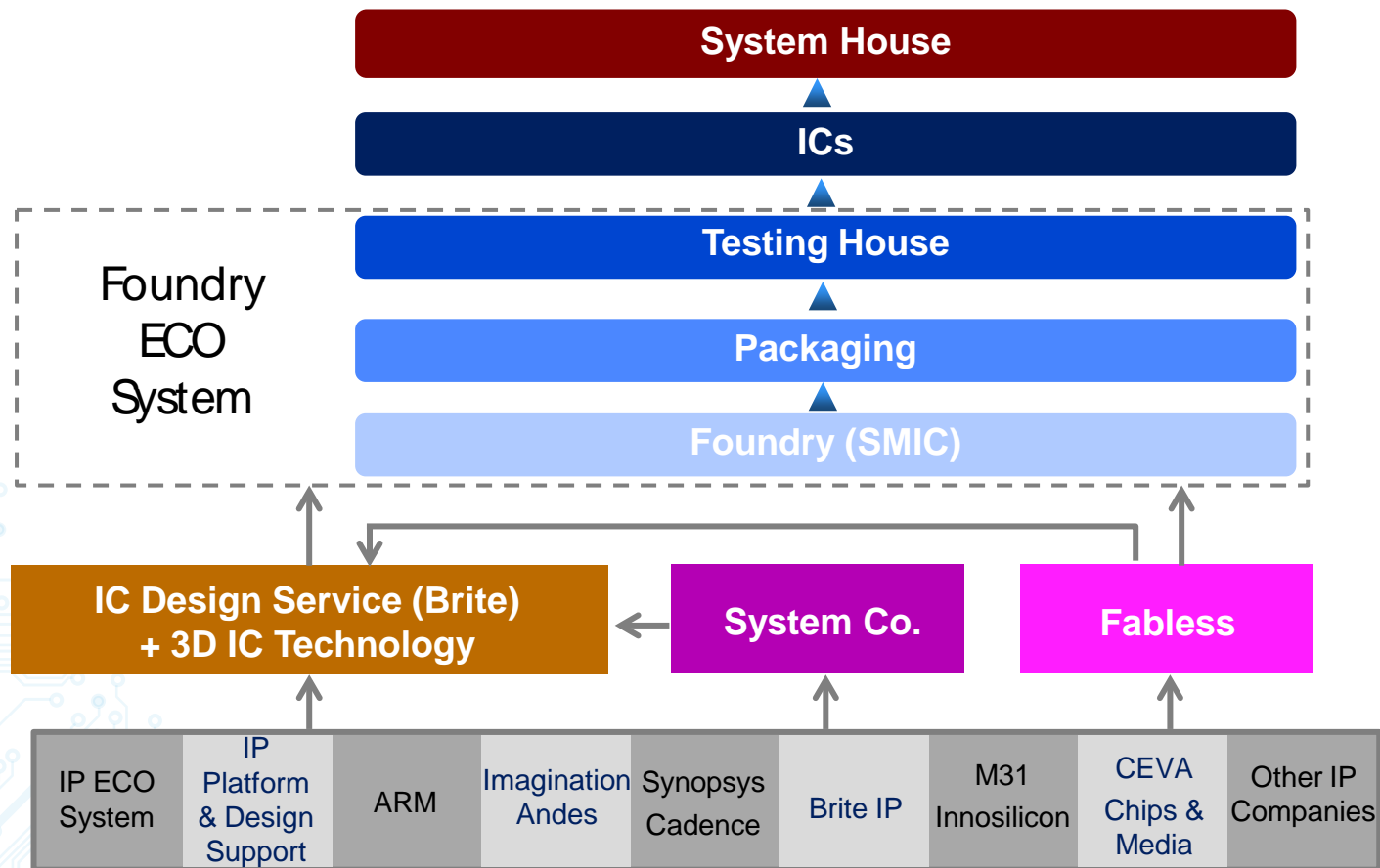
**Design- Lite**

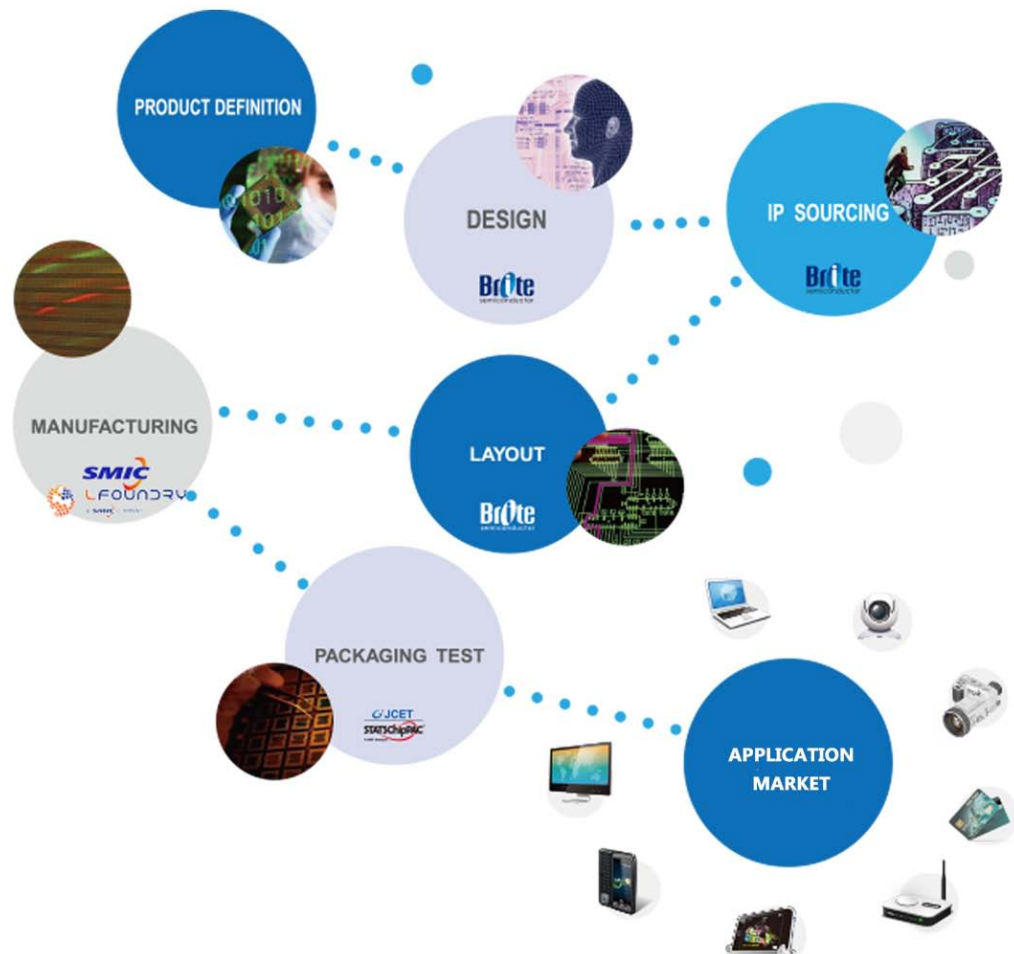


# 2

## Trusted Eco-System





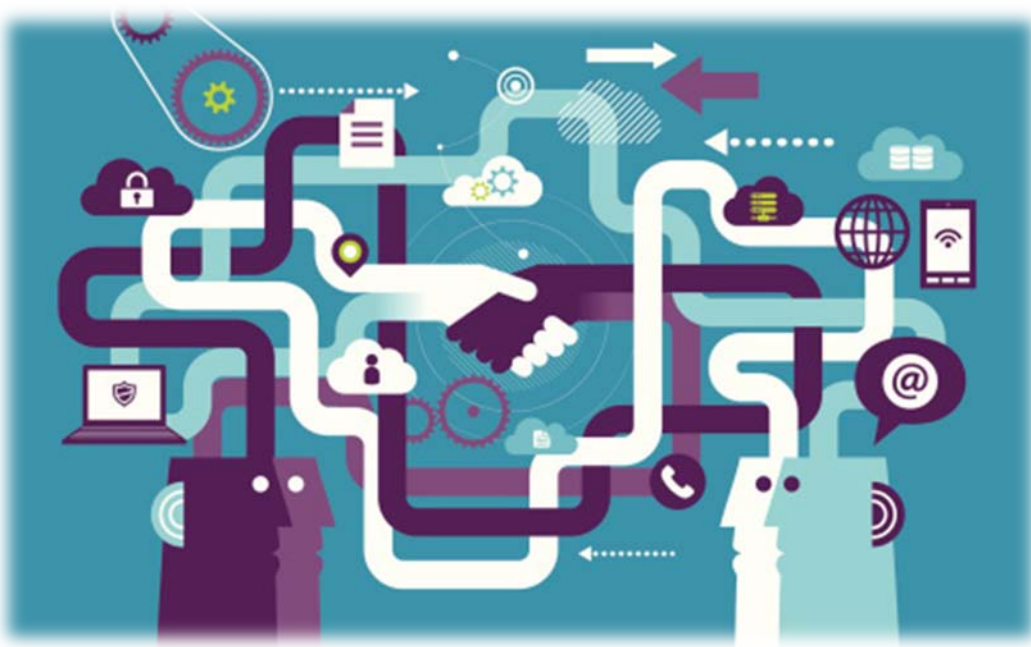


## Strong support from SMIC + LFoundry beyond Brite

- Price
- Capacity
- Cycle Time
- Yield & Quality Control
- Service & Supporting
- Assurance



**BritelP**



# 3

## **Brite's Offerings: Design Flows, IPs, Platforms**

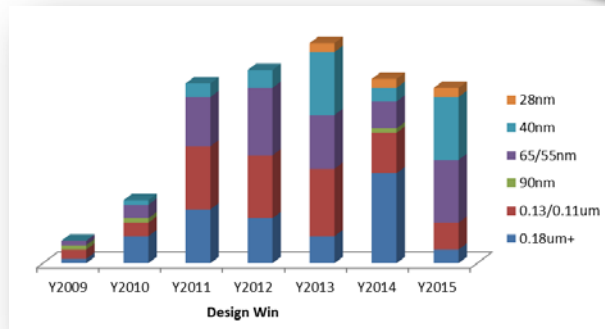


# Who is Brite?

Design Service Company  
Founded in 2008 with VC from  
Silicon valley

Major shareholder : **SMIC**

**130+** Employees (80% are R&D)



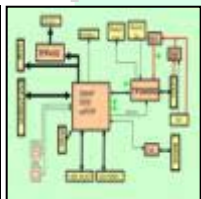
**>240** design wins in 6 years  
Projects focus on the advance process  
node (<65nm)

We provide ASIC design services and  
ARM CPU ,CEVA DSP and SNPS ARC  
based SoC platform.

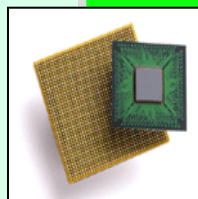
# Total Solution : OEM+ODM



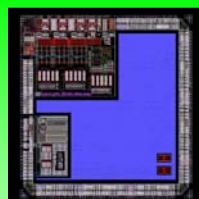
Product  
Specification



Architecture &  
RTL Design



IP Selection &  
Integration



IC Physical  
Design



Wafer  
Fabrication



Package and  
Assembly



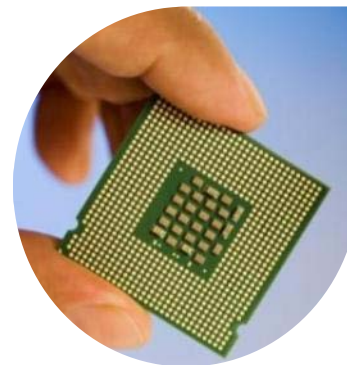
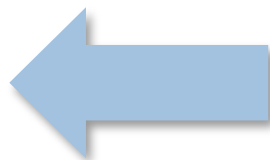
Test & Prod  
Engineering



Prod &  
Logistics



SDK Development



## Tape out & Manufacturing Services

- GDS in
- Mask in and production management

## IP Procurement & Customization Services

- Internal development
- Partnership
- Customer Driven

## ASIC Turn-Key & SoC Services

- Spec/RTL/Netlist to Silicon, complete hardware service
- Porting/Shrinking from an existing product to a derivative product, from other FAB to SMIC

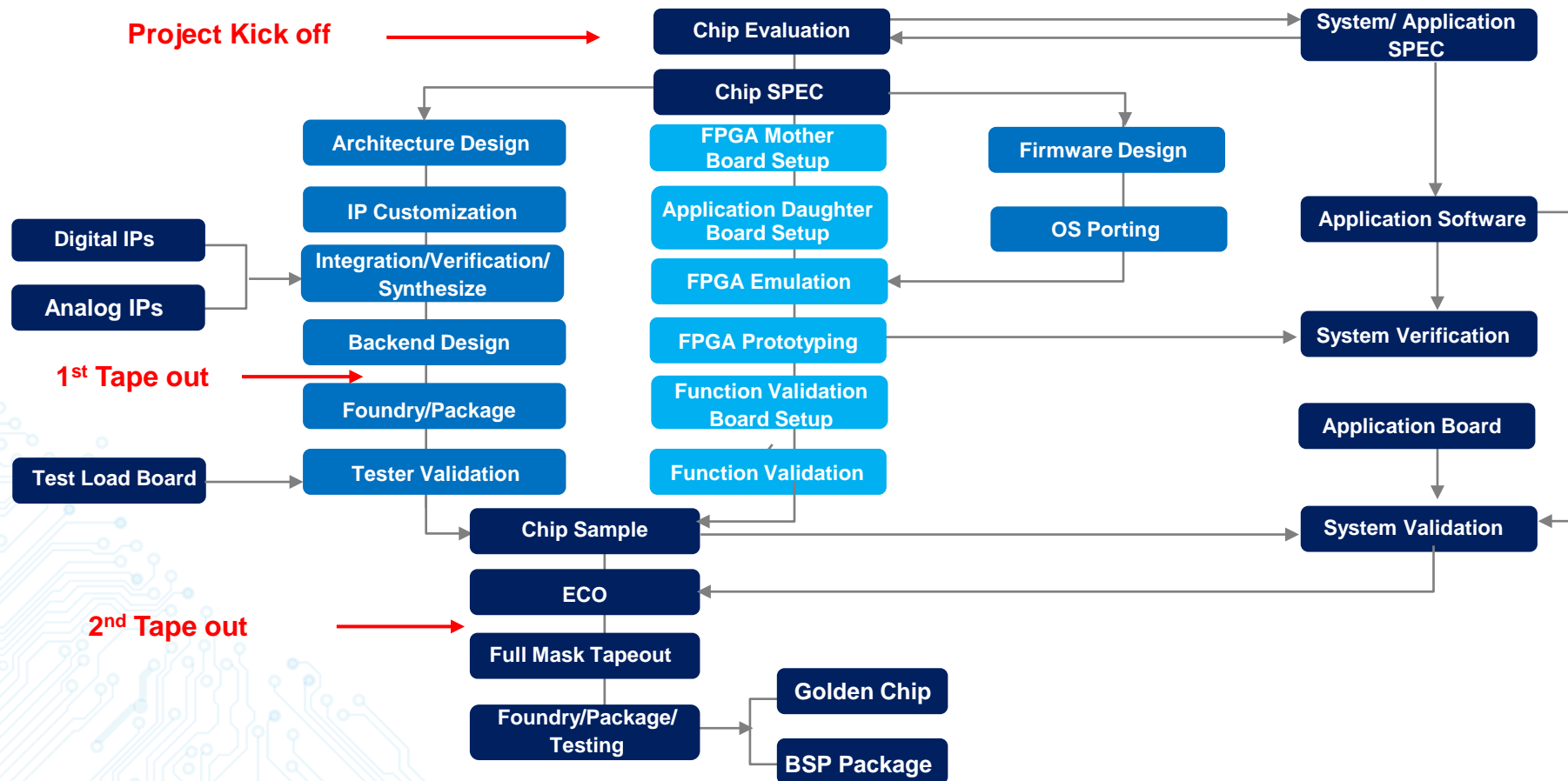
## System Integration Services

- ARM Core based system integration
- CEVA/Cadence DSP Core based system integration
- Synopsys Core based system integration

## As an important part of SMIC eco-system & a bridge to the China markets

- Platform development
- Design porting
- PDK QA & IP QA

# SOC Flow to System House





## IC-ONE

An ecosystem for IP management, SOC design flow and big data application platforms



### IP management

Build, track, reuse IP



### Smart plug-In for EDA

Knowledge tree



### PPA Evaluation

Base on spec. to evaluate PPA



### IP reuse

Library setup file auto generation  
IP version control  
Supported IP reuse in SOC design



### Transparent visualization of project details

Data mining application in SOC design  
Data visualization



### Advanced tech. solutions

Web application  
Support MySQL, sqLite database  
Platform architecture effectively supports sustainable development



### Project management

Project registration  
Library info registration  
Project workflow management



### Push button retrieval

Smart push button retrieve for project experience and smart reuse.



### Benign ecosystem

The architecture design takes IP management, IP reuse and SOC design into consideration and forms closed cycle.

## CUSTOMER

Production / Shipping Instruction

Real Time WIP Report

### Mass Production Management & Logistics Flow

Mask  
Tooling

Wafer  
Fabrication

Bumping  
(flip chip)

Wafer  
Probing

Assembly

Final  
Test

Packing &  
Drop Ship

### Quality and Yield Management

Planning & PO

WIP Monitoring

Shipping & Delivery

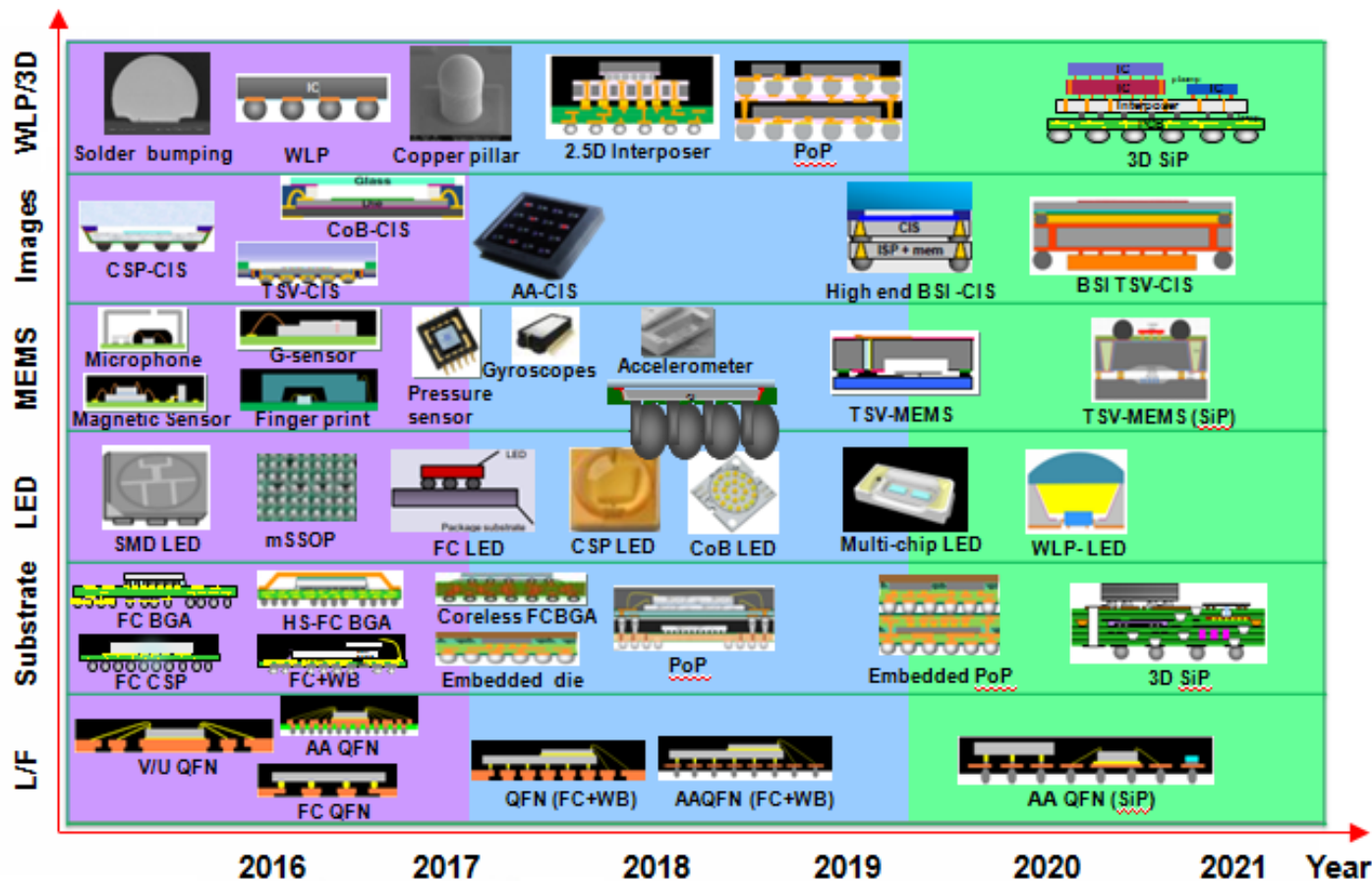
Custom Clearance

Yield Improvement

Cost Reduction

## SUPPLIERS

# Brite New SiP Roadmap



<b>Std Cell/ Memory/IO</b>	<b>Cell Library</b> 0.35um-28nm 0.25um-90nm	<b>Memory Compiler</b> 0.18um-28nm 0.25um-28nm	<b>Std. IO</b> 0.35um-28nm 0.25um-0.11um	<b>SDIO</b> 0.11um-28nm 0.13um-40nm		
<b>Fundamental IP</b>	<b>Regulator</b> 0.18um-28nm 0.13um-40nm 0.11um-40nm,95nm ULP	<b>DC/DC</b> 0.18um-55nm,95ULP 0.13um-55nm 55nm,95ULP	<b>Cap-less LDO</b> 0.18um-28nm 0.13um-55nm 55nm,95ULP	<b>Power On Reset</b> 0.18um-28nm 0.13um 55nm EF	<b>Crystal OSC</b> 0.18um-28nm 0.11um-40nm 0.11um 55nm	<b>Temp.Sensor</b> 95nm ULP,55nm 55nm-28nm 95nm ULP
	<b>Frac./SS/PLL</b> 0.18um-40nm 0.18um-28nm	<b>Comparator</b> 95nm ULP,55nm 55nm EF	<b>Ring OSC</b> 0.18um-55nm 40nm,55nm	<b>Amplifier/PGA</b> 95nm ULP	<b>DLL</b> 0.13um-55nm	<b>Analog Filter</b> 0.18um-0.13um
<b>ADC/DAC</b>	<b>SD ADC</b> 0.35um-28nm 0.18um-28nm 55nm,40nm,95ULP	<b>SAR ADC</b> 0.35-28nm 0.13um-28nm 95ULP	<b>Pipeline ADC</b> 0.18um-65nm 0.13um-28nm	<b>Audio/Video DAC</b> 0.18um-28nm 0.18um-28nm 0.13um-55nm,40nm,95ULP	<b>Baseband/ WLAN AFE</b> 0.18um-65nm	<b>Audio DAC/ Codec</b> 0.18um-28nm 0.18um-28nm
<b>HS Interface</b>	<b>USB3.0/OTG</b> 0.13um-28nm 28nm HK	<b>USB2.0/OTG</b> 0.13um-28nm 0.13um-28nm	<b>LPDDR1/2/3/4</b> 65nm-28nm 65nm-28nm 0.13um-28nm	<b>DDR2/3/4</b> 65nm-28nm 65nm-28nm 0.13um-28nm	<b>PCIe Gen 1/2/3/4</b> 65nm-28nm 28nm	<b>LVDS</b> 0.18-28nm 0.13um-40nm 40nm
	<b>MIPI DSI TX</b> 0.13um-28nm	<b>HDMI1.4</b> 0.18um-28nm	<b>Display Port</b> 40nm-28nm	<b>SATA II/III</b> 0.65um-28nm	<b>Ethernet</b> 55nm-28nm	<b>SerDes (up to 16G)</b> 40nm-28nm 40nm-28nm
<b>CPU Solution</b>	<b>ARM Cortex A53</b> 28nm PS 1.3GHz	<b>ARM Cortex A7</b> 40nm 1.1GHz	<b>ARM Cortex A9</b> 40nm 1.3GHz	<b>ARM Cortex M0/M0+</b> 0.13um EF	<b>CEVA TL421</b> 55nm	
	<b>CEVA XM4 Quad Core</b> 40nm-28nm	<b>CEVA DSP Core</b> MM3101,X1643,TL420,etc.	<b>AXI/AHB/APB/Arbiter/Bridge</b> 0.18um-28nm		<b>Digital Peripherals</b> 0.18-28nm	

 SMIC  
 The other third parties  
 Brite with customization service



## Brite YouIP family

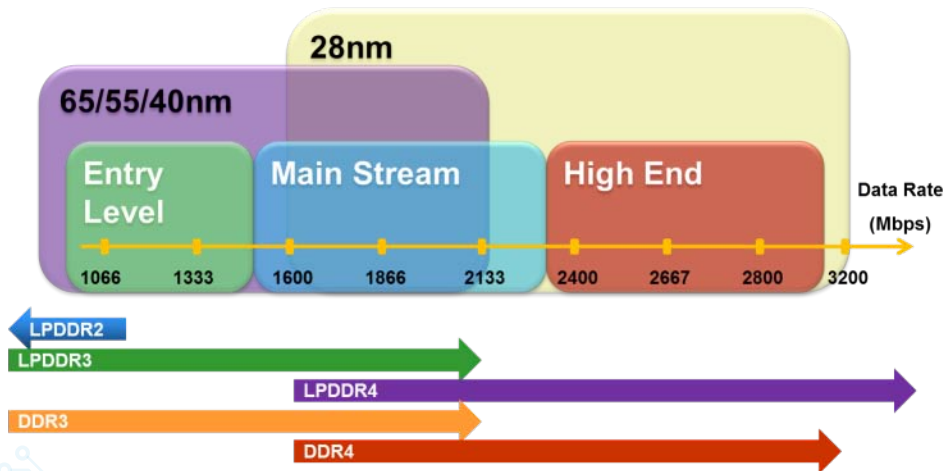
- **YouIP consists of 4 branches:**
  - YouPHY
  - YouRF
  - YouSiP
  - YouAnalog
- **YouSiP (silicon platform) includes:**
  - YouSiP-Audio
  - YouSiP-Vision
  - YouSiP-AP
  - YouSiP-IoT
  - YouSiP-IoM
- **Each platform is launched through silicon validated and product-like application proven**

IP type	IP name	Description	Bits	Speed (MSPS)	Speed (KSPS)	Frequency (MHz)	Data Rate Mbps	Power Sub (V)	Process	Status
ADC	B40NLL_PIPADC_12B170M	12bit 170MSps Pipelined ADC	12	170				1.1V	SMIC40	Silicon Proven
	B28HK_SARADC_12B125M	12bit 125MSps High Speed SAR ADC	12	125				0.9V	SMIC28	Silicon Proven
DAC	B40NLL_DAC_10B300M4CH	10bit 300MSps 4-Channel Video DAC	10	300				3.3V/1.1V	SMIC40	Silicon Proven
AFE	B40NLL_TPAFE_12B200K	Driver and digitizer for 4-wire or 5-wire resistive Touch Panel integrating 12bit SAR ADC	12	0.2				3.3V/1.1V	SMIC40	Mass Production
PLL	B55NLL_PLL_SSCG1P2G	Low Jitter Spread-Spectrum Clock Generator (SSCG)				VCO=200~1200 OUT=12.5~1200		1.2V	SMIC65/55	Mass Production
Audio Codec	B55NLL_AUDCODEC	Stereo ADC, Stereo DAC, Output Power Amplifier	ADC=16 DAC=24		8~96			3.3V/1.2V	SMIC65/55	Mass Production
LVDS TX	B40NLL_LVDS_TX1P05G	high speed LVDS transmitter used for digital flat panel display systems					25~150 @CLK=25~150 1050 @throughput	3.3V/1.2V	SMIC40	Mass Production

Brite provides a complete DDR subsystem including not only controller, PHY and IO, also corresponding tuning and configuration software.

YouPHY-DDR is developed on 130um to 28nm process respectively and support LPDDR2, DDR3, LPDDR3, DDR4 and LPDDR4 combo PHY with the data rate from 667Mbps to 2933Mbps.

With patented dynamic self-calibrating logic (DSCL) and dynamic adaptive bit calibration (DABC) technology, YouPHY-DDR can automatically compensate chip/package/board/memory PVT variation and bit-bit skew.

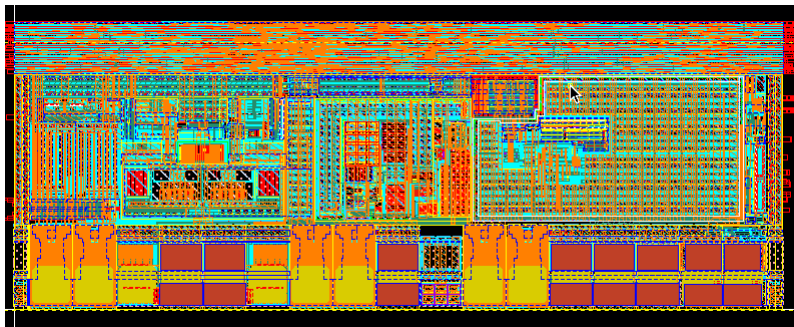


YouPHY-DDR Solution

Brite provides USB2.0 OTG PHY which is a complete mixed-signal IP solution designed to implement OTG connectivity for a System-on-Chip (SoC) design.

The USB2.0 OTG PHY supports the USB2.0 480Mbps protocol and data rate, and is backward compatible with the USB 1.1 1.5Mbps and 12Mbps protocol and data rates.

This solution can be adapted from 130nm to 28nm process. It has been verified by a number of end products, especially suitable for the internet of things(IoT) applications.

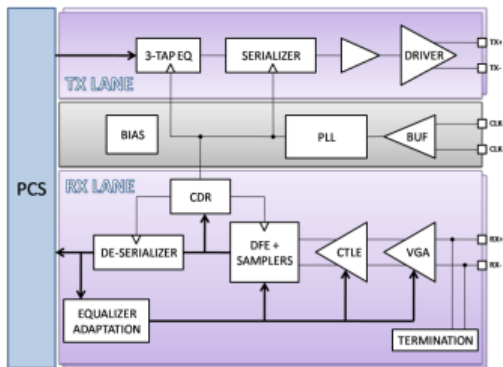


**USB2.0 OTG PHY**

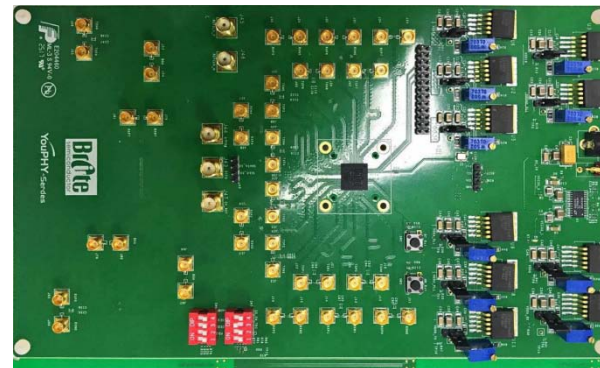


YouPHY-Serdes provides 1.25-12.5Gbps multi-rate SERDES IP which is designed for smooth integration of multiple SERDES lanes offering best in class performance, area and power.

The programmable PHY supports major standards such as PCIe Gen 1/2/3, USB 3.0 / 3.1, XAUI, SATA Gen 1/2/3, CEI-11G-LR, 10GBase-KX4, JESD204B, SGMII/QSGMII, RAPID I/O, HSSTP (Trace Port), V-By-One, DisplayPort and HMC, based on advanced process as 40nm and 28nm.



**YouPHY-Serdes Subsystem**

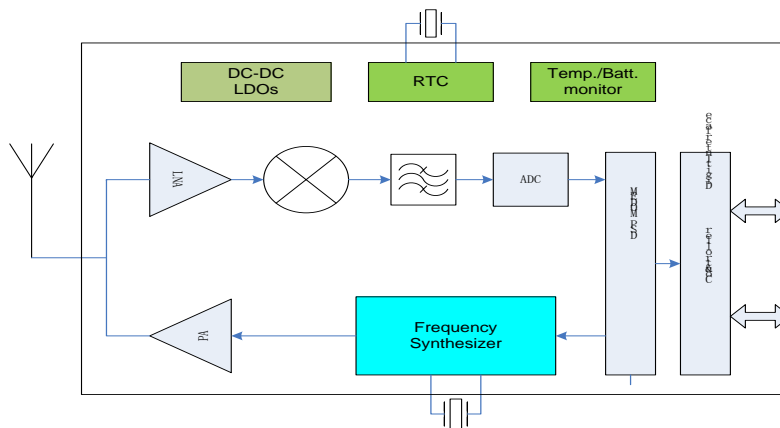


**YouPHY-Serdes Demo Board**

Brite provides a complete Bluetooth Low Energy (BLE) analog PHY.

The RF is a high performance 2.4GHz ISM band wireless transceiver. It integrates high sensitivity receivers, 5G PLL and high efficiency power amplifier, which can support 1Mbps GFSK modulation and demodulation. And can be combined with the Bluetooth smart baseband and controller to form a complete Bluetooth Smart solution.

YouRF-BLE is developed on SMIC 55nm LL process, support 0.9V-4.3V supply voltage with on-chip Buck-Boost DC/DC converter and LDOs, Low power consumption: RX<10mW; TX<12mW @0dBm



YouRF-BLE Block Diagram

YouSiP-Audio is developed based on the CEVA-TeakLite-4 DSP core and fabricated at SMIC's 55nmLP process, running up to 500MHz.

The platform provides designers with a powerful means to add 'smart and connected' capabilities to these devices, including always-on sensing, local processing and intelligence connectivity. The platform also provides real-time power measurement that allows developers to improve power consumption of system by optimizing their DSP software effectively.

It provides a complete development and demo system integrating DSP and multiple peripherals & interfaces IP, and supports diverse wireless technologies including Bluetooth Smart and Smart Ready, Wi-Fi, ZigBee and GNSS. It can be adopted on mobile, wearable, wireless speaker, smart home, surveillance, automotive and so on.



Voice Activated Audio Player DEMO

听不听话，您来说

触发 + 指令 (always-listening)

- ✓ OK CEVA + Play Music
- ✓ OK CEVA + Stop Music
- ✓ OK CEVA + Next Song
- ✓ OK CEVA + Previous Song



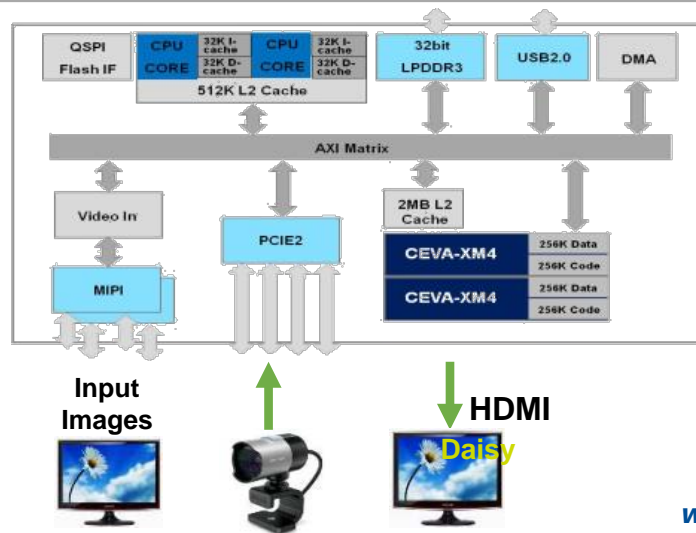
YouSiP-Vision is an image signal processor (ISP) platform integrated with CEVA XM4, and some high speed interface IPs as MIPI, PCIe, LPDDR3 and USB which is developed based on SMIC 28nm, 40nm process.

It can support 3D vision including real-time 3D depth map generation and point cloud processing for 3D scanning, computational photography algorithms including refocus, background replacement, zoom, super-resolution, image stabilization, HDR, noise reduction and improved low-light capabilities, visual perception including deep learning, object detection, recognition & tracking, context aware, augmented reality(AR) and others.

This platform targets any camera-enabled devices such as smartphones, tablets, ADAS and infotainment, robotics, security and surveillance, AR/VR and drones.



Real-Time CNN Object Recognition Demo



YouSiP-IoT platform can assist customer to reduce the processing delay time, enhance the data security, improve the data rate and reduce power consumption of their SoC design, which is adopted in battery power supply environment as smart home, IoT and wearable devices with excellent low power management.



**[www.britesemi.com](http://www.britesemi.com)**

YouSiP-AP(Application Processor) provides an ARM Cortex-A series core architecture based SoC platform prototype which has been verified on SMIC 28nm and 40nm process.

Complete development tool including ISP/ICP tools, development boards, reference code and programmer and peripheral IPs can be offered to customer, enabling customer to achieve SoC product with shorter time to market and higher one time delivery rate, and assisting them win the emerging market opportunities in the field of industrial control, home appliance, security, toys, mobile devices, etc.



**A9 FPGA Development Board**



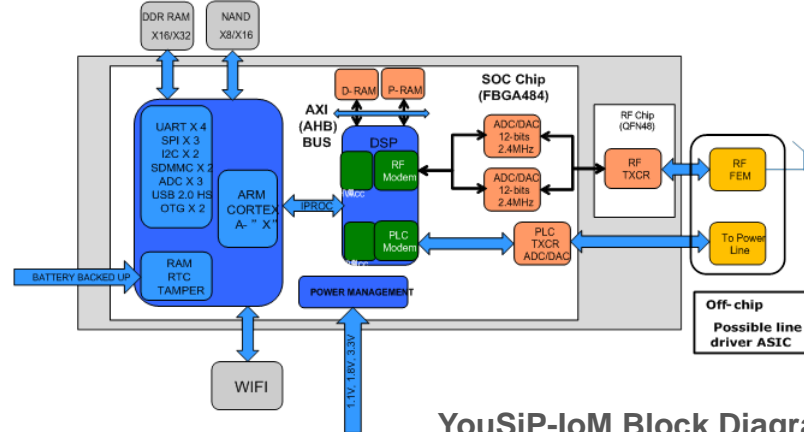
**A9 Chip Testing Board**



YouSiP-IoM(Internet of Meter) is an innovative interconnection SoC solution with SMIC 40nm LL process for smart meters.

YouSiP-IoM based on ARM Cortex A7 and Cadence Tensilica LX6 DSP architecture. Multiply transmission interface IPs are integrated to support industrial level wire and wireless connection as PLC, IEEE 802.15.4g and WiFi which can bring intelligent and connection to smart water, electricity and gas meters.

Abundant peripheral interface containing NAND Flash, LPDDR1/2, SD/MMC, USB 2.0 OTG, UART, SPI, I2C and RTC enable designer to extend sensing function and smart measuring technology and adapt product on various emerging applications and systems.



YouSiP-IoM Block Diagram

# 4

## Summary



- ✓ A close partner of SMIC/L Foundry and JCET, a bridge for supply chain localization on China
- ✓ Flexible business models and assist customer to shorter system to IC
- ✓ Complete offerings in platform, IP, design, and manufacturing as a one-stop service.
- ✓ High quality and on time delivery control

Your desired and trusted  
turkey solution partner!





*A World-Leading ASIC Design Solution Provider*

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