IP vs. Chiplets

SOC Disintegration Trend at Deep FinFET Submicron

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SOC Disintegration at Deep FinFET Submicron - Chiplets
SOC to Chiplet – The Economics

▲ Higher cost per gate below 28 nm HKMG bulk

![Gate Cost Trend](image)

▲ Advantages of “SOC” composed by chiplets
- Components reuse, enable multiple variations
- Mixed process technology
- Simplify “SOC” design, faster time to market
- Reduce “SOC” Cost

Source: IBS
Industry Leaders Building Chiplet Enabling Technology

News & Analysis
Intel Aims to Drive Chiplet Standard
PHY spec to be released within weeks
Rick Merritt
7/26/2018 00:01 AM EDT
2 comments

SAN FRANCISCO — Intel is weeks away from releasing a small but strategic piece of its proprietary packaging technology. It could become part of a future standard enabling a Lego-like design of SoCs out of chiplets.

The x86 giant is putting the final touches on a specification for its Advanced Interface Bus (AIB). AIB is a physical-layer block for the die-to-die connection in its dense, low-cost Embedded Multi-Die Interconnect Bridge (EMIB).
Back To The Future!

Specific Function Chips  \rightarrow  SOC  \rightarrow  Chiplets – Virtual SOC

VeriSilicon
VeriSilicon IP Portfolio

- Neural Network AI
- Compute
- GPU
- ISP
- Video
- Audio/Voice
- Compression/Encryption
- DISPLAY

Server Class

Automotive

Tablets

Smartphone

Wearables & IoT

Compression/Encryption
VeriSilicon Technology in Edge Device, Edge Server and Cloud

Cloud, Data Center

Video Transcoding
Pixel Compression
High Performance Computing

Surveillance
AR/VR Wearables
Smart Home, Vision, Voice
Automotive

Edge Server

Edge Server

Edge Server
Lego of Chiplets

Processor Chiplets

Clock and ResetControl

DDR PHY

Gen3x4

PCIe Controller

APB

AXI4

AHB

64b

32b

2x32b

64b

32b

PL

LS

System Controller

Processor

Mix Chiplets in a solution

Video

Vision/AI

Compute

GPU

ISP

Scale up performance with Chiplets

Vision/AI

Video

GPU

GPU

ISP
Subsystem IP – Pixel Compression & Encryption

Host Block

Register Access Masters

Nonsec

Secure

DDR Access Slaves

Nonsecure Registers

Secure Registers

FIFO

Line Buffer

Compression Pipe

Compression Pipe

Bypass

DEC800

MMU

IED Pipe

MUX

Bypass
Subsystem IP - AI Deep Integration

Smart Sensors
- cell phone, car back camera
- ISP8000
- VIPNano AI

Smart Home, talking device
- Voice ZSP
- VIPPico AI

Intelligent Surveillance Camera Solution
- VISION/AI VIP8000
- Video Encoder VC8000

Compute/AR/VR Solution
- AI GPU/Compute GC8000VX + VIP8000
AI is Everywhere, AI Needs to be Build into Subsystem IP

- Natural User Interface
  - AI VISION
  - AI VOICE
  - AI Sensors

- Multi-Media
  - Graphics, Video, Audio, Voice
GLASS TO GLASS INTELLIGENT PIXEL PROCESSING
The Trend and The Need

The Trend

SOC ➔ Virtual SOC

The Need

Subsystem IP

IP vs. Chiplets