I-fuse™: Dream OTP Comes True
创新熔絲™：美梦成真

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OTP IP: Dream Comes True

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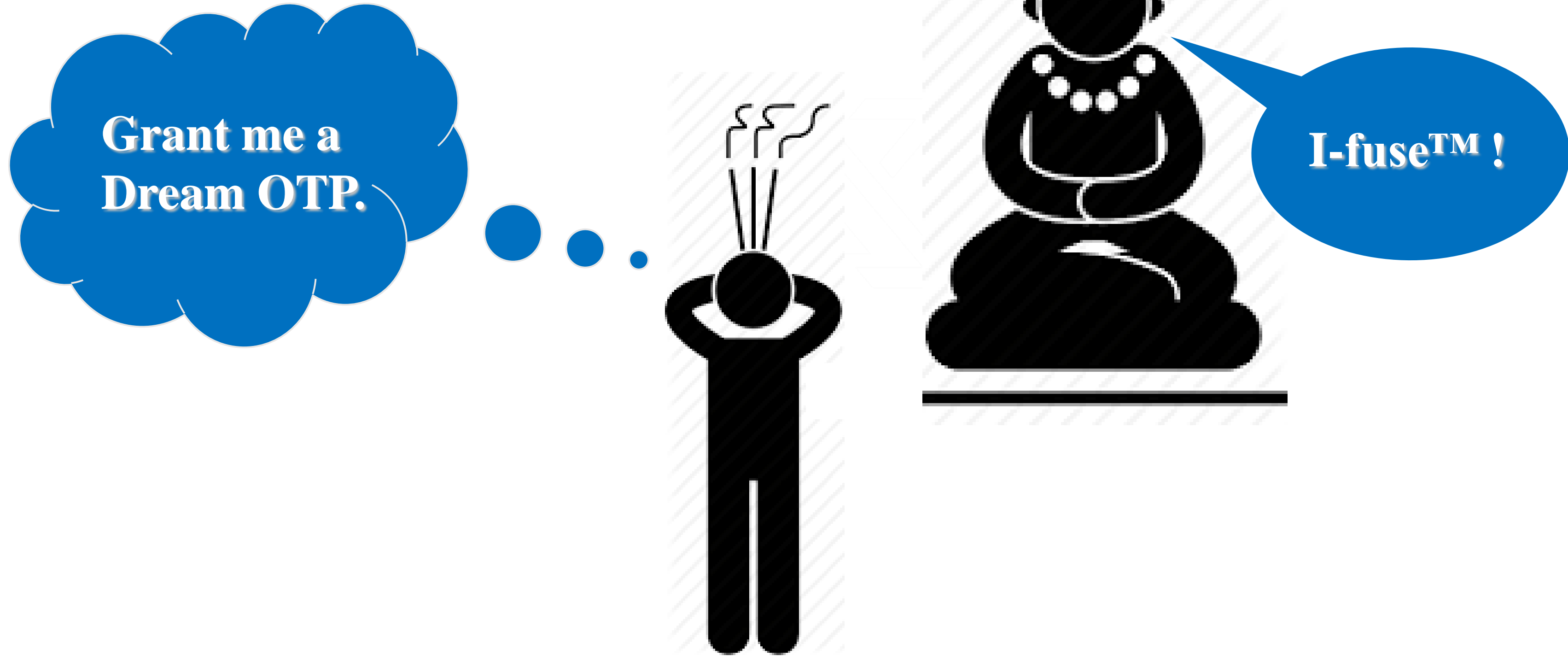


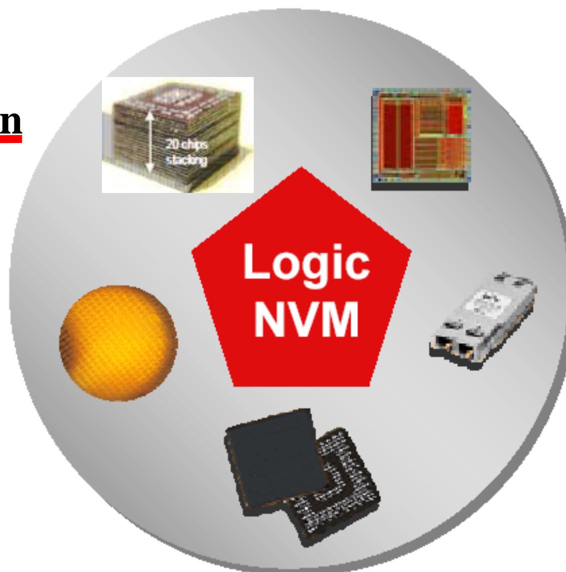
OTP: One-Time Programmable

OTP Applications

- OTP: a memory IP programmable only once to keep data permanent
- OTP allows each IC to be modified after fabrication without any costs
  - Customize data, fix defects, and trim statistic variations, etc.

Product feature selection

MCU code storage
(replace flash)



3D IC repair
Memory redundancy
(replace laser fuse)

Device trimming / calibration
(eliminate EEPROM)

Chip ID, Security Key, IoT

Defying Conventional OTP Wisdom….

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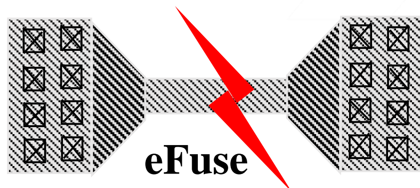
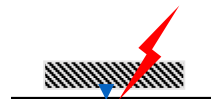
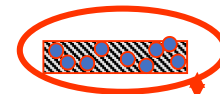
- OTP: NVM mechanisms
  - Break fuse, Rupture oxide, or trap charges in floating gates
- Revolutionary I-fuse™: True logic device
  - Non-breaking I-fuse™ prevails breaking eFuse
  - Best OTP in size, PGM/read voltage/current, temperature, reliability, testability

I-fuse™	 eFuse	 Anti-fuse	 Floating-gate
Non-break fuse	Break fuse	Rupture oxide	Trap charges
Deterministic	Explosive	Explosive	Statistical
≦0.6um	≦0.18um	≦ 0.18um, ≧14nm	≧0.35um, ≦ 0.6um
<0.01ppm defect	29ppm defect	10ppm defect	100ppm defect
No problem	Grow back	Self-healed	data retention

I-fuse™: Best OTP Figure of Merit

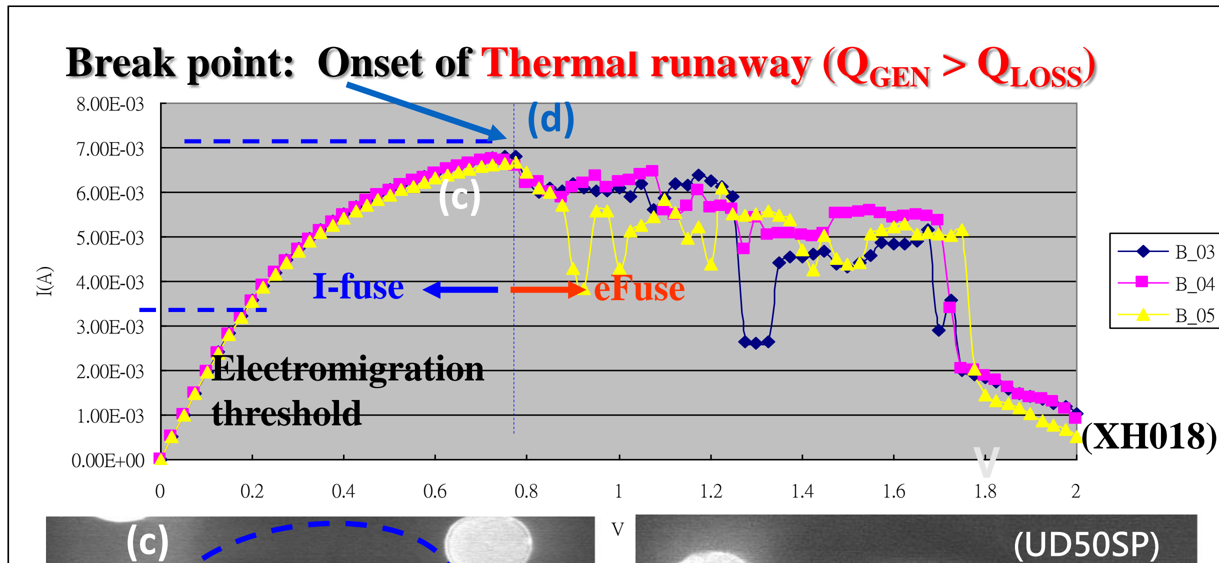
Foundry independent	*No mask/step; no hidden layers
Program mechanism	*True electromigration; based on physics
Small size	*No charge pumps; low PGM current
Robust OTP tech	*PGM resistor, not MOS
Low PGM voltage	*Current programming, not voltage
Low read voltage	*No HV device; sub-VDD readable
Low read current	*Logic device sensing; for energy harvest
Wide temperature	*Less damage to fuse; for automotive
High reliability	*Program below thermal runaway
Full testability	*Non-destructive PGM state for thorough tests
High data security	*Less damage; unhackable OTP key in stdcell lib
Short PGM time	*No read-verified write; temp-assist EM

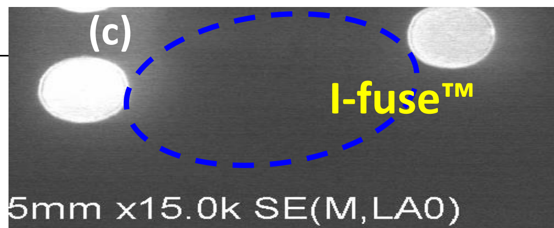
- Applications: AI, IoT, Automotive, Industrial, communication

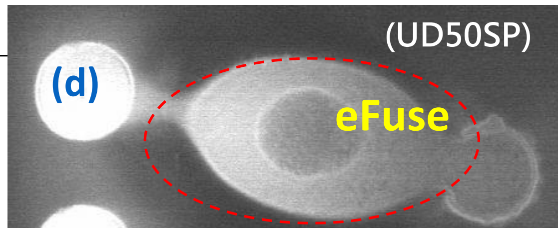
The only OTP programming mechanism can be modeled by physics: heat generation, heat dissipation and electro-migration

I-Fuse™ vs. Efuse Programming

- I-fuse™: non-explosive fuse; Guaranteed reliable by physics
- eFuse: explosive fuse => create debris => grow back







Power devices should not operate in thermal runaway.

So shouldn't programming a fuse this way.

I-Fuse™, eFuse, and Anti-Fuse (AF)

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- I-fuse™ at 22nm (Attopsemi, IEEE S3S conf., 2017-2019)
  - 256Kb programmed w/1.0V, 1.0mA, for 1-10us, 0.788um2 cell, AE=50%
  - Pass 250°C HTS for 1Khr (PR w/GF, Nov. '18, IEEE S3S '19)
  - 0.4V/1uA read for battery-less IoT (PR w/GF, Nov. '18, IEEE S3S '19)
- Efuse
  - @28nm, UMC, Cu fuse (IEEE IITC/MAM 2011)
    - Need >30mA to program
    - Hard to pass @150oC HSTL for 168hr
  - @28nm Intel, metal fuse (IEEE JSSC 4/2010, VLSI Cir Symp. 2009)
    - "read current is only 1/250 of program current". 100uA =>25mA
  - @22nm FinFET Intel, metal fuse (VLSI Tech Symp. 2015)
    - 16.34um2 cell, charge pump,1.6V PGM, 50us, 5x16 array, 0.9V read.
- Anti-Fuse (oxide breakdown)
  - @40nm need 5V (G), 6.25V (LP) to program (Kilopass, MPR 6/2010)
  - @32nm HKMG need 4.5V/200us to program (Intel, VLSI Cir Sym., 2012)
  - @14nm FinFEF need 4.0V to program (GF, VLSI Tech Sym., 2014)
  - @10nm FinFET needs 5.4V to program, AE=2.4% (TSMC, ISSCC 2017)

efuse vs. I-Fuse™

- Revolutionary I-fuse™ fixes all problems in eFuse
  - Reliability & qualification guaranteed by physics
  - Robust OTP technologies NOT to cause any problems

28nm and beyond	eFuse*	I-fuse™
Program current	Up to 100mA	<3mA
HTS qual	4Kb passed 125°C 1Khr with 2 cells per bit	256Kb passed 250°C 1Khr without any redundancy
Read time in life	< 1sec	Unlimited read time
Program yield	A few % loss	~100%
Scalability	NO	YES
Testability	NO	YES. Achieve ZERO defect

* Customers testimonies

Beyond 28nm: I-Fuse™ vs. Anti-Fuse (AF)

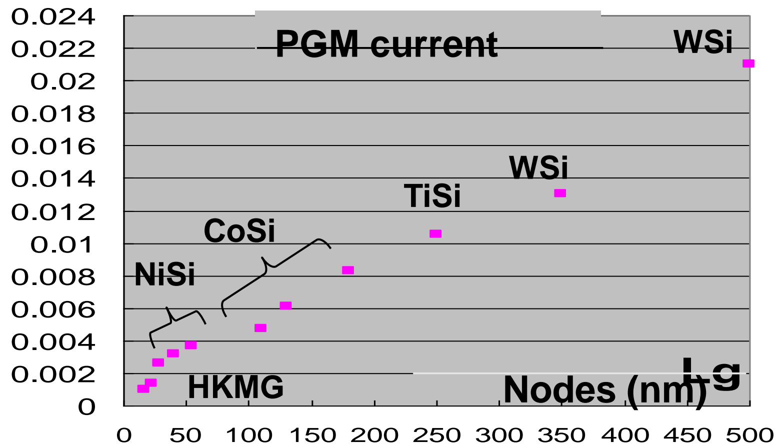
ATTOPSEMI Technology

- Fuse narrower => PGM current lower
- Low PGM current => low PGM volt.
- Fuse PGM scalable to 5/3/2/1nm
- Non-breaking I-fuse™ wins eFuse

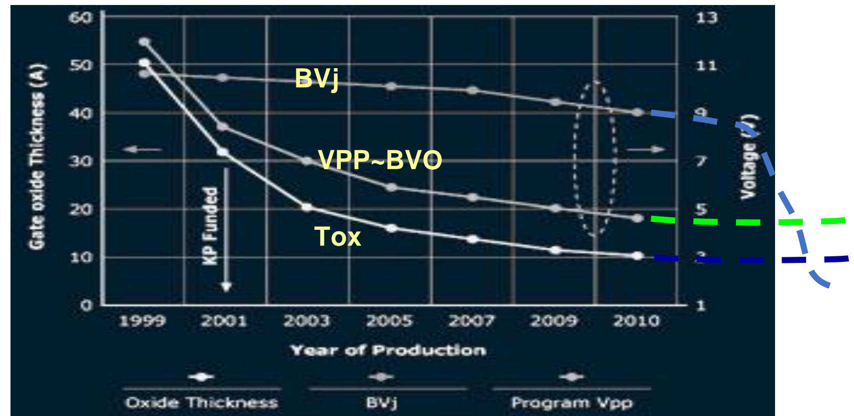
- Supply voltages lower and lower
- Oxide/PGM voltage can't scaled and reduced
- Device breakdown before oxide
- AF Hard to work beyond 14/16nm

Fuse current programming prevails AF voltage programming !!!

Non-explosive I-fuse™ prevails explosive eFuse !!!



I-fuse™: current PGM



BVJ/BVO: Breakdown voltage of junction/oxide

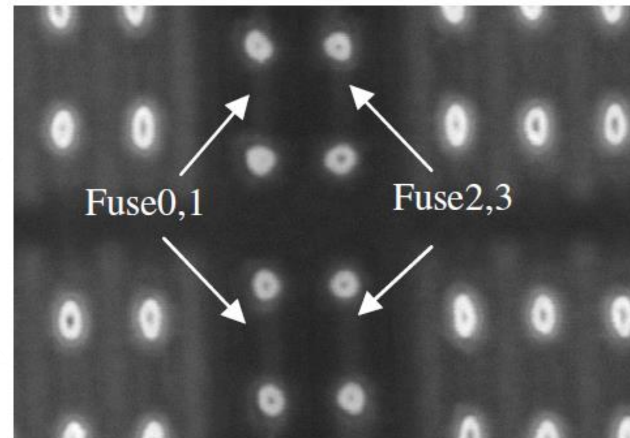
Anti-fuse: voltage PGM

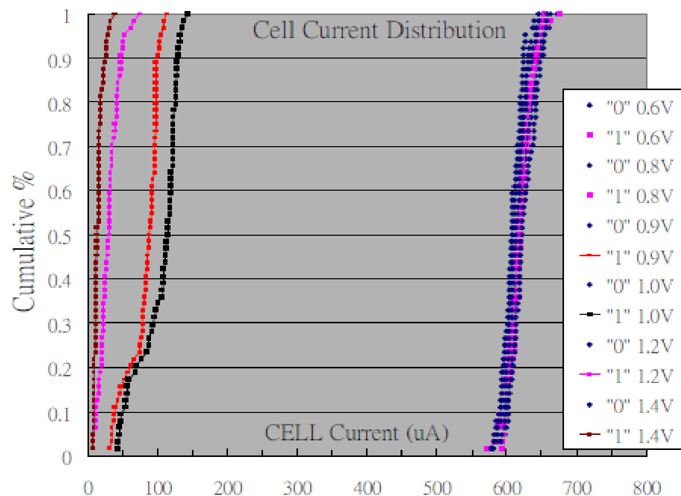
Low Voltage/High Density I-fuse™ IP

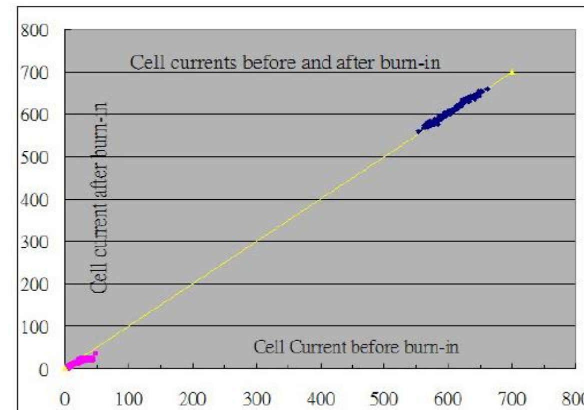
- 1R1T: Low Program Voltage (LV)
  - T40G: PGM 1.15V+/-5%, core VDD=1.1V
  - T22ULP: PGM 1.1V+/-5%, core VDD=0.8V
  - GF22 FDX: PGM 0.8V+/-5%, core VDD=0.8V
- 1R1D: High Density (HD)
  - 0.18um: PGM 3.9V+/-5%, Area: 1/4~1/5 of LV IP
  - 0.13um: PGM 3.6V+/-5%, Area: 1/4~1/5 of LV IP
  - 40nm: PGM 2.9V+/-5%, Area: 1/4~1/5 of LV IP
- Ultra-low Energy Read
  - 1/100 read energy for energy harvest (0.4V/1uA read @GF22)
- Many 1st tier customers: 15 in sensor/MEMS/PMIC out of 30 worldwide
- Sub-16nm FinFET nodes: Silicon in Q1 2020

I-Fuse™ 4K8 Macro at 22nm CMOS

- 4K8 I-fuse™ (IEEE S3S Conf 2017-2018)
  - Small 1R1T cell: 0.744um2
  - Small 4K8 macro: 0.0488mm2
  - 1.0V~1.45V program voltage
  - <1.4mA program current
  - High data security
  - High reliability: 150°C HTS, 125°C HTOL







0.4V/1uA Read @22nm CMOS

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- Battery-less RFID needs 128b OTP for authentication
  - Low voltage: 0.4V, rectified from antenna receiver (0.8V nominal VDD)
  - Low current: 1uA, source power from antenna coupling
  - High reliability: secured key stored in OTP for authentication

- I-fuse™ 64x1 OTP worked 0.4V/1uA @22nm CMOS--- The only OTP in the world.
  - Cell: low program voltage allows reading at 0.4V
  - Peripheral: ultra-low current sensing to achieve 0.4V/1uA :
    - Not MOS as amplifier: need to bias in high gain region
    - Not Inverter as amplifier: need post-program resistance >100K ohm
    - Novel sensing techniques never used in memory designs

  - Press released w/ GF and Fraunhofer IPMS on Nov. 19 2018
  - To be published in IEEE S3S Conf. Oct. 2019

I-Fuse™ in Standard Cell Library

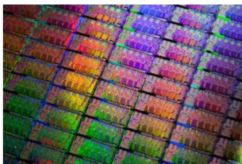
- **Build I-fuse™ bit-slice in any standard cell library**
  - Meet standard cell library formats and design/layout guidelines
  - Write Verilog model to synthesize any low bit-count I-fuse™ OTP
  - P&R I-fuse™ OTP macros with the rest of circuits

- **New Applications: security key and trimming-in-place**
  - OTP key built by random logic can be very secured than OTP memory
  - Trimming-in-place: Store tuned data locally
    - Tune and store SRAM wordline width in each block
    - Save up to 30% of 4Mb SRAM current without speed degradation
    - Silicon on UMC 28HPC+ will be back and under test
  - Tune and store FBB/RBB bias locally in each voltage island
    - Unique FD-SOI features to trade performance vs. leakage

- **Pre-requisite**
  - I-fuse™ needs no high voltage, and no charge pumps

I-Fuse™: ZERO Defect

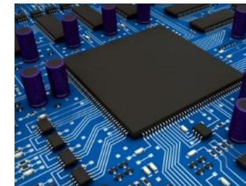
- Field return is very costly
  - 10x costs from wafer sort, packaged chip, module, PCB, to system
- ZERO defect after shipping
  - Defects should be found out and screened before shipping
- I-fuse™ can achieve ZERO defect
  - OTP dilemma: fully tested before shipping; but can't be used any more
  - Guarantee cell programmable: if initial fuse resistance <400Ω
  - Guarantee 100% programmable: if programmed within specs
  - Fully testable: every functional block, including program circuits
    - Create non-destructive program state to read 1 for complex tests
    - Concurrent read with low-voltage fake programming



$0.1

$1

$10



$100

$1000

Attopsemi Product Roadmap

ATTOPSEMI Technology

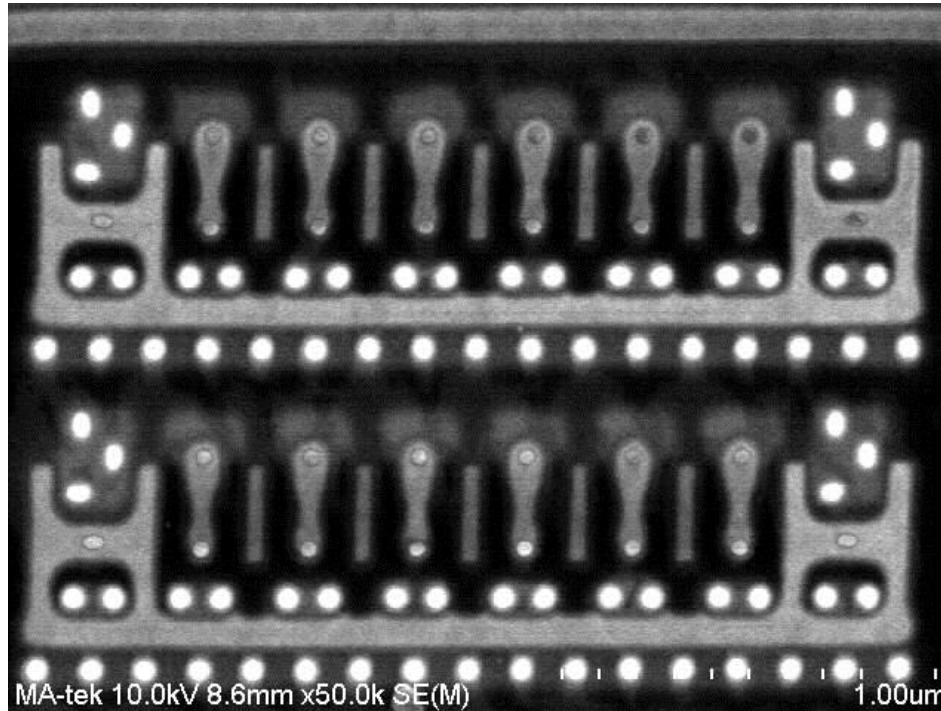
Available IP	
Technology	Foundry
0.5 um	UMC, VIS
0.35 um	UMC, VIS
0.25 um	VIS, TowerJaz
0.18 um	TSMC, UMC, VIS, Silterra, X-Fab, On-Semi, Epson
0.15 um Logic, MS	TSMC, UMC
0.15 um BCD	VIS
0.11 um Logic, MS, BCD	VIS
65/55 nm	GF, UMC
45/40 nm	TSMC, GF
28 nm	UMC
22 nm SOI	GF

2019: Q1 Q2 Q3 Q4 — 2020: Q1 Q2 Q3 Q4 — 2021: Q1 Q2 Q3 Q4

TSMC 40G/UPLP
TSMC 22/ULP
TSMC 12nm
TSMC 7nm
TSMC 5nm
XFAB 130nm
UMC 110nm
GF 22nm FD, LV Pgm
GF 12nmLP
Samsung 5nm
Samsung 11nm
Samsung 7nm

I-fuse: High Security to Hide Data

- Which I-fuse(tm) has been programmed? (GF28nm)
  - Enhanced: Lightly program to 1K, not 2K, to create less damages*
  - Enhanced: Lightly program virgin fuses, but read 0, to hide data states*



Conclusions

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- Revolutionary I-fuse™ concept: logic device, not NVM
  - High quality and reliability guaranteed by physics
  - Program behavior can be modeled in HSPICE or Verilog-A
  - Synthesized in standard cell library like flip-flops
  - Low program voltage/current: 0.9V/1.4mA
  - Low read voltage/current: 0.4V/1uA
  - High reliability (defect <0.007ppm)
  - No charge pumps.
  - Cell/IP scalable with Moore's law
  - Fully testable: for ZERO defect
  - Pass 250oC 1Khr HTS
  - High data security

- I-fuse™: the dream OTP comes true
  - I-fuse™ is a logic device. Doesn't need to be qualified like an NVM
  - Save tremendous amount of time, costs, and efforts to industry !!!

Backup

The Team

- **Founder: Shine Chung**
- **Harvard graduate in Applied Physics**
- **30 years of IC design experience**
- **Memory design in AMD, Intel, and HP**
- **PA-WW architect (PA-WW: precedent of Intel's Merced)**
- **Director at TSMC (eFuse pioneer)**
- **VLSI and ISSCC technical committee for 4 years**
- **Two-time TSMC innovation award recipient**
- **61 patents granted before Attopsemi**
- **Filed >70 U.S. patents and >60 granted after Attopsemi**

- **Co-founder & VP of Eng: WK Fang**
- **MSEE from Ann Arbor, U. of Michigan**
- **20-year experiences in memory**
- **Technical Manager at TSMC**
- **Department Mgr for eFuse**
- **Design managers for N90/N65 SRAM TV, eDRAM**
- **MTS in SRAM, FIFO, CAM at IDT**

Thank You

OTP: One-Time Programmable IP

ATTOPSEMI
Technology

I-fuse™

Lord, give me a dream OTP.