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***Innovative eFPGA IPs revolutionizing low cost low
power edge devices.***

Catherine Le Lan
Catherine.lelan@menta-efpga.com
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Menta eFPGA product

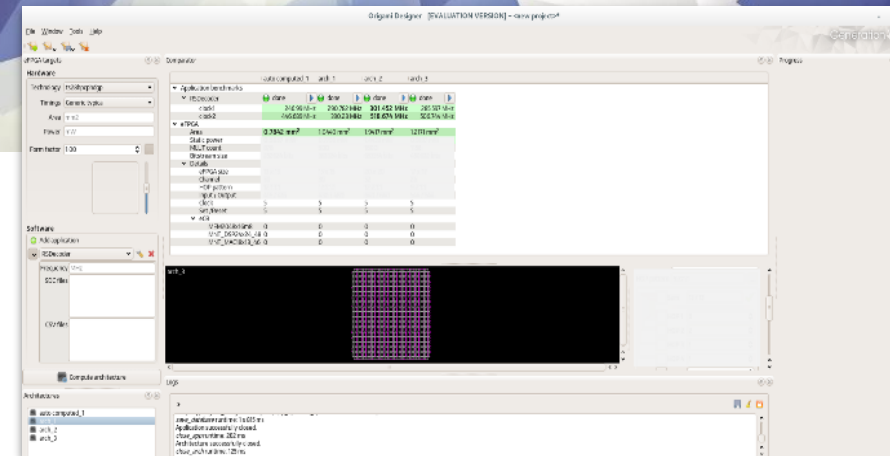
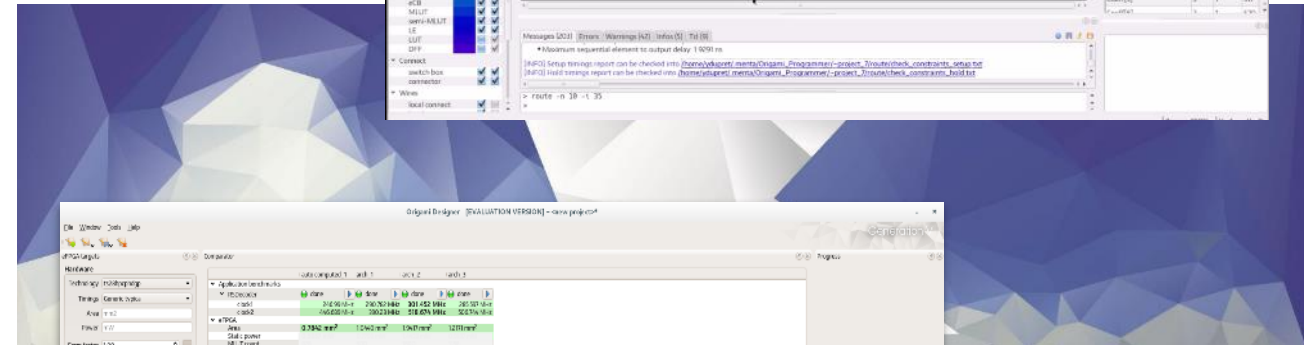
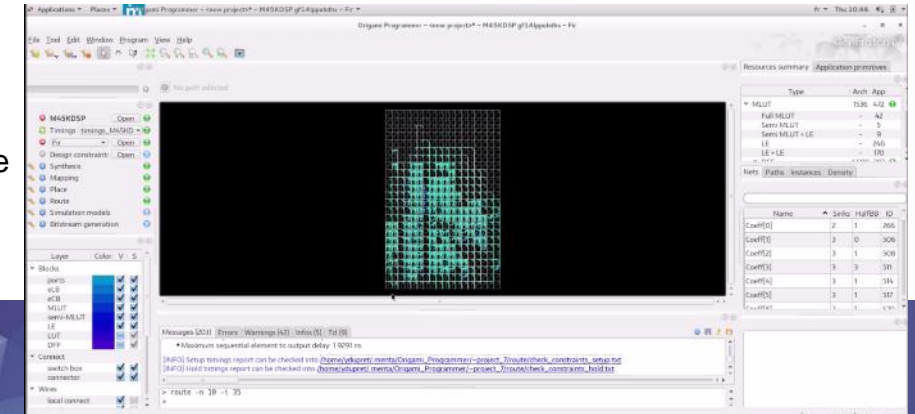
Enable SoC lifetime re-programmability

Combine ASIC/SoC and FPGA



Pure digital eFPGA IP

Programming Software
Origami Programmer



Definition Software
Origami Designer

Define the perfect eFPGA IP

Processing is moving to the Edge

- Privacy
- Latency
- Reduce data transfer

On the edge, power is even more critical
 On the edge configurability is even more critical

➤ **New algorithms, new architectures need to be used to address power and reconfigurability at the edge**

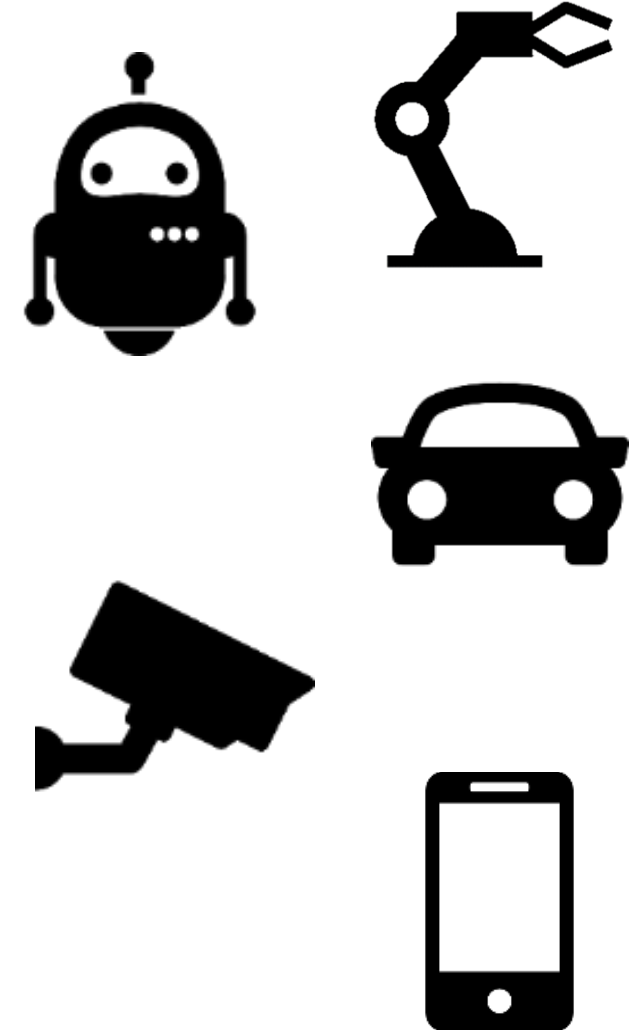
Cloud / Data center



Heterogeneous computing
 CPU / GPU / FPGA/ ASIC

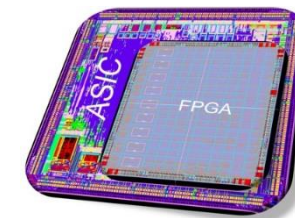
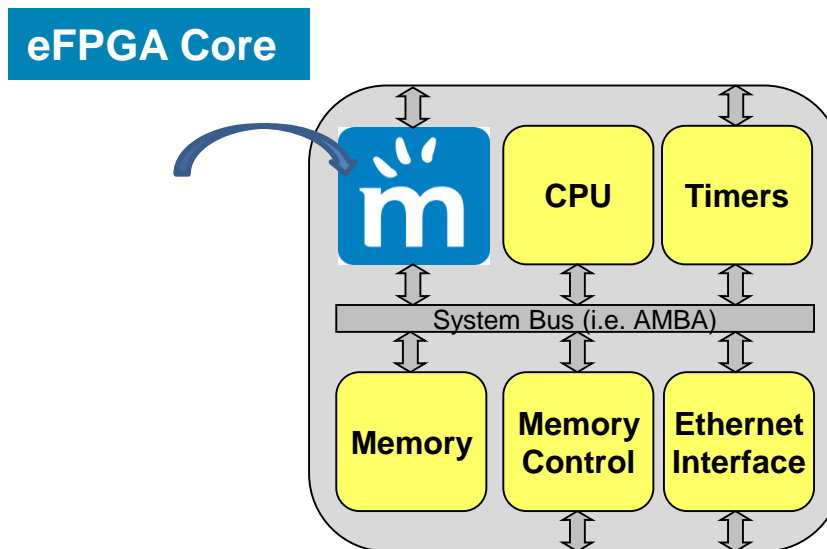


Device / Embedded



Reconfigurability Challenges

- For Time to market and cost reduction
 - System needs
 - To support different applications
 - To be reconfigurable during their life time.



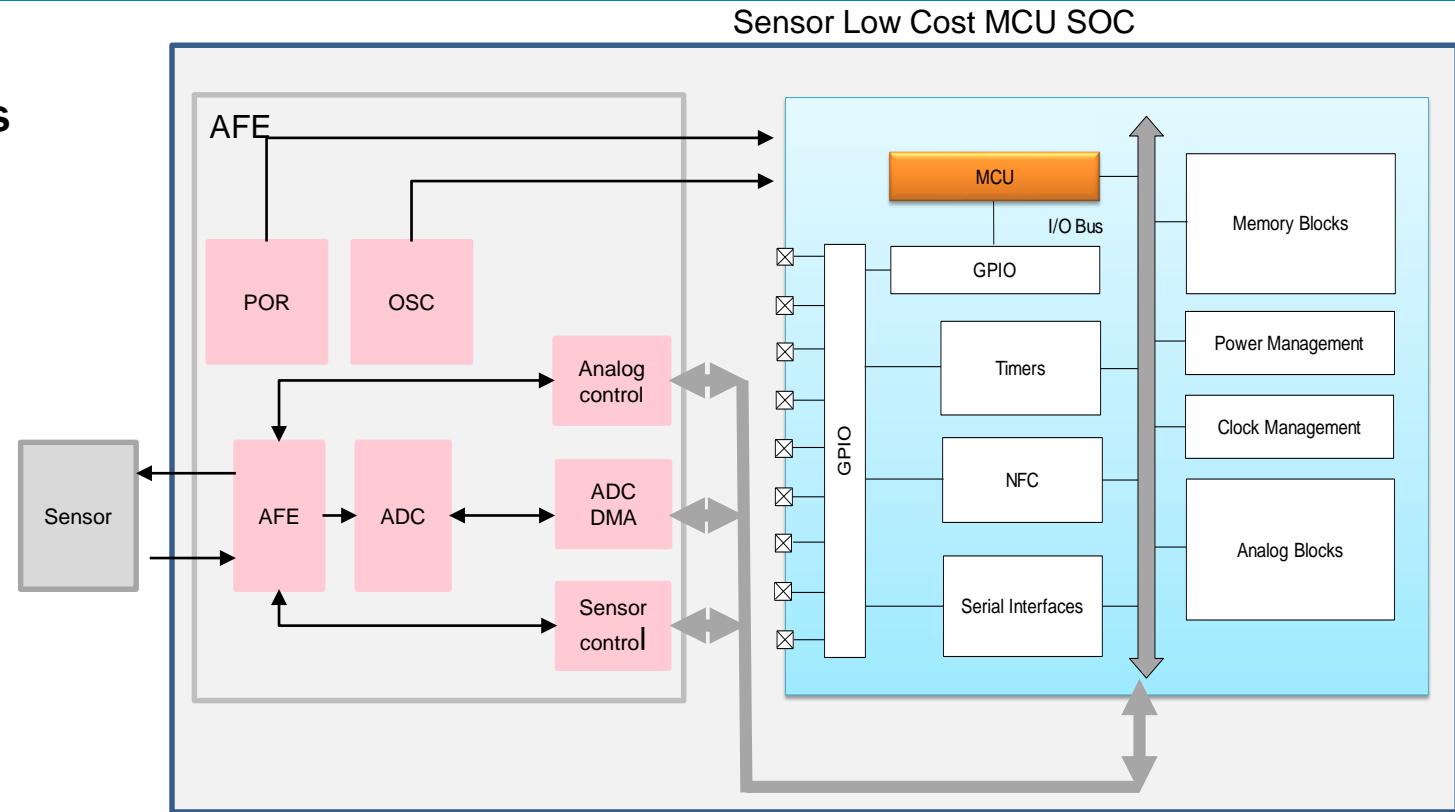
Power consumption challenges

- Data center consume 5% of WW energy
 - may move to 20, 40% in close future
- Most of this power is due to Data movement rather than data processing



Typical example: Sensor chips

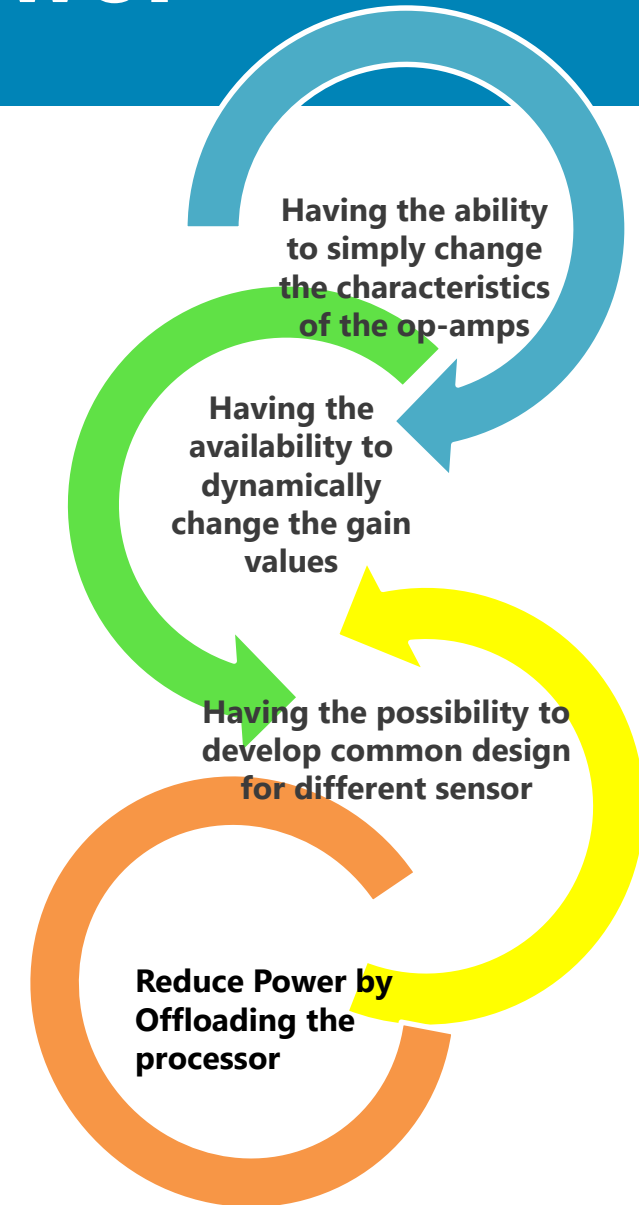
- **Sensor Chips circuitry:**
 - Digital is only glue logic, Differentiator is mainly in the analog part
- One chip per sensor
- AHB bus interface
- No re-configurability during sensor life time
- **Targeted Applications**
Automotive, Consumer Electronics, Industrial, Motor Control, Secure Transactions, Sensors control, etc



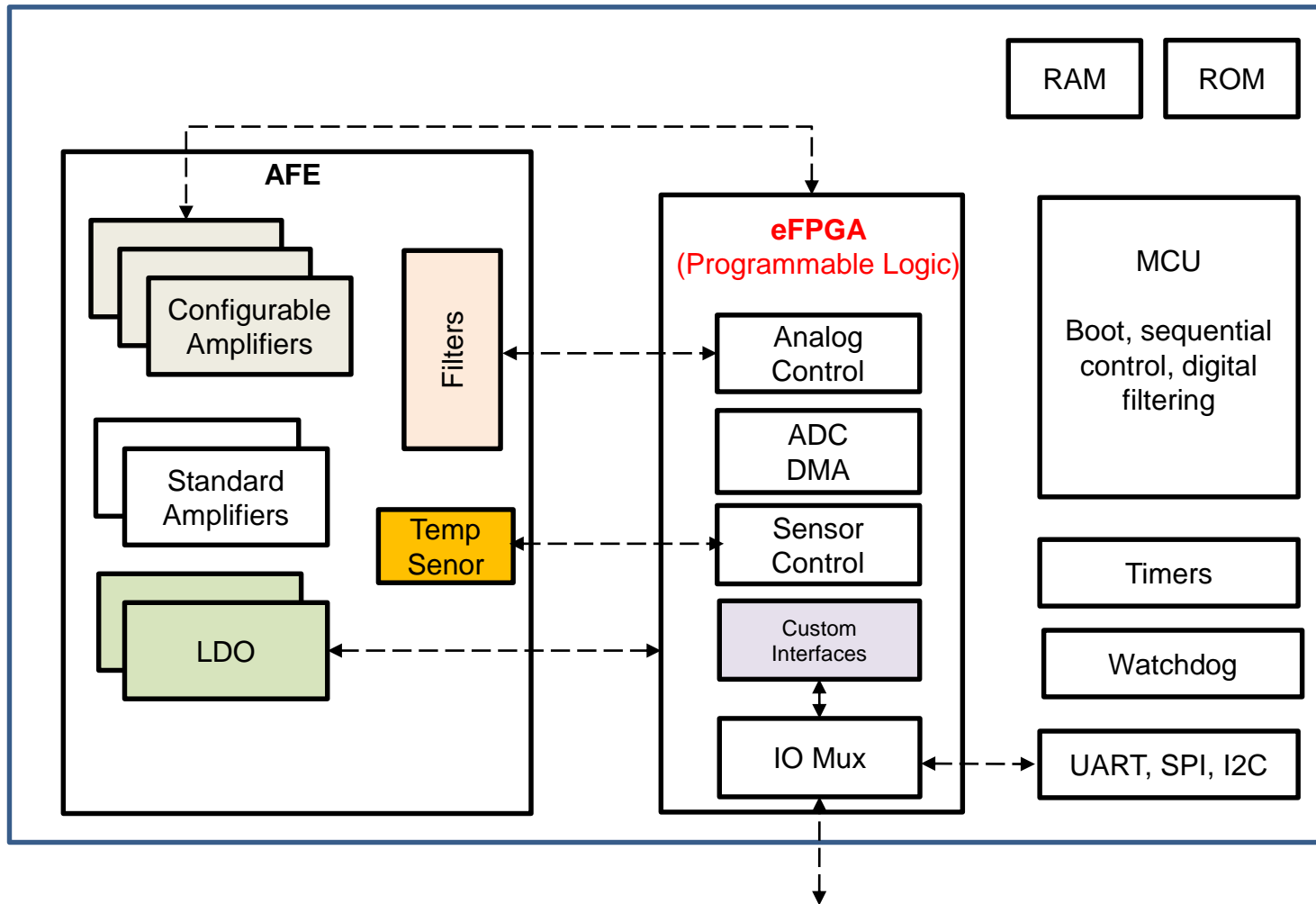
- Limited possibilities to support various sensors
- Limited possibilities to act on sensors drift or trimming over time
- Prone to design error and re-spin – especially when last minute changes are required

- Sensor SOC need to be tune during production or during life time to adjust trimming or drift. Not easy to do when they are in the filed
- Need to develop common design for different sensors
- Need to reduce power consumption by off loading the MCU and doing data parallel processing

The idea is to use eFPGA technology to build a fully configurable SOC that allows such capability.



The Architecture Solution



- Sensor calibration made unique per chip through unique bitstream
- Compensate for environment variation, like filtering adjustment depending on thermal or other environment parameters or through out the life product (captor drift) as a back treatment
- CDSP can be useful for digital filtering even if analog filters are necessary first
- Configurable IO dedicated to user interface (uart/SPI/I2C) - ok all or partly in eFPGA (only configuration and control of IO and the com IP (uart/SPI etc.)
- Off load the MCU

- **Menta eFPGA IPs** is be used to:
 - Allow the designer tune and debug AFE characteristics on the fly:
 - *New bitstream can be loaded on eFPGA during system run time*
 - Automate trimming
 - Adjust for sensor drift
 - Add scalability to support multiple sensor types with a single platform
 - Off load the MCU and allow parallel data processing
 - Allow power management

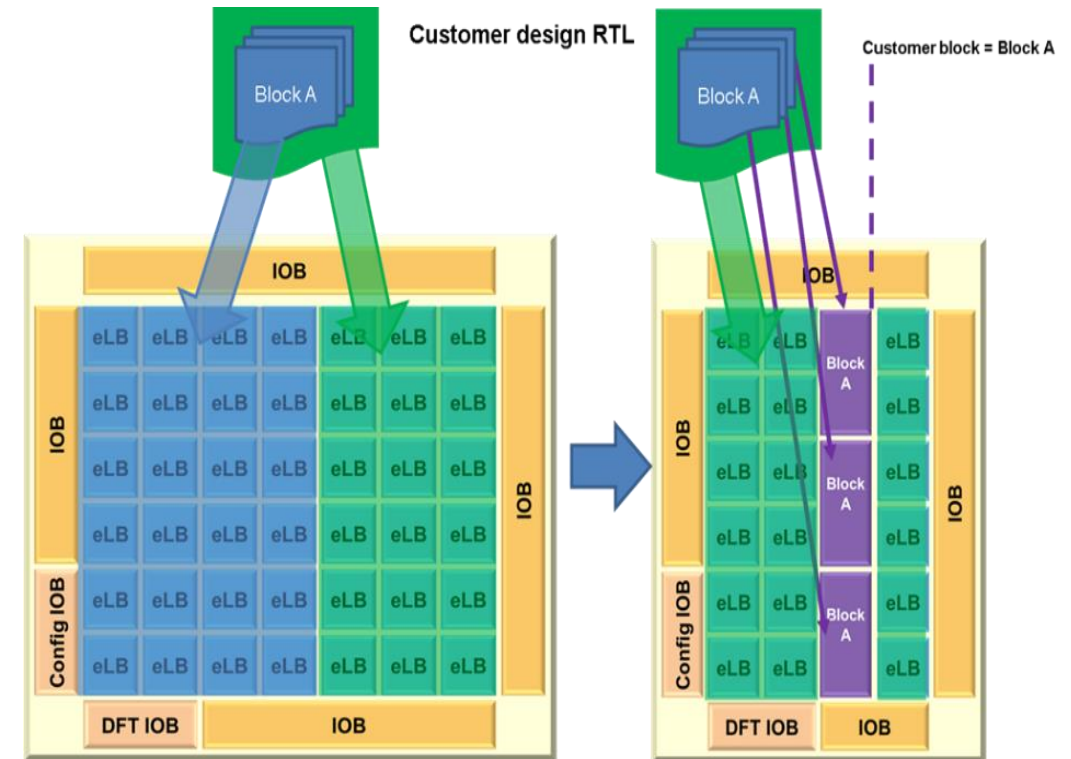


- **Menta eFPGA helps you reduce the development time and the number of chip**
- **Menta eFPGA allows you to have an architecture with you the best PPA**

Other example: Cryptographic Hardware Accelerator

- Implementation **Arithmetic IP-core** like into an eFPGA core
- eFPGA offer flexible cryptography algorithms during the product lifetime
- This is performed by establishing specific crypto custom blocks dedicated to the targeted security algorithms, using Menta's unique capability to integrate any arithmetic block.

Up to 20x performances increase expected – vs FPGA
Direct impact on the power consumption and cost of the system

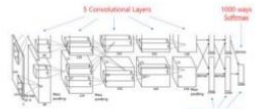


Allow several variants of a same security algorithms
Add features or customize crypto applications according to your needs

Other example: eFPGA usage AI example

CNN Architectures

AlexNet



VGG



GoogLeNet

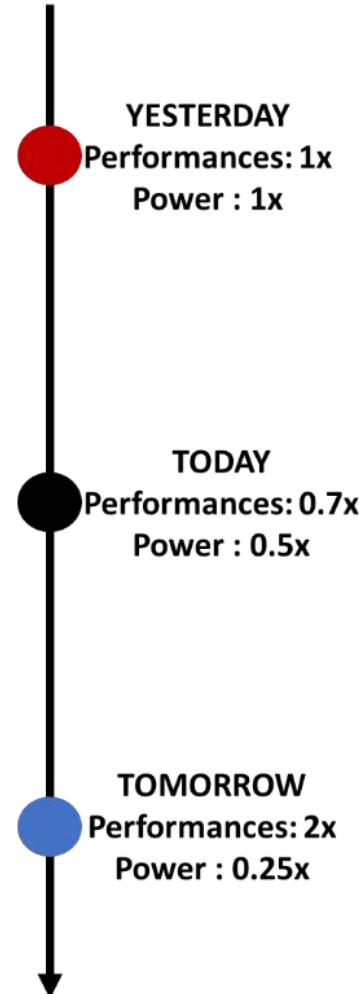
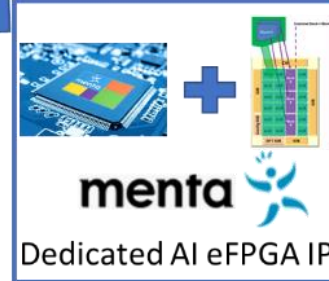


ResNet



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Sell a single “minimum functionality” configuration, thereby allowing OEMs (or end customers) to pay for the possibility of additional capabilities.



8x better Performances/Watts

AI vision algorithms inference



Decrease risk and ensure lower cost with Menta embedded FPGA

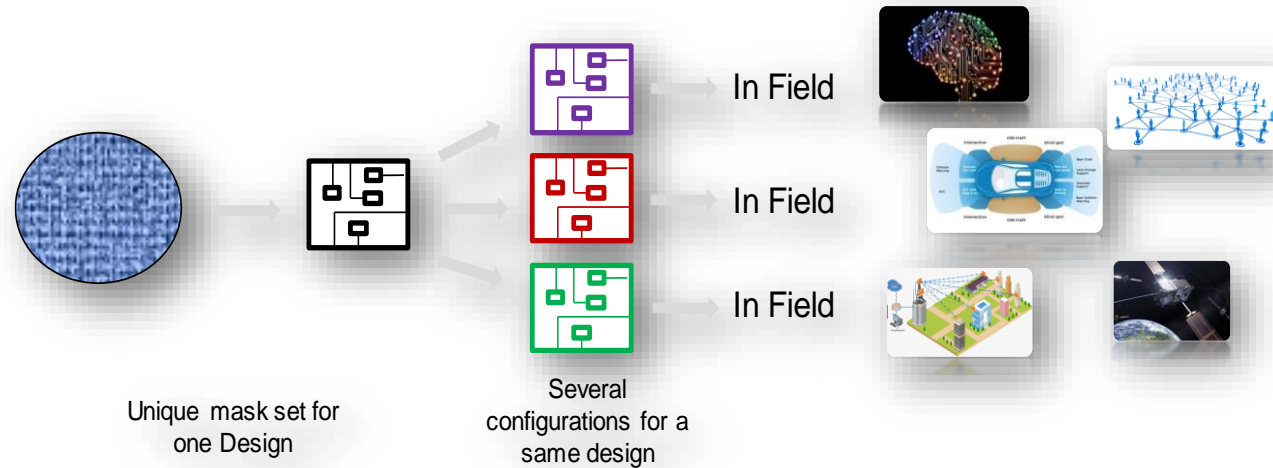
eFPGA improves Chip Flexibility & Security

Adapt your chip to different sensors

More generic and customized MCU Chips

Programmable and reconfigurable GPIO subsystem

Post Tapeout features customization (Crypto Security...)



Unique mask set for one Design

Several configurations for a same design

In Field

In Field

In Field

Adapt MCU Chips to market and customer needs after it is manufactured

Reconfigurable State Machines, complex and specific PMW functions

Reduce power consumption and increase performances by offloading the embedded processor.

Act on sensor tuning over life time

- **Menta 100% standard cells eFPGA solution**
 - Support of any technology node, foundry and process option
- **ASIC like options**
 - Power management features
 - Retention, triplication, etc.
- **Fully customizable**
 - Amount of eLB
 - Amount and provider of eMB
 - Amount and type of DSP blocs
 - Amount and type of eCB:
 - Specific arithmetic functions blocks can be developed on purpose
- **eFPGA in house software (Origami)**
 - Origami designer to create your custom architecture
 - Origami Programmer to generate your application bitstream





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谢谢