

The background of the slide is a night sky featuring the Milky Way galaxy. The galaxy's core is visible as a bright, orange and white band of light stretching across the upper half of the frame. The sky is filled with numerous stars of varying colors, including blue, white, and yellow. In the lower right corner, a person is silhouetted against the sky, standing on the edge of a dark, rocky cliff. The overall scene is dark and atmospheric, with the light from the galaxy providing the primary illumination.

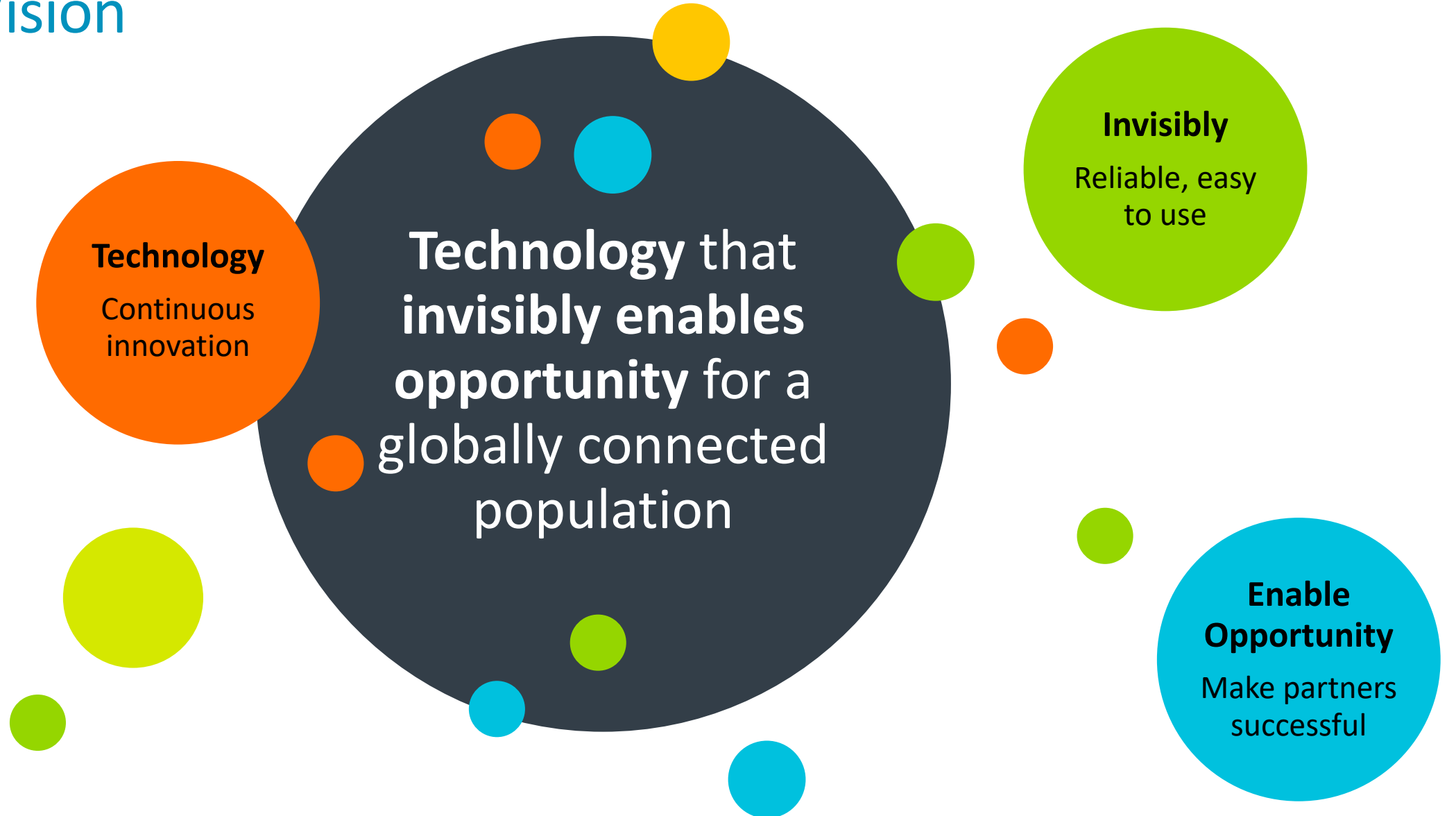
arm

Acceleration and Differentiation

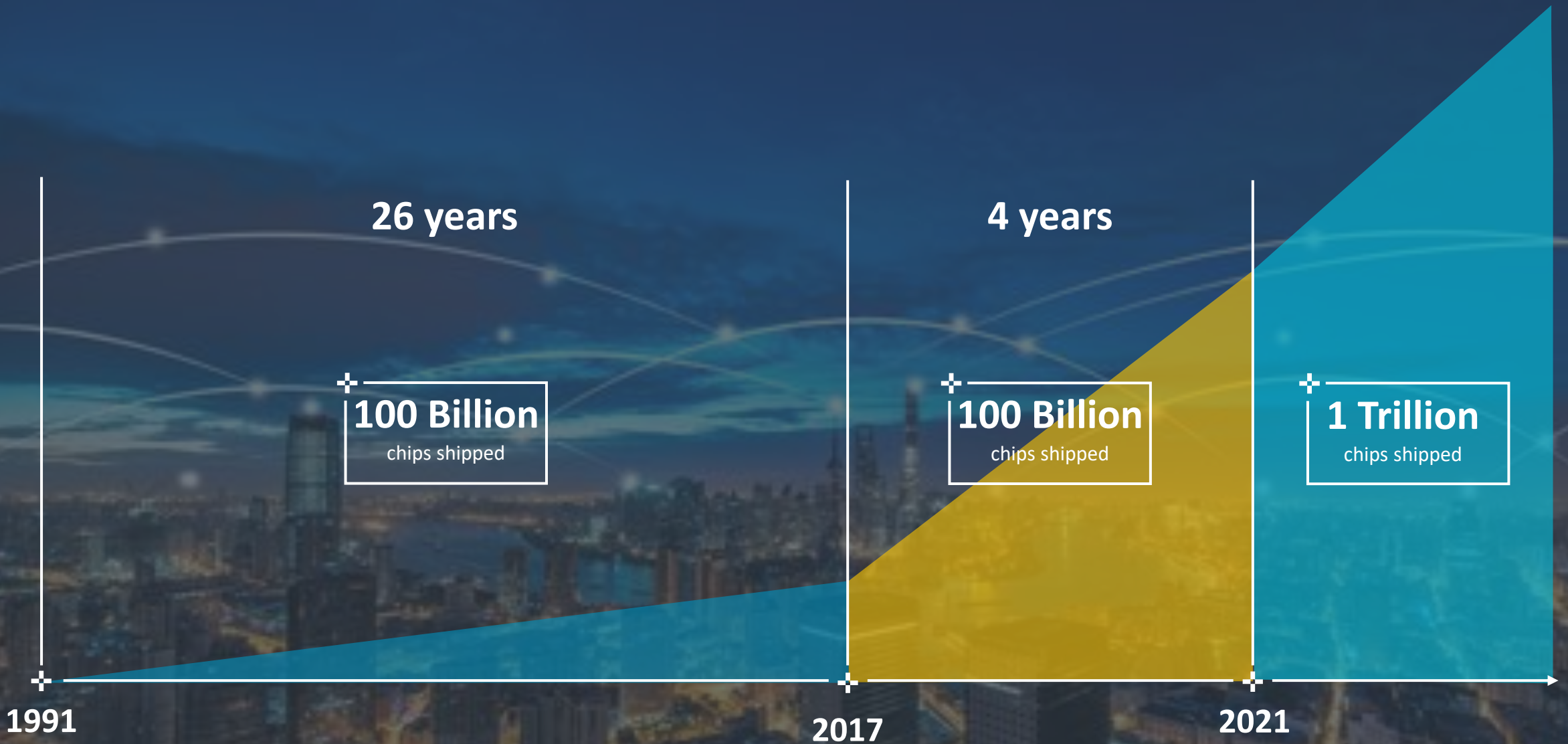
for a World of a Trillion Devices

Mike Eftimakis – Director Business Innovation Strategy
3rd December 2019

Arm's Vision



Digital Transformation Drives Volume



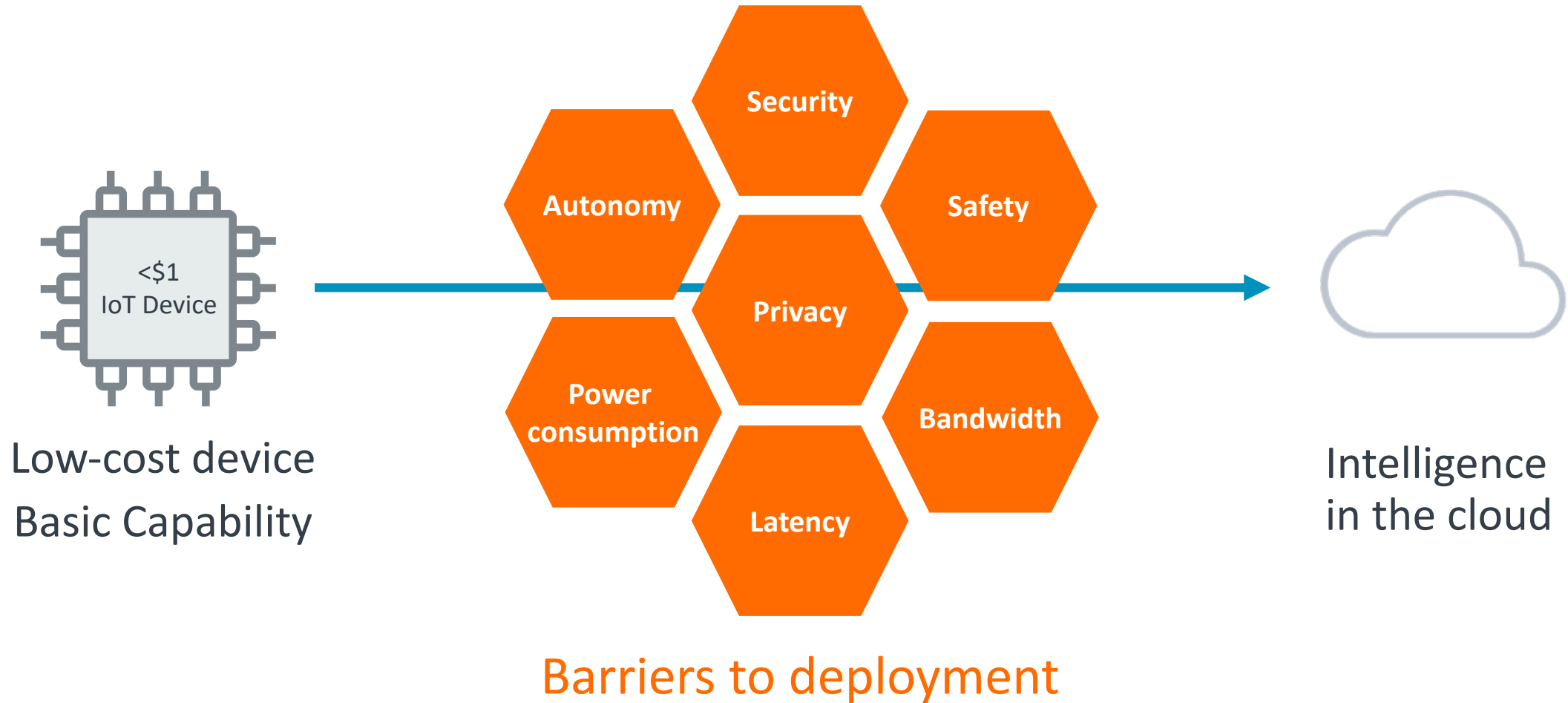
1991

2017

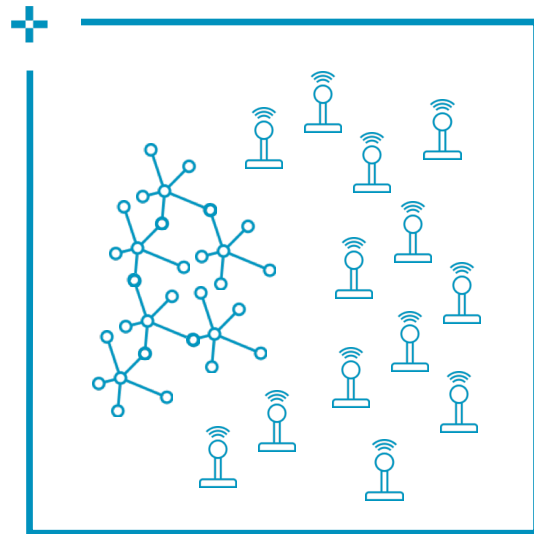
2021

Barriers to IoT Mass Deployment

“All intelligence in the cloud” will struggle to scale



Compute Requirements in a Trillion-device World



Trillions
of Devices

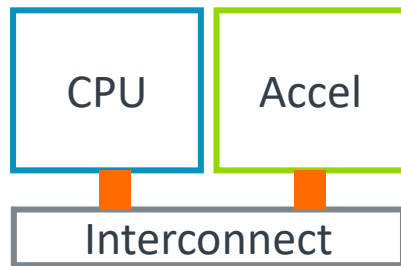


Millions
of Workloads

Optimal use cases
for workload-specific
acceleration

Different Types of Acceleration

Memory Mapped



- Decoupled
- Parallel

Co-processor



Custom Instructions

New
for Arm



- Integrated
- Interleaved



Acceleration Through Custom Instructions

```
mov.w    r1, #0x55555555
and.w    r1, r1, r0, lsr #1
subs     r0, r0, r1
mov.w    r1, #0x33333333
and.w    r1, r1, r0, lsr #2
bic      r0, r0, #0xcccccccc
add      r0, r1
mov.w    r1, #0x01010101
add.w    r0, r0, r0, lsr #4
bic      r0, r0, #0xf0f0f0f0
muls     r0, r1, r0
lsrs     r0, r0, #24
```

Multiple general-purpose instructions



```
MyOp01  p0, R1, #0
        // pop count n R1, return r1
```

One instruction with custom logic



- Gain performance and efficiency
 - Fewer cycles, less power




- Cost of more design investment
 - Additional logic and integration



- Risk to hardware complexity and software ecosystem
 - Impact on existing design – re-verification
 - Compilers and downstream tools need to support


The Benefits of Arm Custom Instructions



Lowest risk
Lowest cost path
to integrated custom
workload acceleration



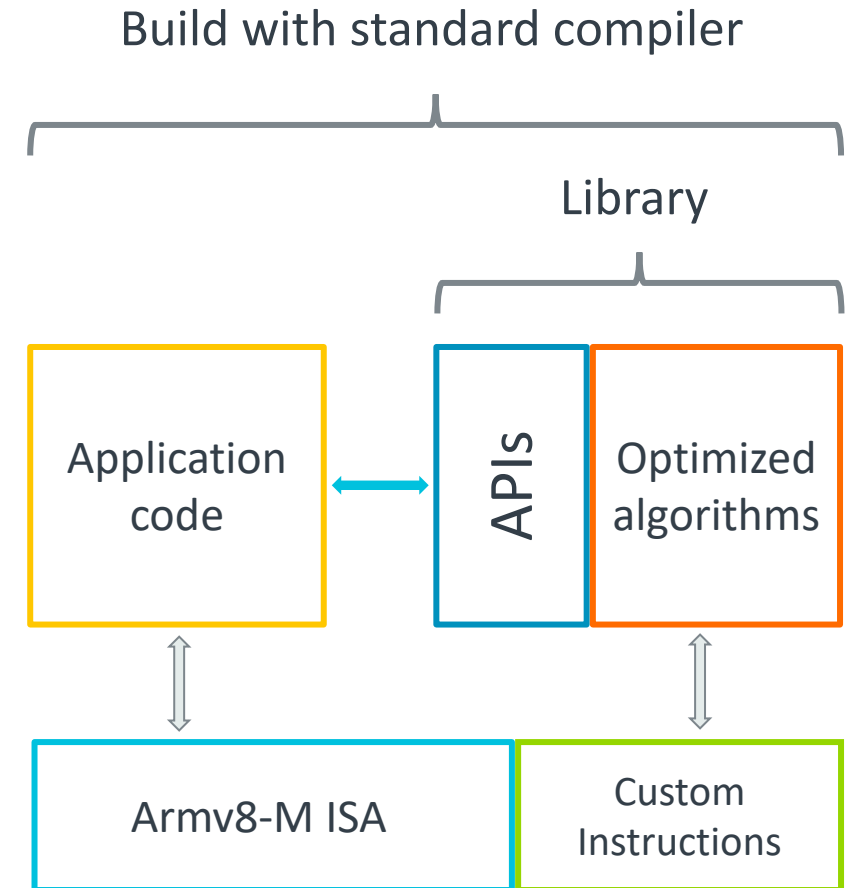
Maximizes efficiency
of hardware design
investment



No disruption to CPU
features
Standard toolchains
and SW ecosystem

Customization without Software Fragmentation

- Custom instructions use a pre-defined instruction space in Armv8-M
- Out-of-the-box support of Arm and 3rd party compilers and debuggers
- Custom instructions enabled through libraries shipped with standard board support package



Arm Custom Instructions

Workload-specific acceleration

- + Available for Cortex-M33 CPU in 2020
No additional cost
- + Standard for future Armv8-M processors
- + Customization without software fragmentation

Supported by Arm partners



arm

Thank You

Danke

Merci

谢谢

ありがとう

Gracias

Kiitos

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