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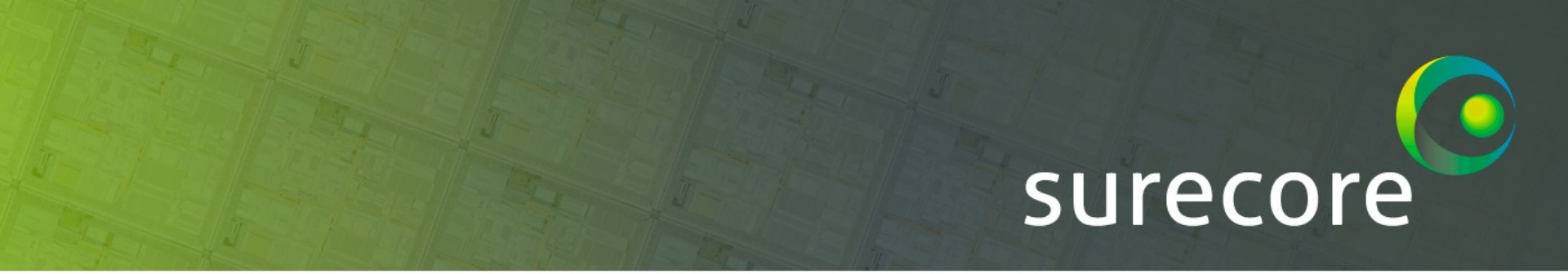
Optimizing The Silicon Porting Of Physical IP

Tony Stansfield – CTO



Premature Optimisation Is The Root Of All Evil

(attributed to Tony Hoare)

Corporate Overview

- Ultra Low Power/Voltage SRAM IP product supplier
- Custom, application-centric low power SRAM design services provider
- Innovative, patented, silicon validated architecture
- Proven in 40/28/22/16nm process nodes, scales to 7nm
- Solutions for AI, IoT, Imaging, Wearables applications
- Headquartered in UK - Design Centre in Sheffield
- Backed by investors Capital-E, Finance Yorkshire, Mercia Technologies, IMEC
- Member of RISC-V Foundation

New & Evolving Markets Demand Power Efficient IP

Technology Market Fit

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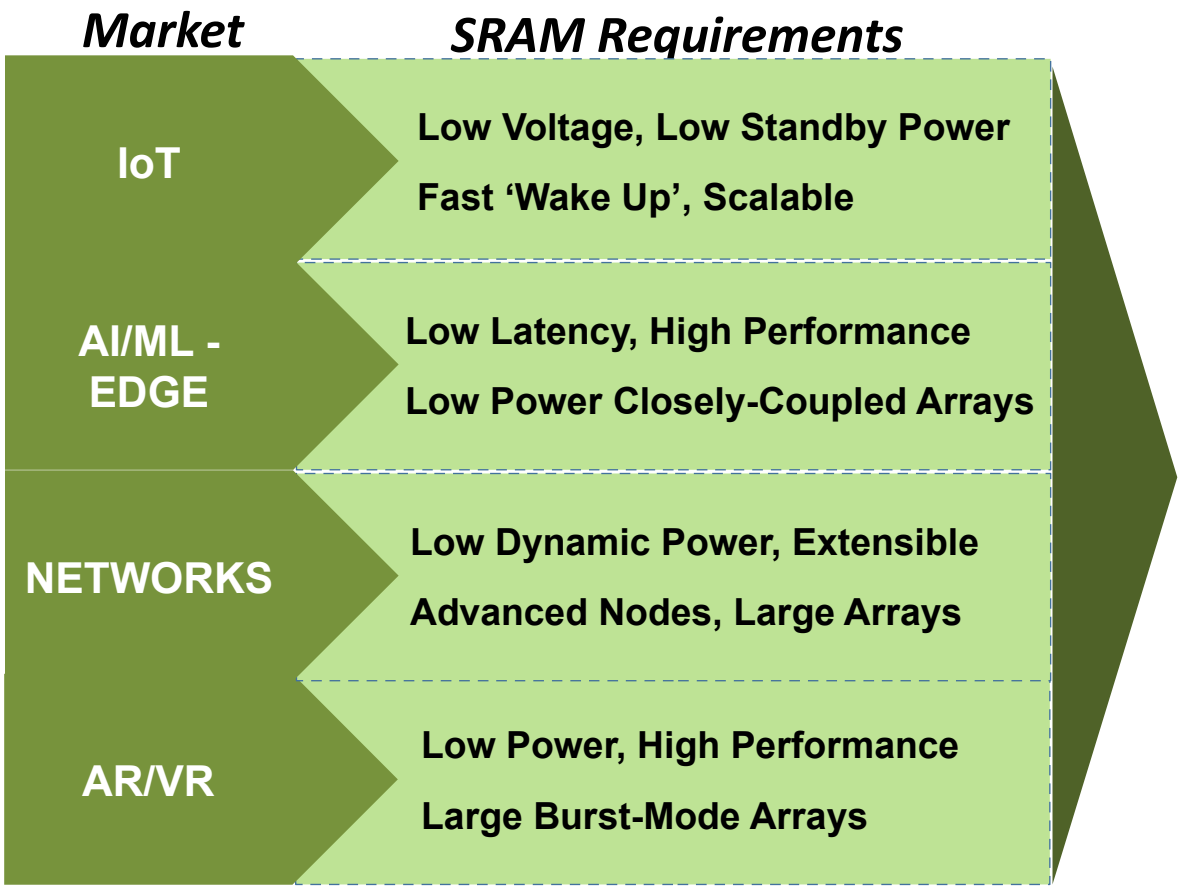

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Process Porting And Optimisation

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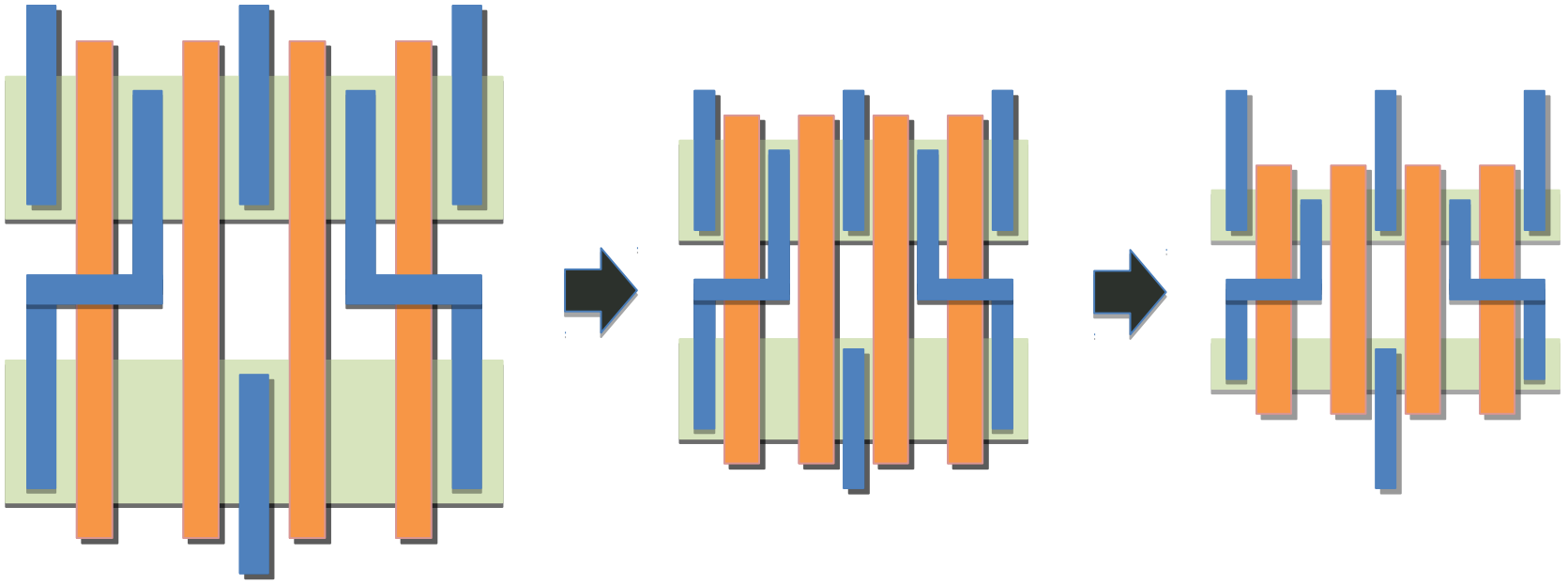

- Different scaling for different components
- High or low VT transistors
- Change in relative RC effects
- Changes in matching
  - Especially important with small transistors (e.g. SRAM)

sureFIT Streamlined SRAM Design Methodology

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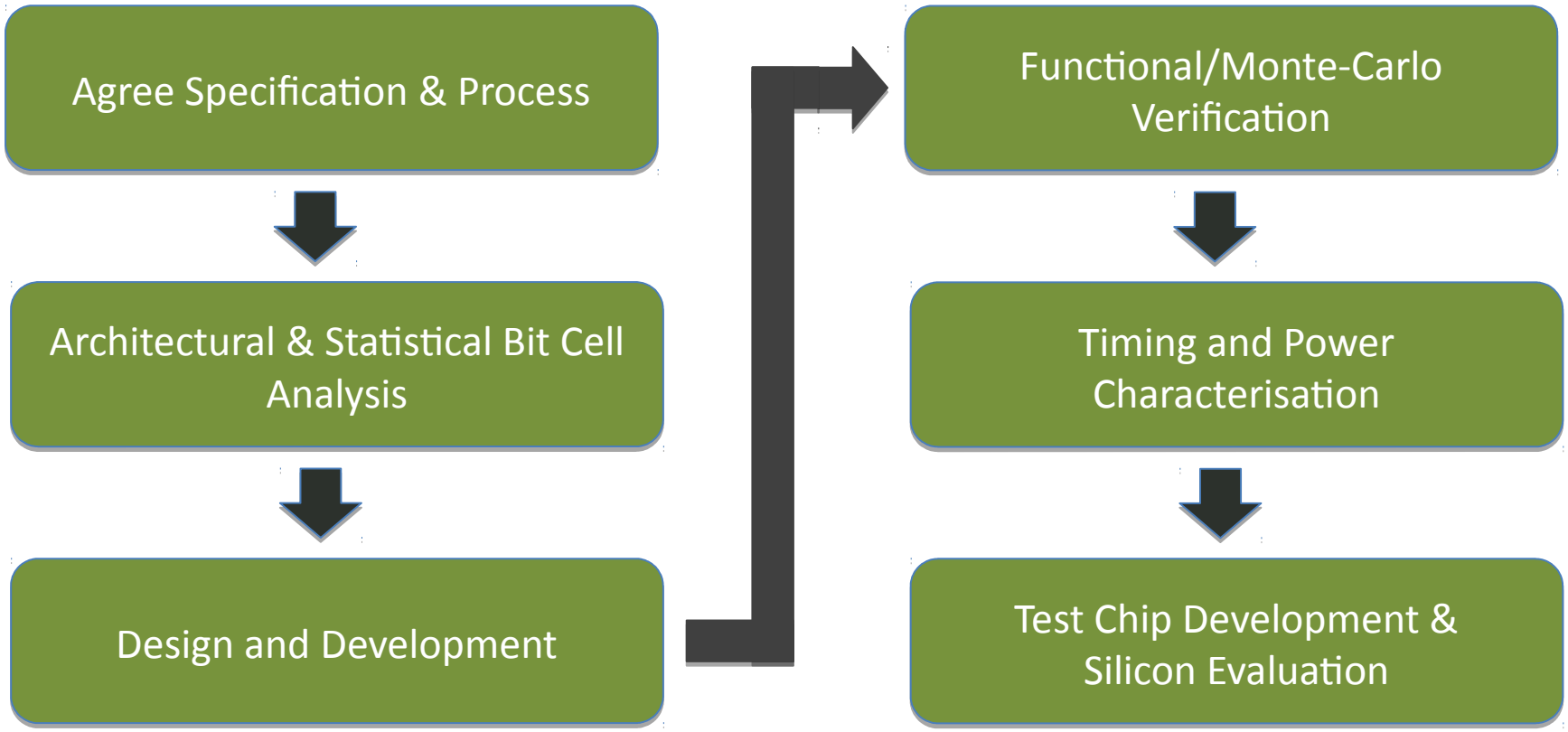

Delivers Robust & Reliable Memory Designs

Multi-Port Low Power SRAM
sureFIT – Design Example

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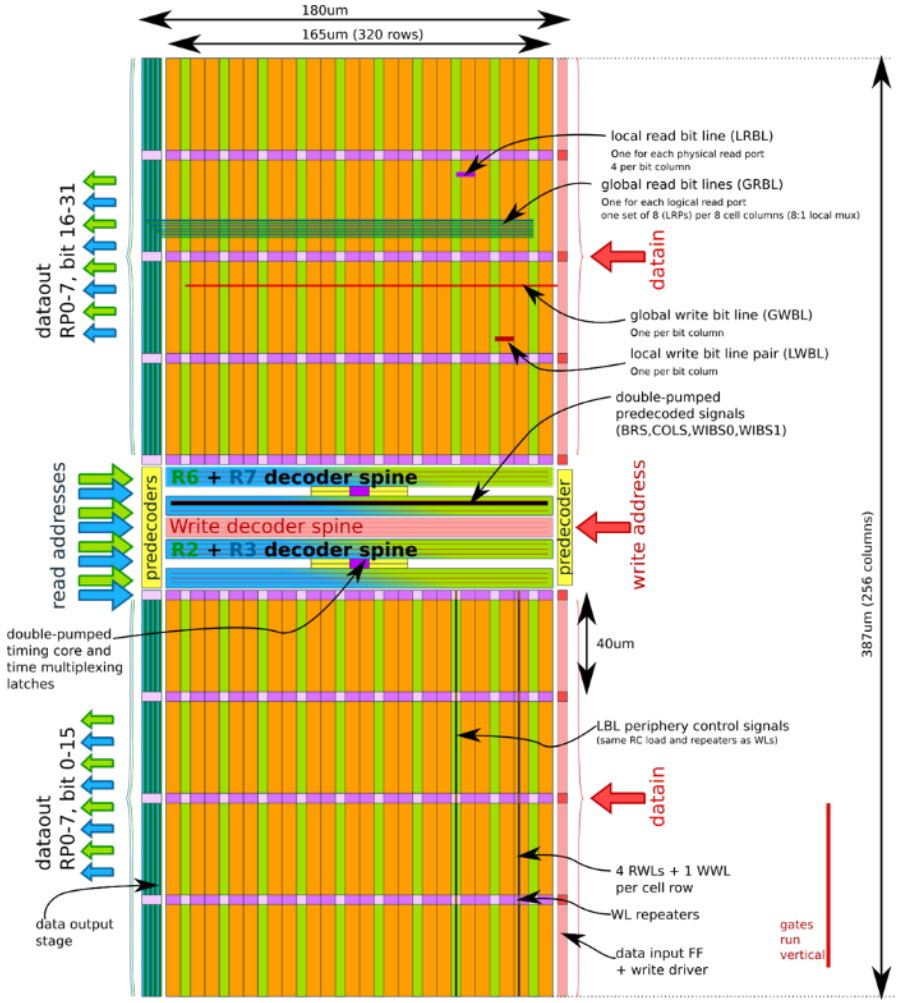

- Full custom implementation
  - Tier-1 Comms Application
  - 16 FinFET Process
- Multi-port design
  - 1 Write Port, 8 Read Port
  - Double pumped

Key achievements

- **>40% write power saving**
- **>60% read power saving**
- **Timing marginality >6sigma**
- **Achieved fmax >1GHz**
- **Met area budget**

Does It Meet The Specification? (e.g. Leakage Optimisation)

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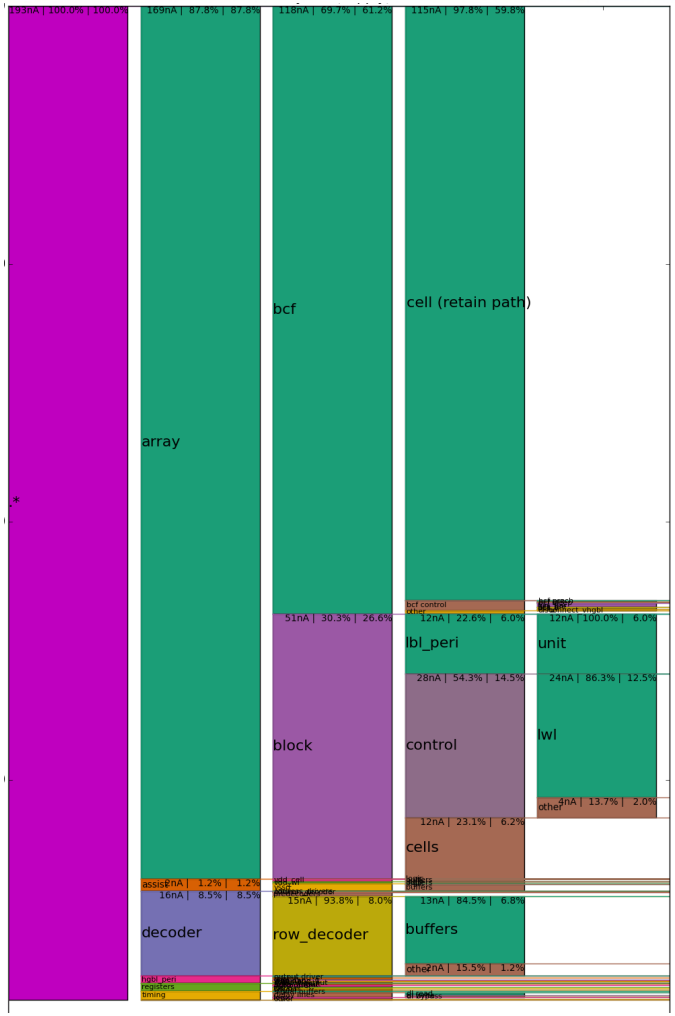

- Energy profiling
  - Hierarchical decomposition of where leakage current is going
  - SRAM bit cell leakage is unavoidable
  - Easy to see where current is going …
  - Then decide if anything can be done

Is It Reliable?
Monte Carlo Simulation

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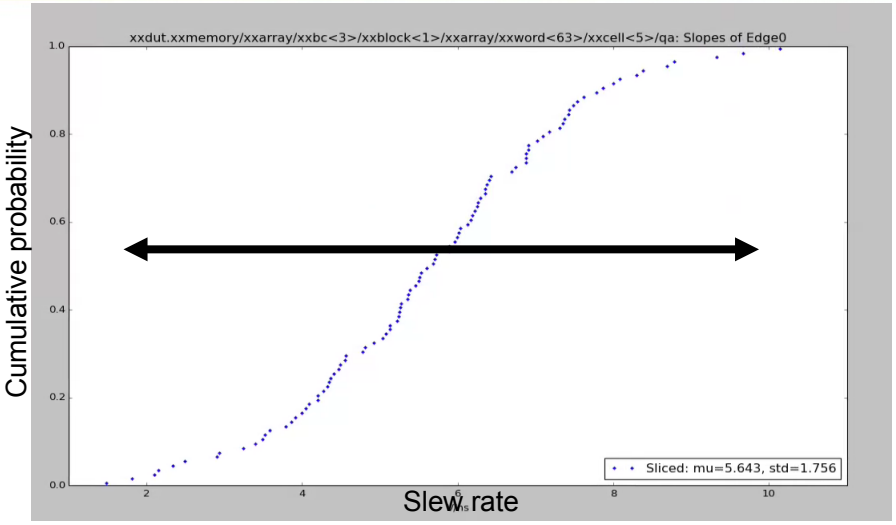
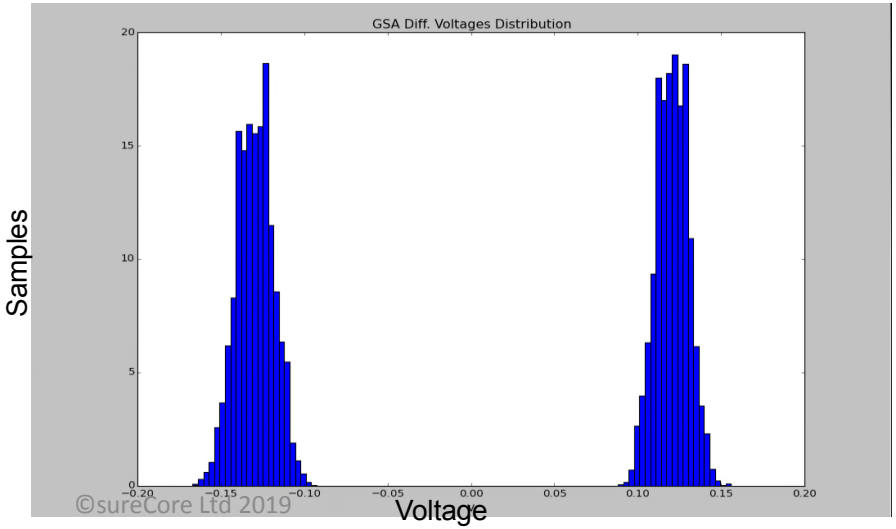
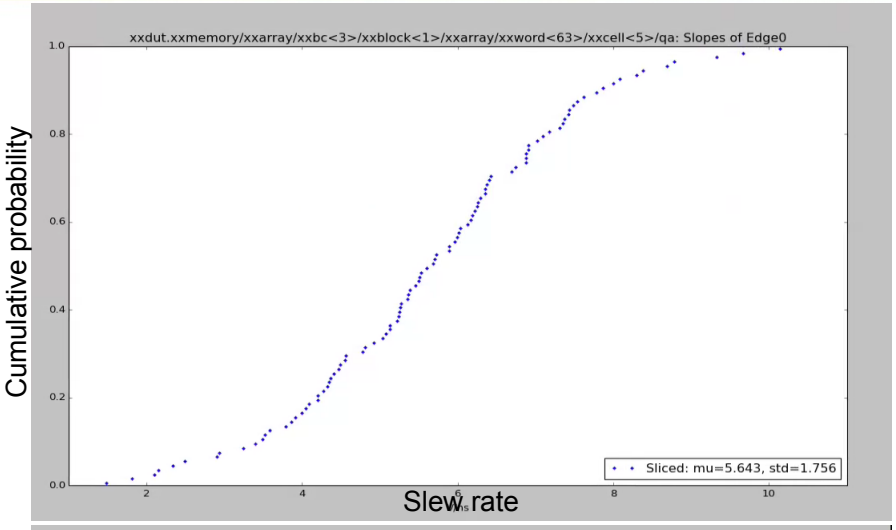
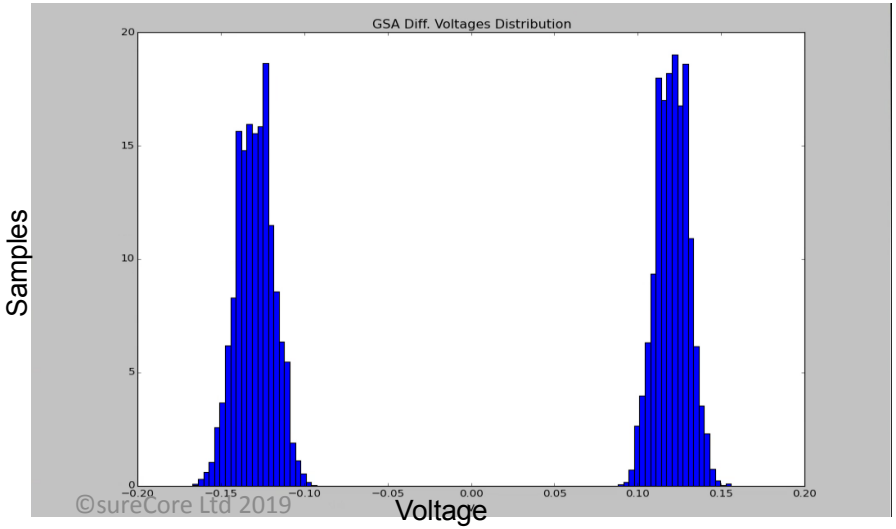




- Probe for issues in a design
- Edge rate on a node
  - Slowest is 1/6 the typical case
  - Is this a sign of a weakness?
- Voltages on a differential signal
  - Clear separation – good

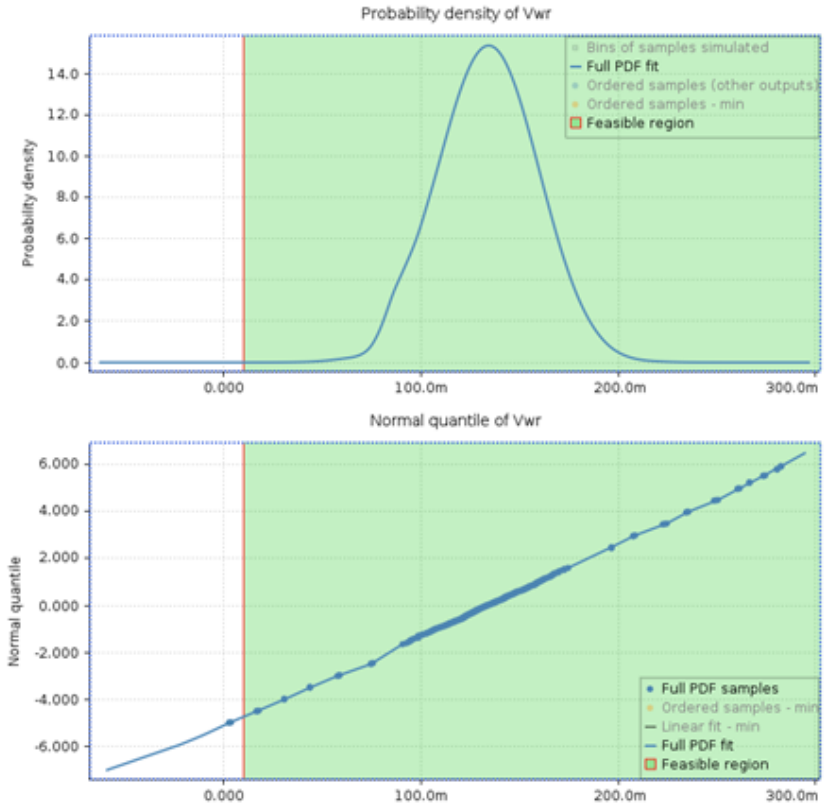
Is It Reliable?
Monte Carlo Simulation





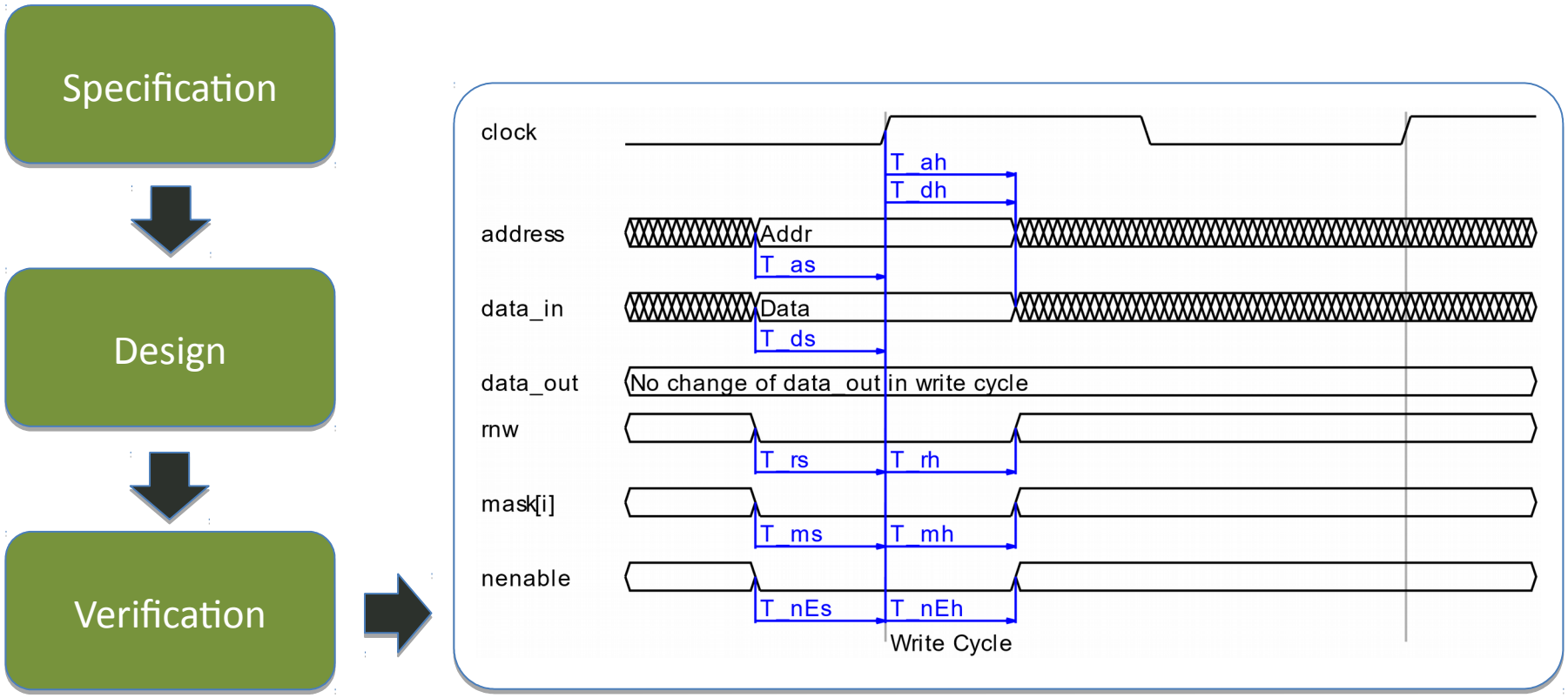
- Don't need to know in advance which nodes to check
- Check every node in a design for:
  - Edge rates
  - Transition times
  - Voltage levels
- Screen for a large spread in the Monte Carlo simulation

High-Sigma Monte Carlo Simulation



- Circuit validation with the equivalent of millions or billions of Monte Carlo samples
  - i.e. can probe the extremes of possible process variation
- Useful when there are millions of instances of a component in a device
  - E.g. bit cells

Characterisation



Well understood, well characterised design

- Monte Carlo results feed into margins
- Understand worst-case process, voltage, temperature points

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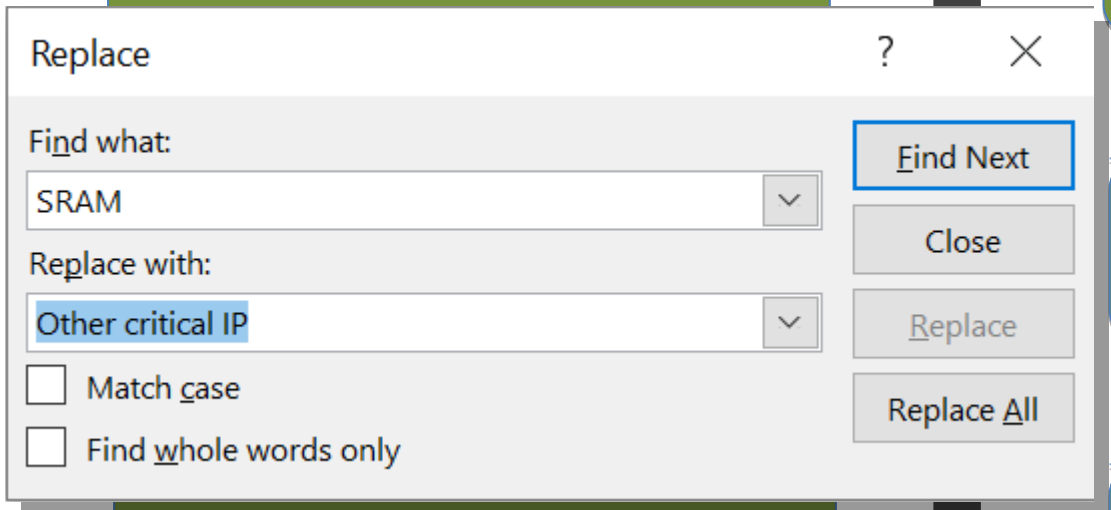
Agree Specification & Process



Design and Development

Functional/Monte-Carlo Verification

Timing and Power Characterisation

Test Chip Development & Silicon Evaluation

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Application To Non-Memory IP

- The same SRAM optimisation and process migration approaches are portable to other mixed-signal designs
  - Component understanding and optimisation
  - Verification
  - Characterisation

- SureCore design and characterisation flows applicable to other IP:
  - Simulation, verification and characterisation environments are portable
  - Design and layout skills potentially allow us to fix any issues found

Examples

Can a logic design be pushed to a lower voltage?

- Which library cells are best to use?
  - Identify which cells show least variation at reduced voltage
  - Restrict synthesis to use these cells in normal flow

- What happens to a critical path?
  - When process variation is included

Moving an IP catalogue to a new process

- Quickly remap transistors in the netlist
  - Re-simulate to check functionality
  - Vary VT types to explore performance envelope

Summary

- “Optimizing The Silicon Process Porting Of Physical IP”
- Don’t optimize for a particular piece of IP or a particular process
- General techniques that are widely applicable mean that we can quickly investigate the behaviour of a wide range of IP on a wide range of processes

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Thank You

Any Questions?