

Integrating ADAS Controllers with Automotive Grade IP

Design & Reuse IP SoC

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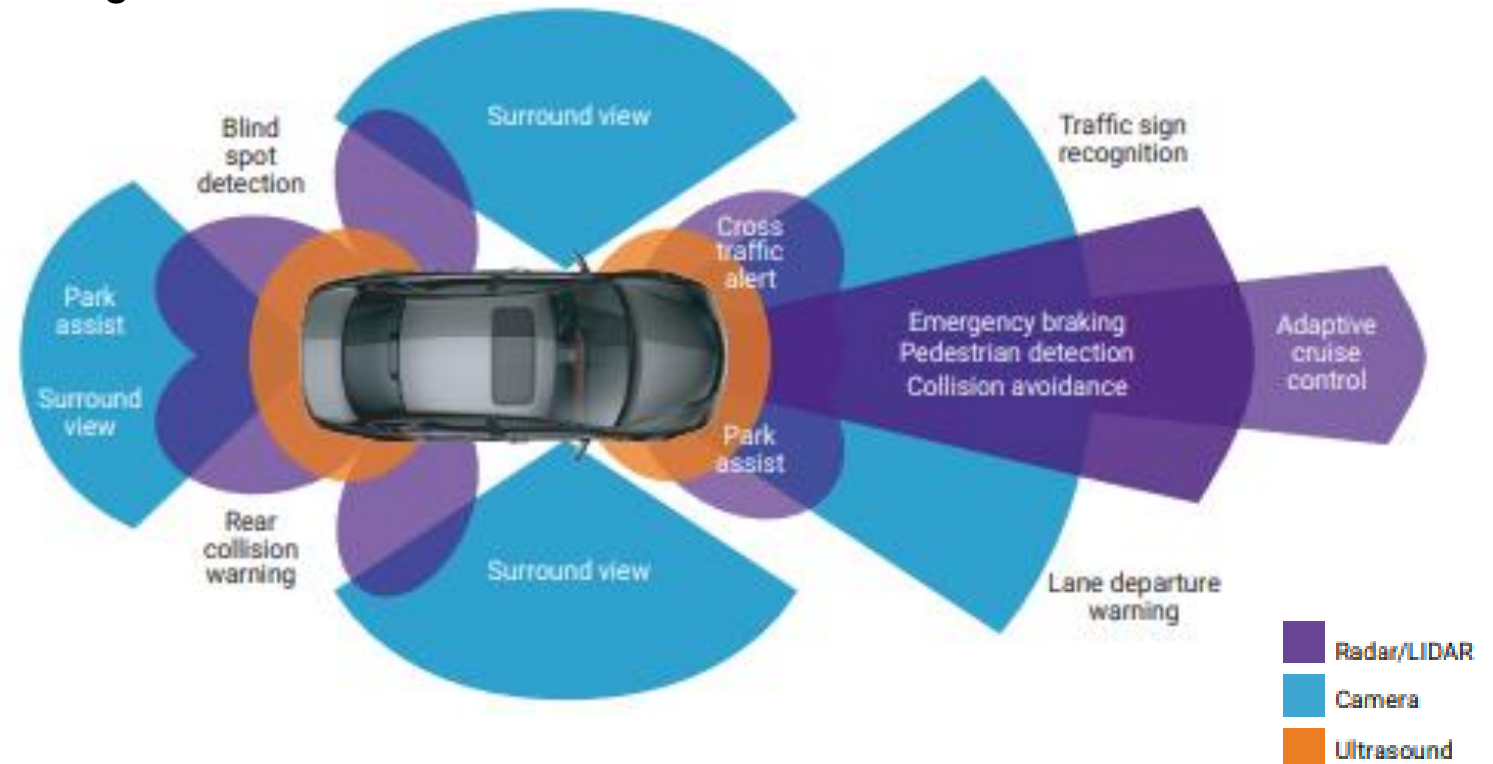
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ADAS & Autonomous Driving SoCs

Goal: Reduce Accidents, Injuries & Fatalities

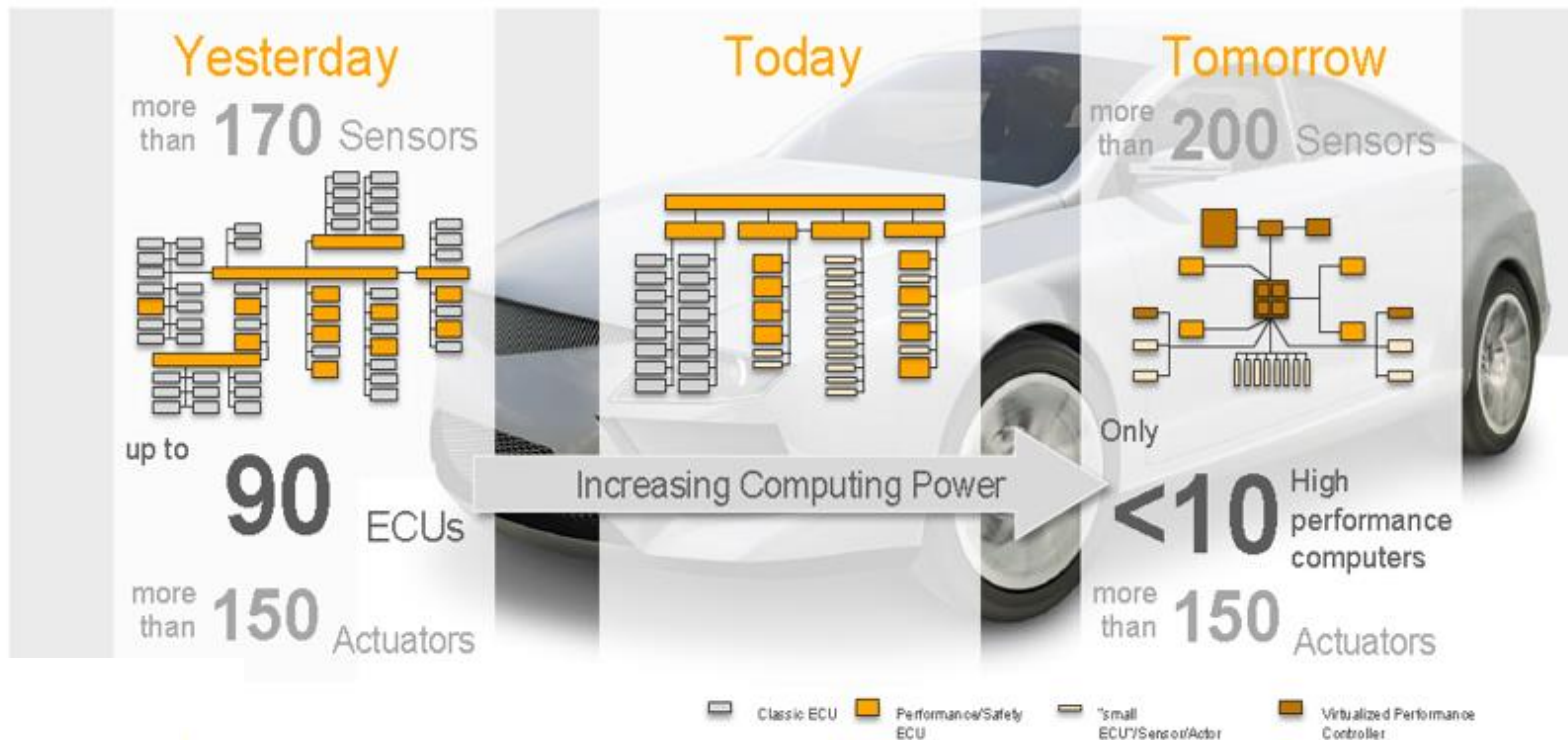
- 6.2 million automotive accidents and 35,000 deaths* in 2015 (in United States)
- About 94% of accidents caused by human error*
 - 2% environment, 2% mechanical, 2% margin error
- ADAS applications (vision-based)
 - Rear view camera
 - Park assist
 - Front camera
 - Pedestrian detection
 - AEB (Automatic Emergency Braking)
 - Surround view cameras
 - Interior camera
 - Drowsiness / gaze detection



*Source: Traffic Safety Facts Research Notes, NTSA, Aug 2016 & Feb 2015

Automotive Systems Transition to Centralized Compute Architecture

Architecture Trends shown by Continental



- Increasing requirements for compute performance lead to centralized architectures
- Separate hardware from Software
 - SW integration required
- Requires Multi-layered security and safety
 - Due to single point of failure & vulnerabilities

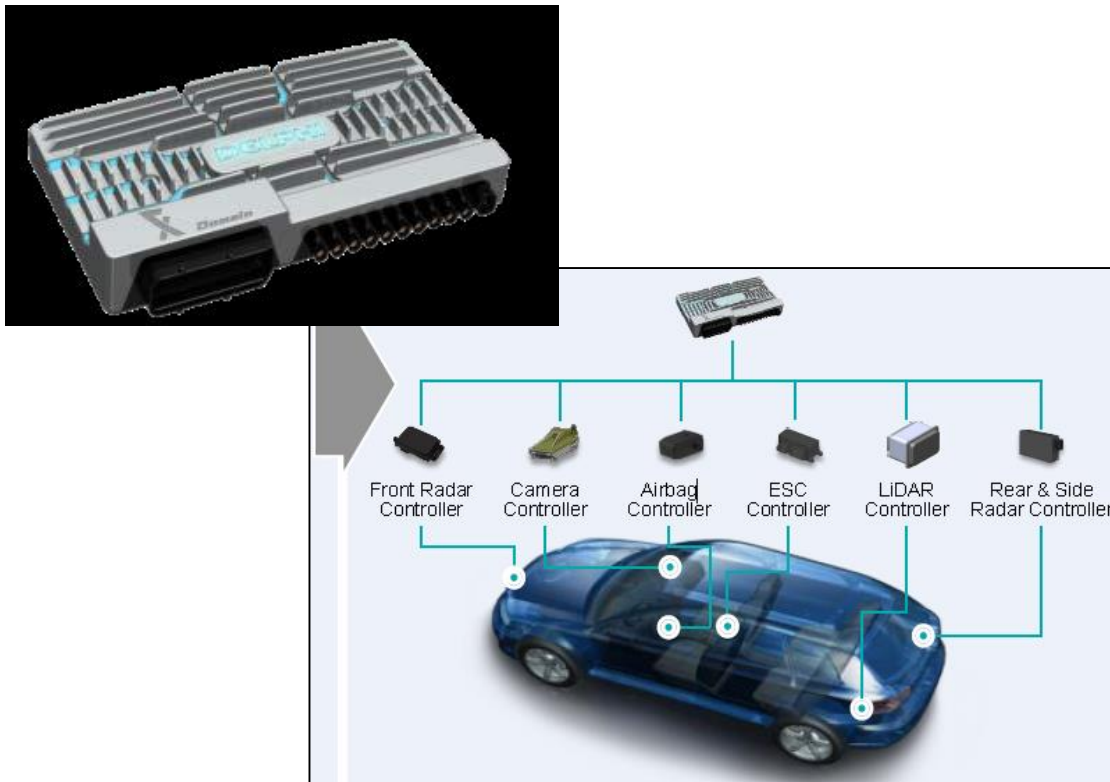
Source: Dr Elmar Degenhart, CEO, Continental CES 2018 Strategy Presentation

<https://www.continental-corporation.com/en/press/fairs-events/ces-2018/continental-at-the-ces-2018-106244>

<https://www.continental-corporation.com/resource/blob/118106/deafe75b7e11426dabcc785c0e0316ab/2018-01-09-strategy-key-figures-data.pdf>

Examples of ADAS Architectures

Delphi (Aptiv) Multi-Domain Controller (MDC)



Audi ZFAS Centralized ADAS Module

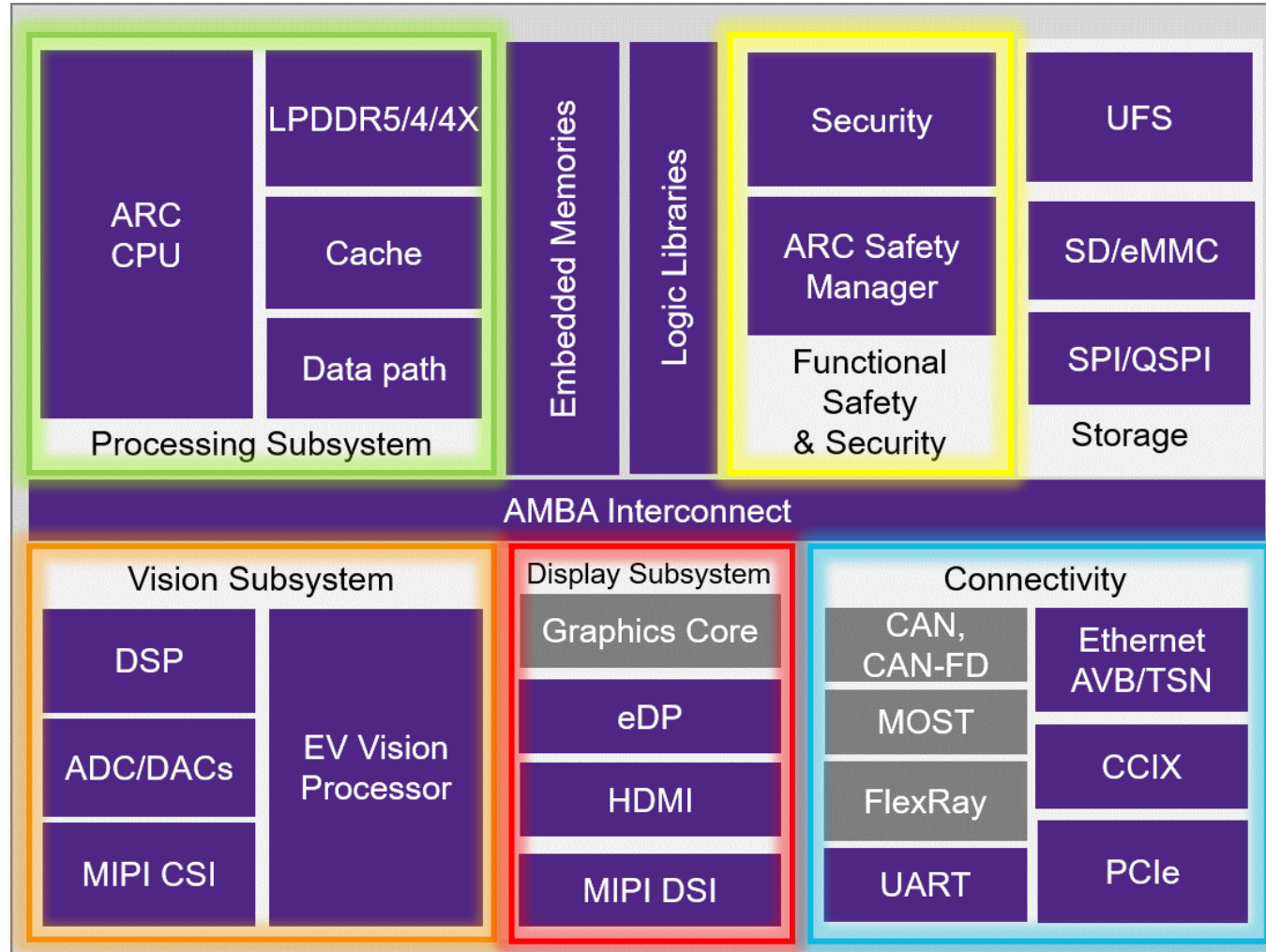
The diagram shows the Audi ZFAS Centralized ADAS Module architecture, featuring a central processing unit connected to various sensors and controllers. The architecture is supported by several key components:

- Infineon - Aurix**
 - ▶ Hosting different functions
 - ▶ A-SIL D compliant
 - ▶ Interface to the Car architecture
- Altera - Cyclone**
 - ▶ Responsible for Sensor Fusion
 - ▶ Preprocessing Ultrasonic Sensors
 - ▶ Internal Gateway
- NVIDIA K1**
 - ▶ Imageprocessing for Parking
 - ▶ 4 Kameras computed
 - ▶ Drivermonitoring
- MobilEye - EyeQ3**
 - ▶ Frontcamera Image Procoessing
 - ▶ AEB Cars
 - ▶ AEB Pedestrians

The diagram also includes the Audi logo and the slogan "Vorsprung durch Technik".

- System & Component Integration
 - Higher computing, performance and density
 - Same trend as smartphones and servers in last 10 years
- Ongoing development in established suppliers and start-ups

Centralized ADAS typical SoC Architecture



- Interfaces
 - LPDDR5/4/4X, Ethernet TSN, MIPI, HDMI, PCI Express, CCIX, ADC
- Processing with Accelerators
 - Embedded Vision
 - DSP
- Security
- SoC Safety Manager
- Sensor Fusion
- 28-nm → to 16-/14-nm → 8-/7-nm
- Requires Functional Safety

Designing Multi-Domain ADAS Processors for Safety Critical Operations

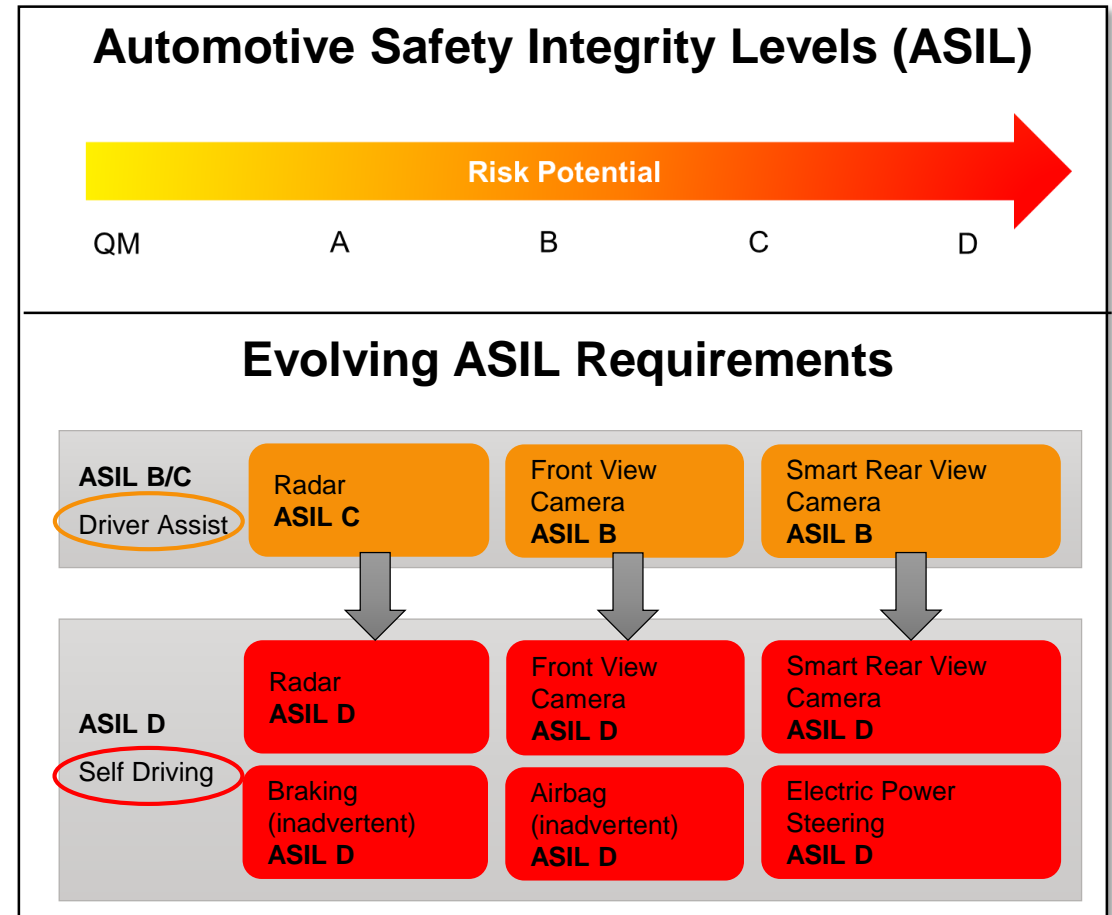


Automotive Functional Safety

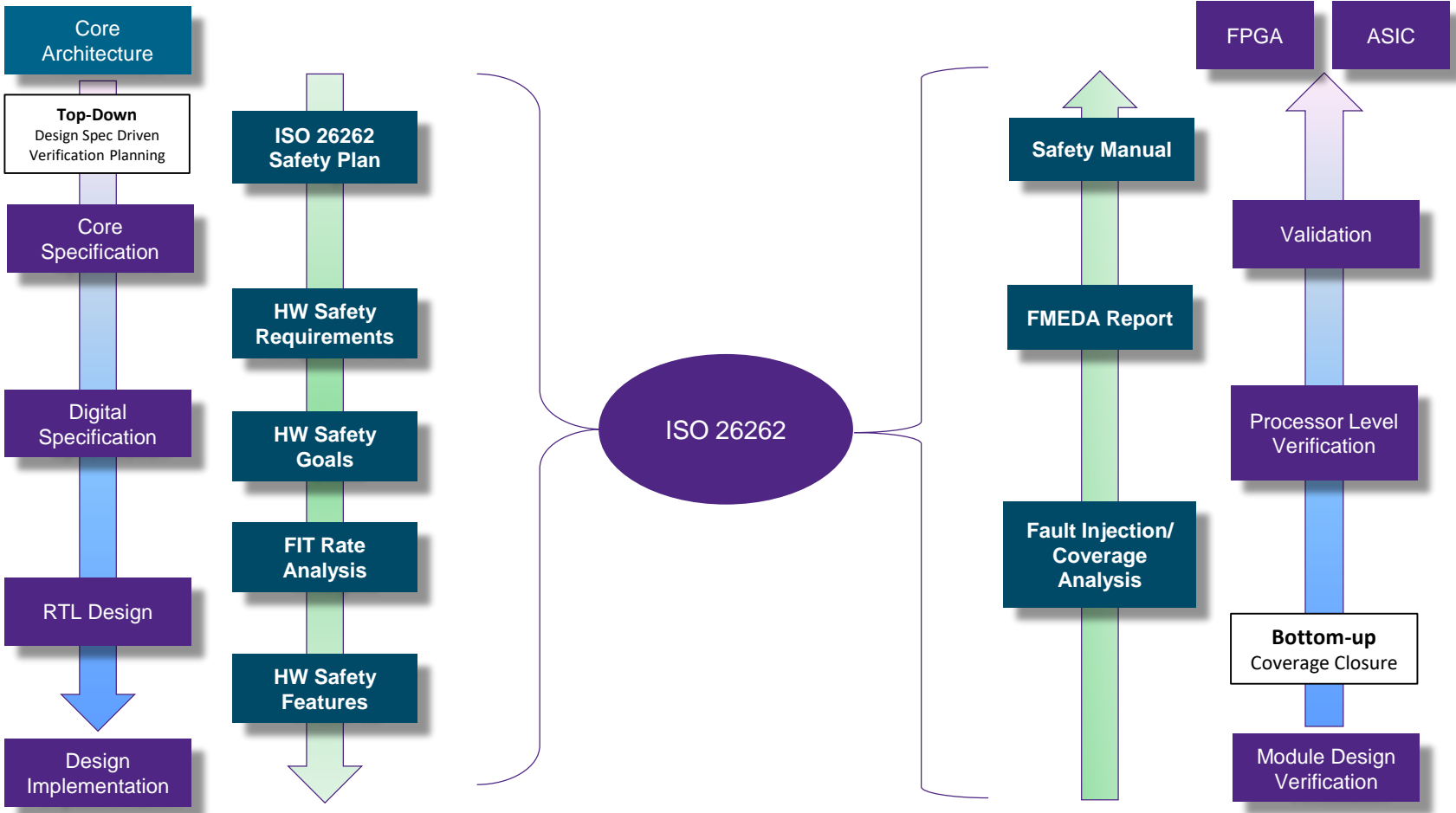
ISO 26262 Standard Focuses on Safety-Critical Components



- “Safety-Critical” systems must minimize risk of catastrophic failures and respond to failures in a predictable manner
- ICs in these systems must meet ISO 26262 functional safety requirements
- Automotive Safety Integrity Level (ASIL) designates risk potential, from QM (lowest) to D (highest)
- Compliance certifications for SoCs granted by accredited providers
 - Product & process reviews
 - Product assessments, audits & certifications



Adapting SoC Development Flows to ISO 26262



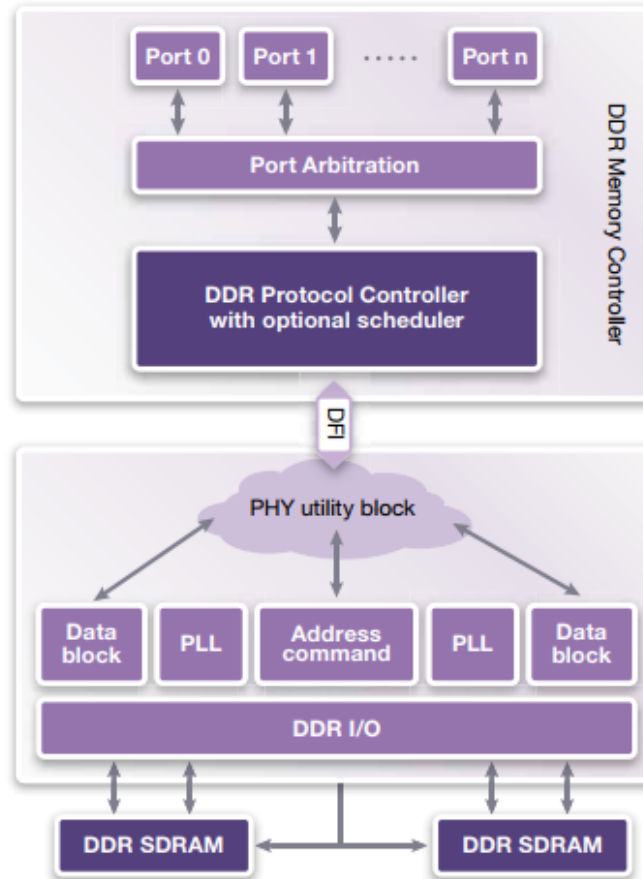
Synopsys Automotive IP with ISO 26262 Functional Safety Features

Example Showing Safety Mechanisms Added to DesignWare LPDDR4 Controller & PHY

Inline ECC – Data Path Protection

On-chip Parity– end-to-end Data Path Protection

Register Parity Protection on critical clocking



Command and Address Path Protection: Parity, ECC and Redundancy

Command and Address Path Protection: Parity and Redundancy

Configuration and Status Registers Parity Protection



Automotive Safety Features

DesignWare MIPI CSI-2 Device Controller IP

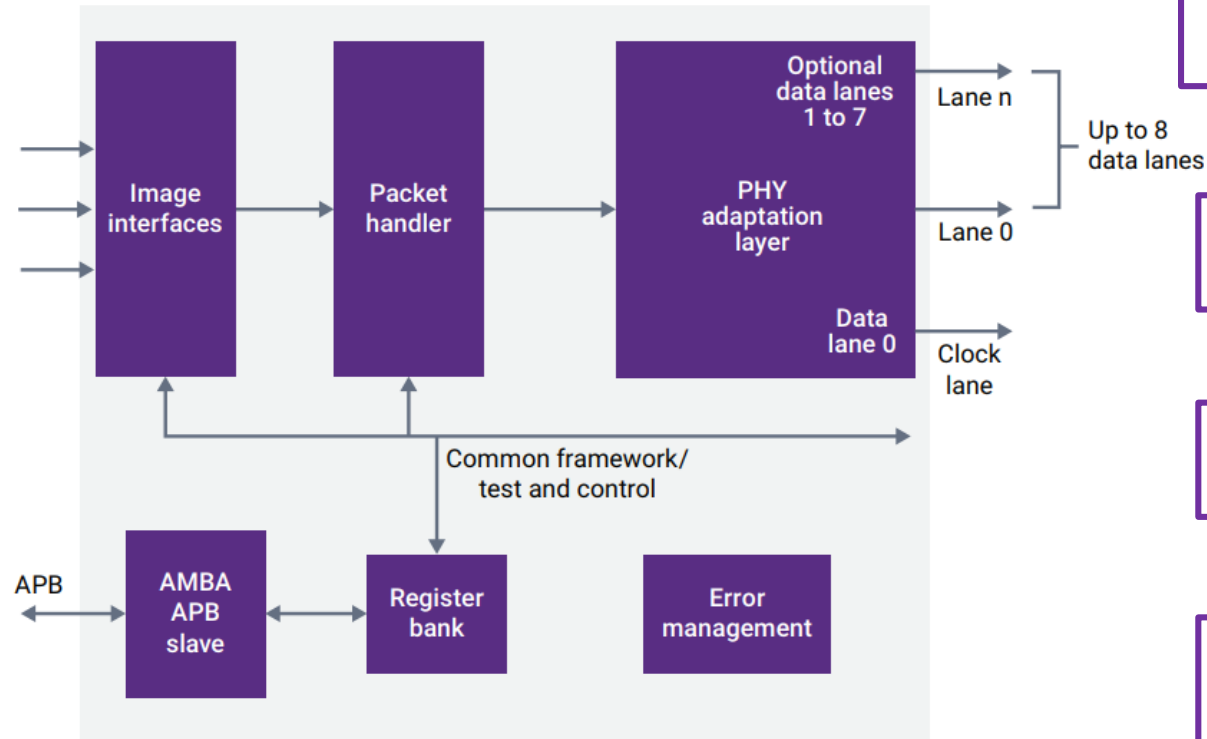


ECC Protection on Packet Header stored in Memory

ECC Protection on IDI/IPI Packet Header

Parity Protection on IPI Data Path

Parity Protection on Configuration Registers



IPI/IDI Overflow Protection

CRC Protection on Packet data path

IDI Header and payload Data checks

Module Redundancy Protection for critical logic

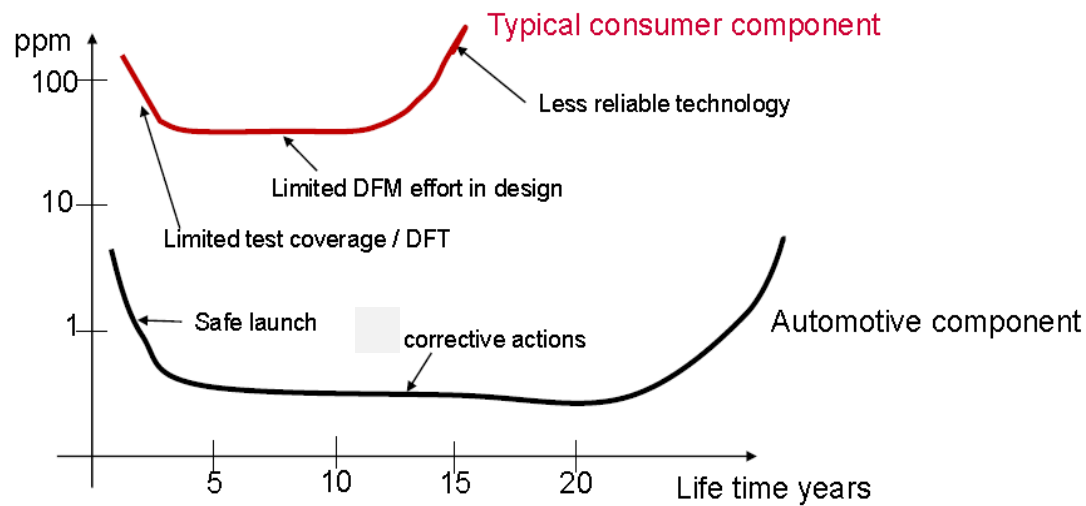
Certification for ISO 26262 Part 5 HW

Automotive Reliability

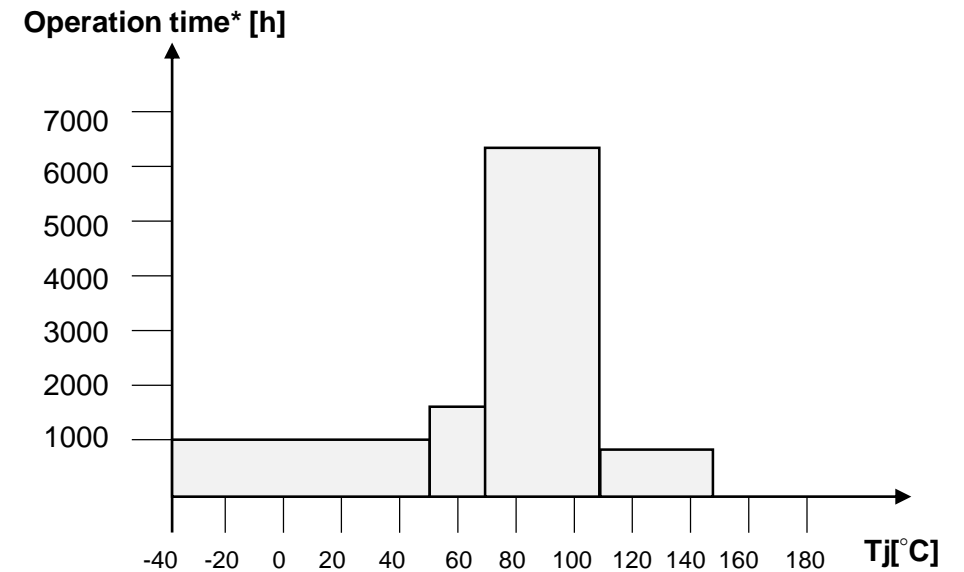


Synopsys Has Defined Internal Reference Temp Profiles Based on Multiple Automotive Engagements

Target Low PPM Automotive Reliability vs. Consumer



Temperature Mission Profile* Industry Example



Duration (h)	Percentage (%)	T_j component ($^{\circ}\text{C}$)
1000	10	48
1600	16	71
6500	65	108
890	9	150

* Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications, ZVEI, May 2015

Synopsys Automotive Grade IP

Reduce Risk and Accelerate Qualification for Automotive SoCs



Functional Safety

Accelerate ISO 26262 functional safety assessments to help ensure designers reach target ASIL levels



Reliability

Reduce risk & development time for AEC-Q100 qualification of SoCs



Quality

Meet quality levels required for automotive applications

new

Synopsys SG: ISO 9001 Certified for Quality

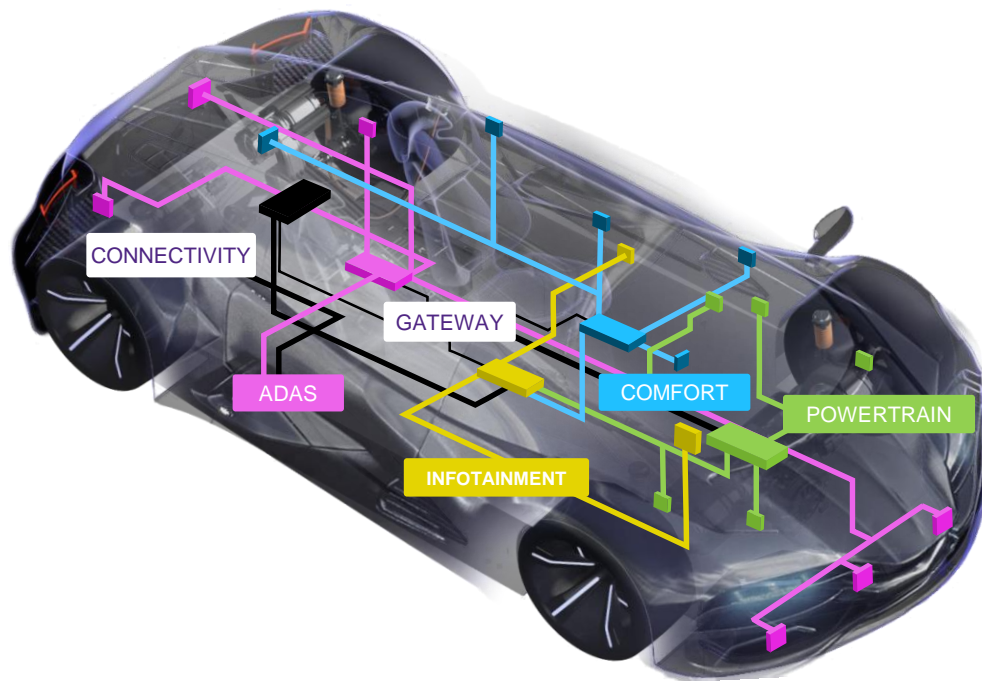
Commitment to Quality Minimizes Integration Risk and Accelerates Time-to-Market



- Synopsys' IP Business Unit or Solutions Group (SG) is committed to maintaining and continually improving its Quality Management System (QMS) modeled on ISO 9001:2015
- SG's QMS is applicable to the development of Synopsys' portfolio of DesignWare IP and tools at worldwide Synopsys sites
 - Helps ensure IP quality, minimizing integration risk
 - Increases confidence in IP development processes, eliminating the need for customers to perform 2nd party quality audits
 - Implements key clauses of IATF 16949 in our QMS, supporting additional automotive requirements
- SG's QMS is ISO 9001:2015 certified by 3rd party: BSI

DesignWare IP Portfolio for Automotive Applications

Accelerates Qualification of Automotive SoCs



IP Portfolio

Ethernet AVB/TSN	Embedded Memories
LPDDR5/4/4X	Logic Libraries
MIPI CSI-2/DSI	PCI Express
HDMI	Mobile Storage
USB Host & Device	Data Converters
Star Memory System	Star Hierarchical Sys.
ARC EM & HS Processors	Embedded Vision Processors
Security: Encryption & Decryption	Sensor & Control IP Subsystem
NVM	Datapath IP

ASIL B/D Ready IP with AEC-Q100 Design & Testing and Automotive Quality Management targeting ADAS, infotainment and MCU applications

Synopsys Delivers Automotive-Grade IP in TSMC 7-nm Process for ADAS Designs

DesignWare IP in FinFET Processes Adopted by More Than a Dozen Companies

Press Releases

Synopsys Delivers Automotive-Grade IP in TSMC 7-nm Process for ADAS Designs

DesignWare IP in FinFET Processes Adopted by More Than a Dozen Companies Designing ADAS and Autonomous Driving SoCs

MOUNTAIN VIEW, Calif., Oct. 1, 2018 /PRNewswire/ --

Highlights:

- Broad portfolio of controller and PHY IP in the 7-nm process includes LPDDR4X, MIPI CSI-2 and D-PHY, PCI Express 4.0, and security IP
- IP solutions implement advanced automotive-grade design rules for TSMC 7-nm process to meet the reliability and 15-year automotive operation requirements
- ISO 26262 ASIL Ready IP with safety packages, FMEDA reports, and safety manuals accelerates SoC-level functional safety assessments

Synopsys, Inc. (Nasdaq: SNPS) today announced delivery of automotive-grade IP in TSMC's 7-nanometer (nm) FinFET process. The IP portfolio includes LPDDR4X, MIPI CSI-2, D-PHY, PCI Express® 4.0, and security IP implement advanced design rules to meet the stringent reliability and operation requirements for automotive-grade SoCs (SoCs). The delivery of automotive-grade IP in TSMC's



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ASIL Ready DesignWare IP Accelerates Path to ISO 26262 Compliance*



*Certification for ISO 26262 Part 5 HW Development

DesignWare IP	ASIL Functional Safety Level	Temperature Grade PHYs, Embedded Memories, NVM
ARC EM22FS Processors	ASIL B and ASIL D	
ARC EV7xFS Vision Processors	ASIL B and ASIL D	
ARC MetaWare Toolkits for Safety	ASIL D	
Embedded Memories 16FFC	ASIL D	Grade 1 & 2
Star Memory System (SMS)	ASIL D	
Star Hierarchical System (SHS)	ASIL D	
EEPROM and Trim NVM	ASIL D	Grade 1 & 2
Ethernet QoS, Ethernet XPCS and 10GMAC	ASIL B	
PCIe 4.0 Controller, PCIe 3.1 Controller & 16FFC PHY	ASIL B	Grade 1 & 2
USB 2.0 & 3.0 Controller & 16FFC PHY	ASIL B	
LPDDR4 Controller & 16FFC MultiPHY v2	ASIL B	Grade 1 & 2
MIPI CSI-2 Controller & 16FFC PHY	ASIL B	Grade 1 & 2
MIPI DSI	Compliance in progress or planned	
Security IP	Compliance in progress or planned	
ARC VPXFS	Compliance in progress or planned	
ARC HS4xFS	Compliance in progress or planned	



In Closing...

- **ADAS:** Fastest growing automotive application: 19% CAGR '14-23
- Synopsys provides ISO 26262 Safety Features integrated into Automotive IP portfolio
 - DDR, Ethernet, USB, MIPI CSI-2/DSI, PCIe IP
 - Memories, Logic Libraries and Test & Repair
 - Analog and Non-Volatile Memory
 - ARC EM & ARC Safety Island with Safety Enhancement Package
 - Sensor & Control IP Subsystem
 - VDKs, IP Prototyping Kits
- ISO 26262 ASIL Ready IP, AEC-Q100 Design, Verified & Testing, Automotive Quality Management accelerates qualification of automotive SoCs

For more Information visit synopsys.com/ip-automotive

