Sowmyan Rajagopalan, Founder & CTO
Thalia Design Automation

Bluetooth IP Migration & Leveraging FDSOI Back Gate Biasing feature

December, 2019

Analog IP Design – Decision fork

Design new IPs

- Address new sections of the market
- Increasing revenue
- Targeted customer base
- Exciting

Build a portfolio of analog IPs

- Expand within the existing market
- Stabilise
- Increase revenue – widen the customer base

Not an Either-Or Situation

Analog IP Reuse – Is it a myth ?

- Analog circuit design is impacted by a number of factors
  - Device performance,
  - Technology characteristics,
  - Functional requirements,
  - Design methodology
- Migrating an Analog circuit into a new technology is almost a redesign of an existing IP – custom requirements
  - Even a bandgap requires design redo !!!
- Limited solutions in the market and a shortage of good analog designers exacerbates the problem

- Is efficient Analog IP reuse a myth/dream ?

Thalia – Who are we ?

- Paradigm shift in how Analog IP is reused
- Thalia's unique Re-use Platform as-a-Service (**RePaaS**)
  - allows analog IP vendors to diversify their product range;
  - optimize performance of new and existing IP;
  - and to quickly and efficiently serve market needs whatever their customers' choice of process technology.
- **RePaaS** addresses customers' analog and mixed signal design requirements by combining three elements – **The Trifecta** :
  - proprietary design automation technology that increases designer efficiency and improves quality of results;
  - innovative design methodology – a design based approach rather than a CAD based or circuit synthesis;
  - and an experienced team with proven expertise in RF, analog and mixed signal design

Thalia Story

2011

Thalia is founded

2015

Solutions Offer[illegible]g launche[illegible]
targeting Analo[illegible] Reus[illegible]

- Experienced Delivery Team Established – Avg. 20 years of experience

2016

Several customer designs delivered

- RF Front end, Baseband applications

2017

Thalia established in India

2017

Tha[illegible]ec[illegible]me[illegible] IP Reuse
pa[illegible]n[illegible] of c[illegible]ice for
Ca[illegible]na

2018

Thalia expands into Germany

2019

Delivered RF Front end IP in 28 FDSOI technology

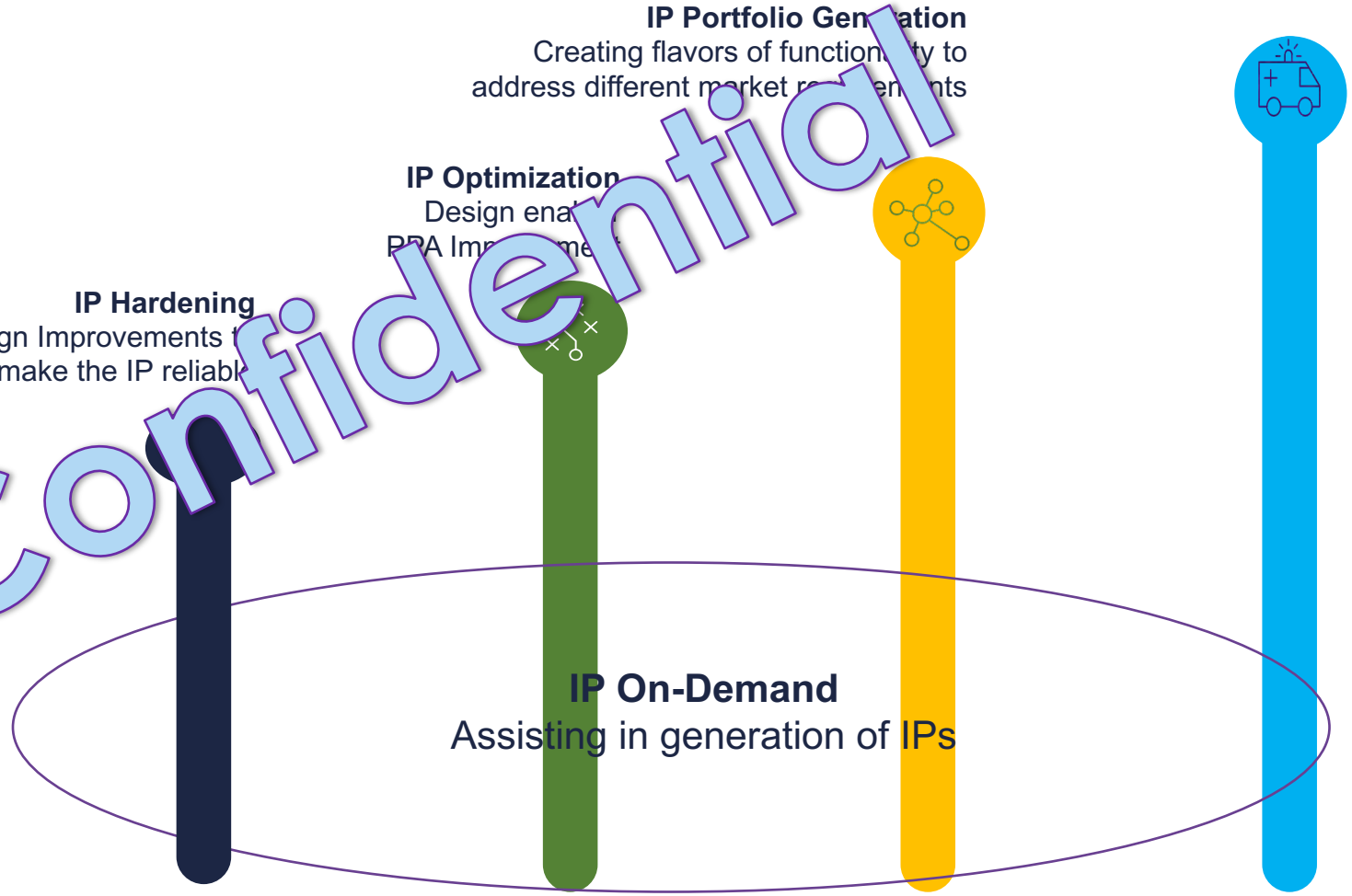
Thalia Value Proposition

IP Migration
Migrating Design across technologies

IP Portfolio Gen ation
Creating flavors of function ty to address different market re en nts

IP Optimization
Design ena
PPA Im me

IP Hardening
Qualify and effect design Improvements t
make the IP reliabl

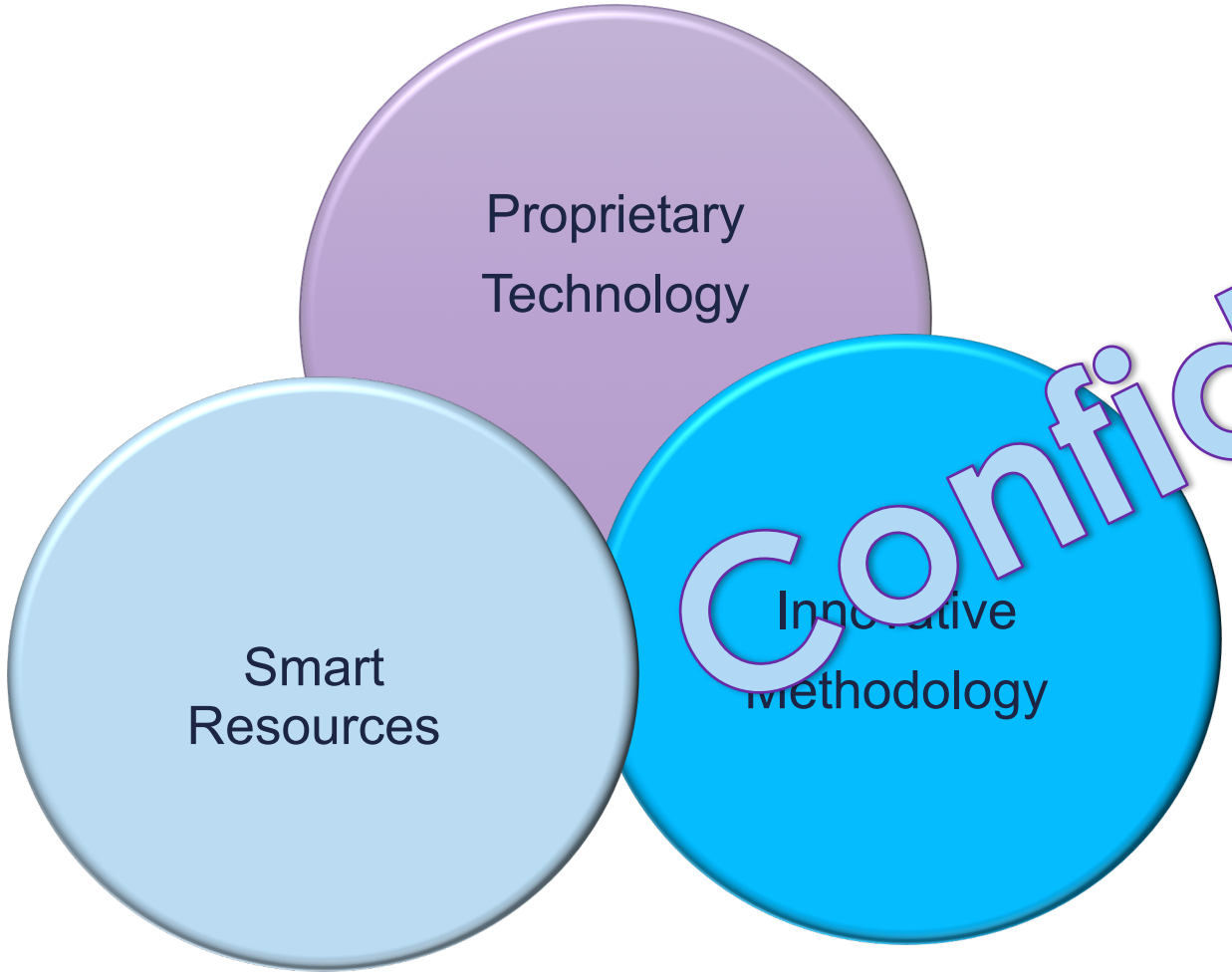


IP On-Demand
Assisting in generation of IPs

Through a combination of

Methodology
High Value Design Services
Innovative Technology

Thalia Unique Selling Point

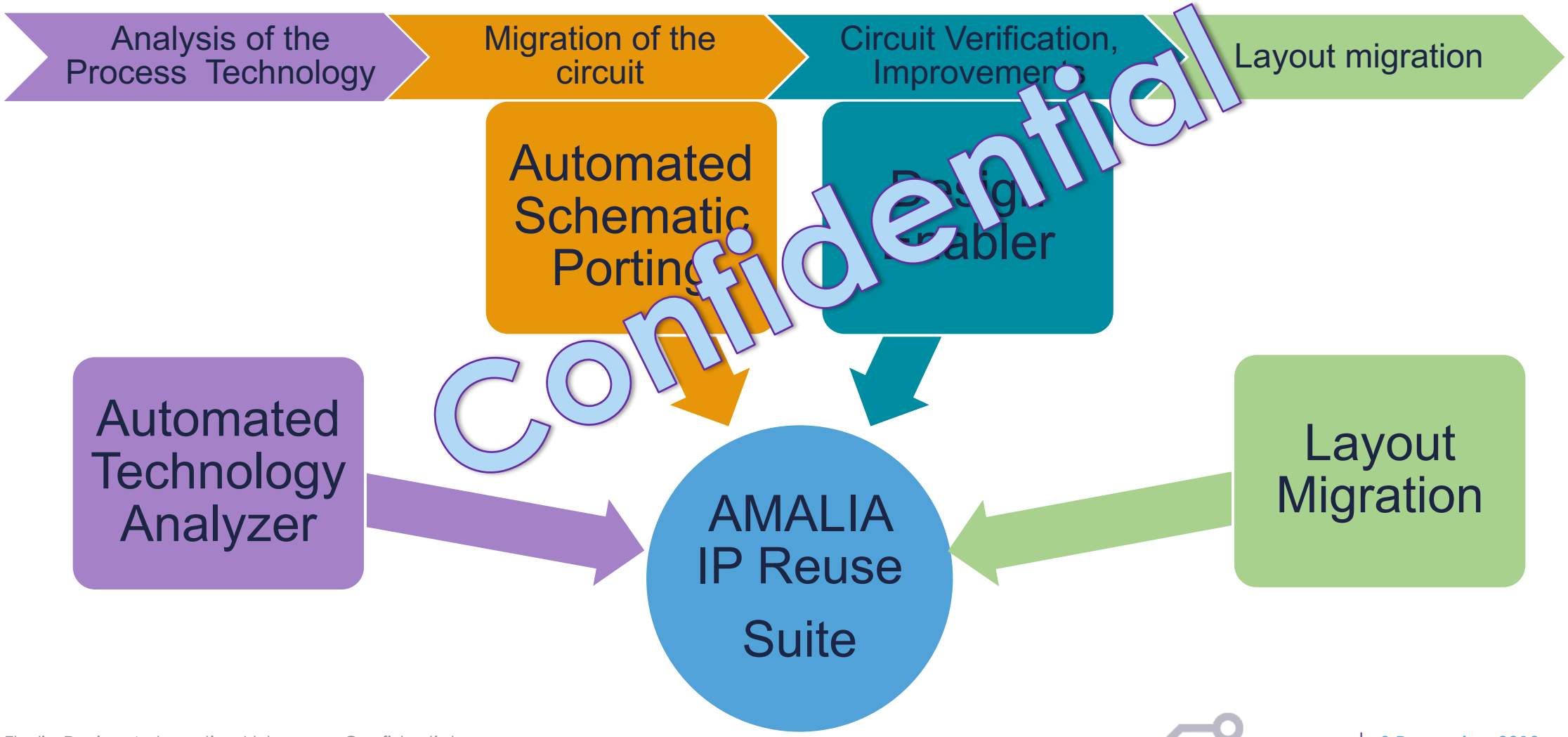


Thalia Technology
- **Schematic + Design +Layout**
- **AI and Algorithms**

Thalia Methodology
- **Targeted automation**
- **Process Technology Analysis**

Thalia Unique Approach
- **Speed**
- **Efficiency**
- **Cost**

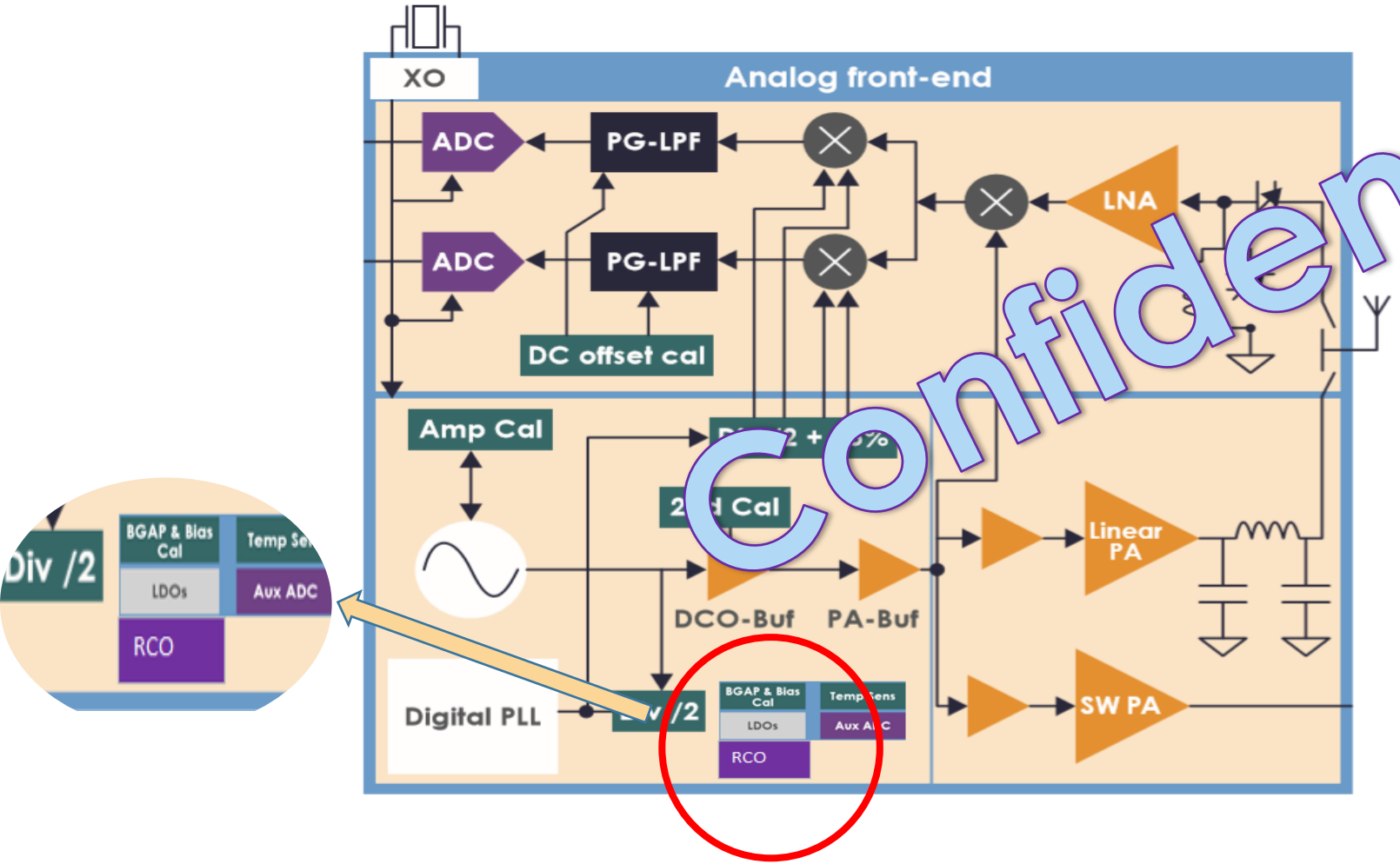
Amalia™ Technology



Automated Process Technology Analysis

- A design centric approach
- Mapping based not only on parameter names/values or callback limits
- Device level simulations to match Ft, Vth, gm, gm/Id, Vds-Ids curves and other second order effects
- Circuits similar to base design post migration, comparable performance and hence lesser design iterations

Bluetooth IP Reuse & FDSOI Techniques

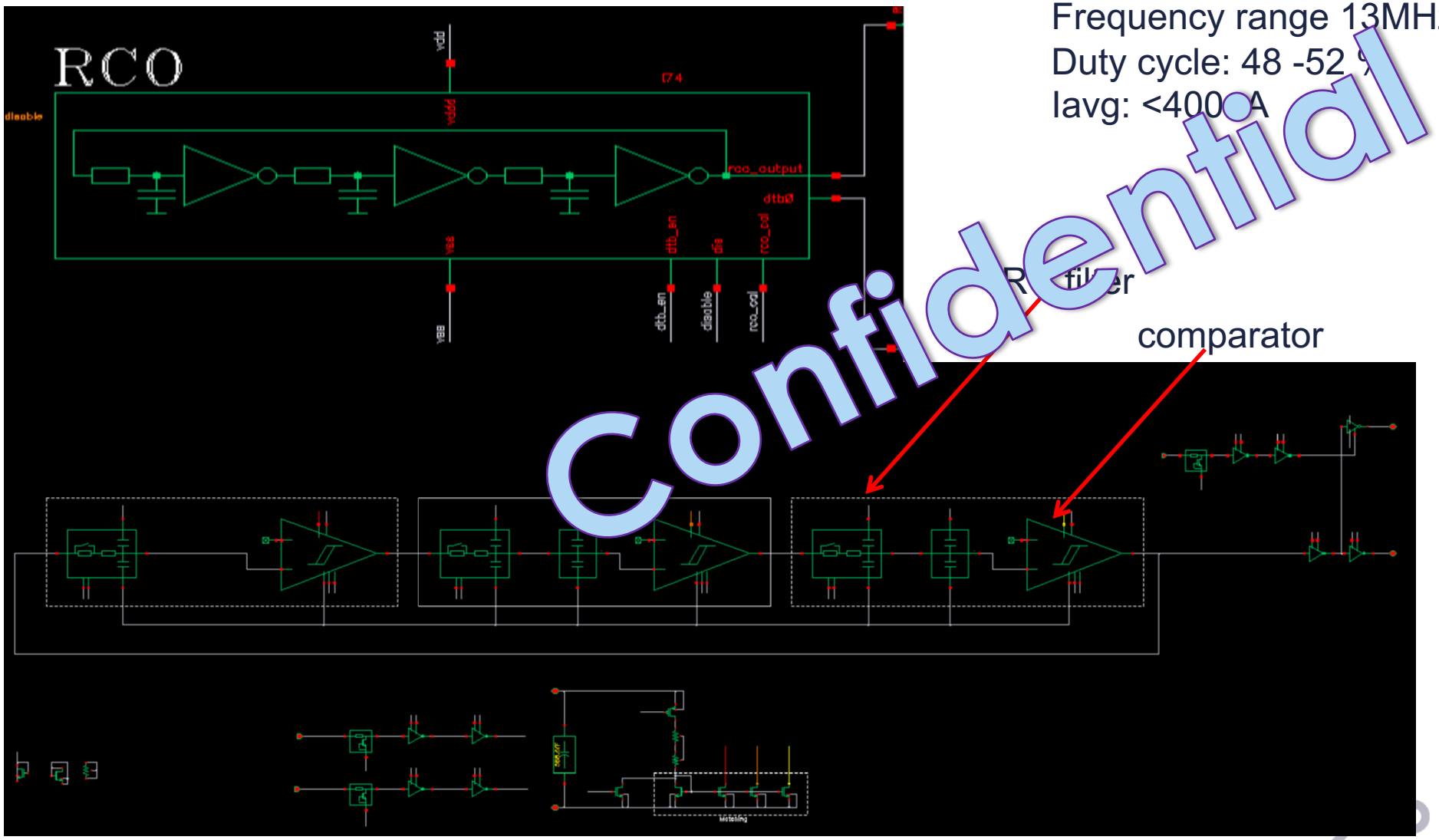


Top Level Specifications

- RF Front-end IP for Bluetooth low energy and IEEE 802.15.4 in the 2.45 GHz ISM band
- Compliant to Bluetooth core specification 4.2 and to IEEE 802.15.4-2011 clause 10 (DSSS-OQPSK)
- Prepared for Bluetooth 5 (2 Mb/s and Long Range)

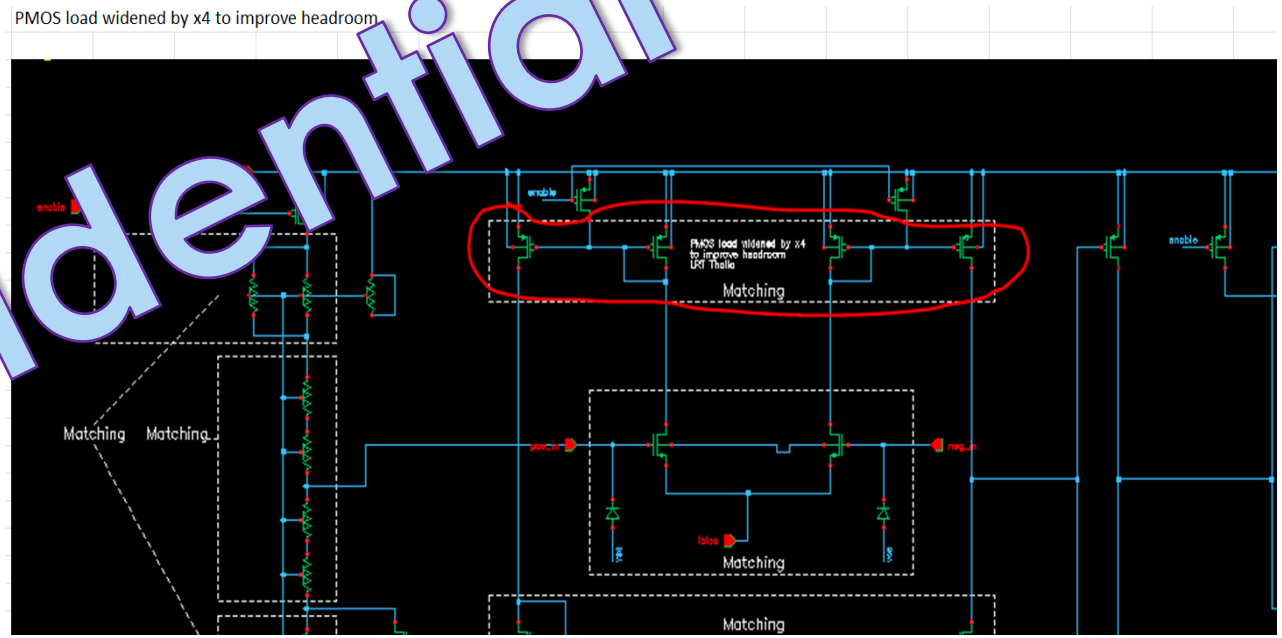
RCO

Specification:
Frequency range 13MHz-52MHz
Duty cycle: 48 -52 %
Iavg: <400 uA



Process differences strikes back !!

- Vt of the nfet and pfet between the technologies were different
- Headroom pressure
- To maintain the required drive, the W of mirrors had to be increased (and L). Increased area
- So flipwell lvtfets were used and Vsb altered to reduce Vt



Design Example: RCO – Thalia's Solution

- Targeted automation to provide incremental time and cost savings – full automation doesn't work in Analog

Business Value: Analog Migration

Parameter	Nominal
Vdd	900m
temperature	27
topinclude.scs	top_tt

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
PVT	i_avg	245.7 uA	< 500		pass	119.8 uA	411.6 uA
PVT	Duty Cycle Freq_low	50.43 %	range 40 60		pass	47.82 %	51.5 %
PVT	Duty Cycle Freq_high	49.51 %	range 40 60		pass	46.97 %	50.75 %
PVT	Frequency_Comp_f_high	26 MHz	range 13 52		pass	15.83 MHz	MHz
PVT	Frequency_Comp_f_low	15.18				9.235	
PVT	Startup time	29.94 ns	< 50		pass	0 ns	

Parameter	Nominal
Vdd	900m
temperature	27
topinclude.scs	top_tt

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
PVT	i_avg	240.3 uA	< 500		pass	102.5 uA	414.2 uA
PVT	Duty Cycle Freq_low	50.66 %	range 40 60		pass	49.8 %	50.83 %
PVT	Duty Cycle Freq_high	50.05 %	range 40 60		pass	48.34 %	50.05 %
PVT	Frequency_Comp_f_high	26.95 MHz	range 13 52		pass	15.29 MHz	42.33 MHz
PVT	Frequency_Comp_f_low	15.52				9.387	24.56
PVT	Startup time	16.79 ns	< 50		pass	10.47 ns	33.02 ns

- The circuit was migrated, simulated, design tweak applied and laid out.
- Design expertise along with Design methodology allowed Thalia to identify the right component

Rapid Analog Porting - Reuse Customer Examples

Classification	Examples	Redesign Cycle Time*	Thalia's Cycle Time*
Standard Analog IP	DAC, ADC, PLL	12-[illegible] weeks [~ 2-3 FTE]**	**4-8 weeks [2 FTE]****
Application Analog IP	Bluetooth, GPS/GLONASS	>40-50 weeks [~ 6-8 FTE]**	**18-22 weeks [~ 6-7 FTE]****
Application Analog IP	Dual Band WLAN	>50 weeks [~ 6-8 FTE]**	**22-28 weeks [~ 6-7 FTE]****

(*) Elasped calendar time to Specification Compliant Design
(**) FTE : Full Time Equivalent
Timescales will be impacted by Circuit complexity and process node differences

Customer Testimonial

Kave Kianush, Catena Vice President and Chief Technology Officer

- "We're taking a new approach, which represents a fundamental shift in the way analog IP is created and delivered.
- Our relationship with Thalia helps us to deliver exactly the right feature and performance combination for our customers, against ever more demanding time-to-market and cost requirements.
- Thalia's combination of novel design automation technology and analog design expertise is unique in the market.
- **We've already seen a positive impact on our ability to deliver against tight customer deadlines."**

- https://www.thalia-da.com/catena-selects-thalia-da-to-facilitate-analog-ip-re-use/

Summary: Re-inventing Analog Reuse

- RePaaS – A platform that delivers efficient reuse of Analog IP
- Unique combination of Technology, Methodology and Design experience
- Reduced design cycle time and hence lower cost –> **up to 50% time and cost savings**
- Proven track record - 22nm to 350nm; Samsung, TSMC, UMC, GF, Tower, SMIC, AMS, Tier 1 Technologies
- Direct application in migrating IPs – Off the shelf IPs

- Contact us sales@thalia-da.com