



IP SoC 2019 Santa Clara - For Panel Discussion

**Frankwell Lin
President
Andes Technology**

Andes Technology Corporation

- A 14-year-old public CPU IP company
- >1B Andes-Embedded SoC shipped in 2018. >3.5B cumulatively



- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
 - Chair of P-extension (Packed DSP/SIMD) Task Group
 - Co-chair of Fast Interrupt Task Group

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rv64-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

SiFive bluespec
redhat
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LLVM

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM
- Talk yesterday afternoon
- Poster on Tuesday night
- RV32IM(A)FD support upstream
 - Missing hard-float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Rust port in progress
 - Poster on Tuesday

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lowRISC
Berkeley

Linux

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64-based systems
 - Drivers are trickling in now

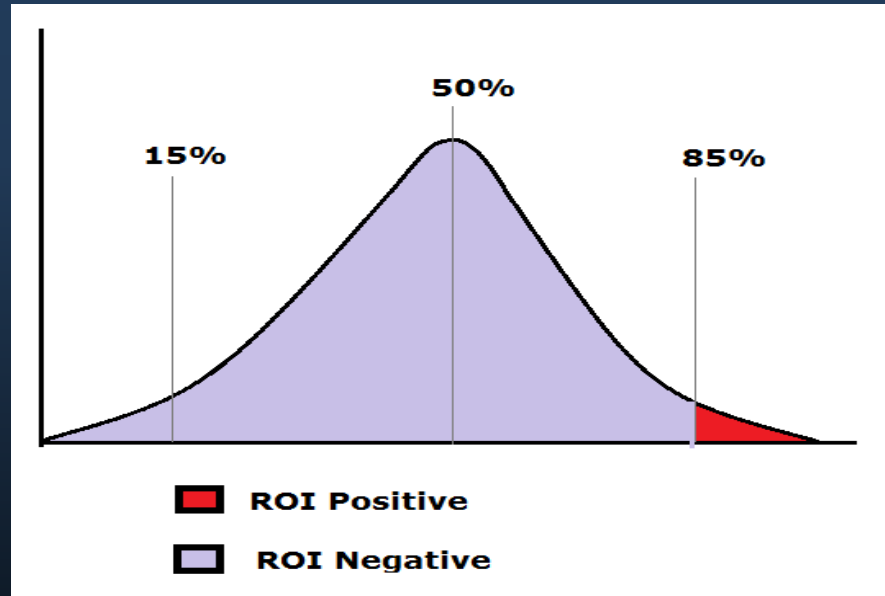
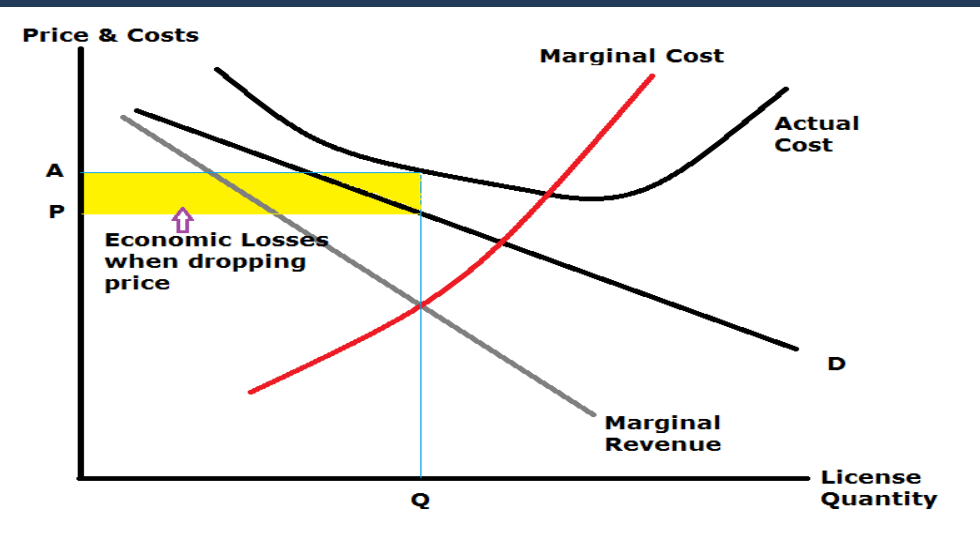
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Free-of-Charge?: It's All About Competition



- **Monopolist: Very hard to keep monopoly now**
- **Chasers: Who's winning?**





Smart Business Model

- Open = Free?
- ISA enters "Open Source Era", but open source chip or core IP are still far from open source
- University may pay for academic works, or some initials, but hard to pay for industrial works
- When you use Google service for free, someone out there pays for you – advertisement
- Smart business model must be healthy one
- Under competition, or co-petition, what is a healthy business model?



Taking RISC-V® Mainstream



Thank you !!

