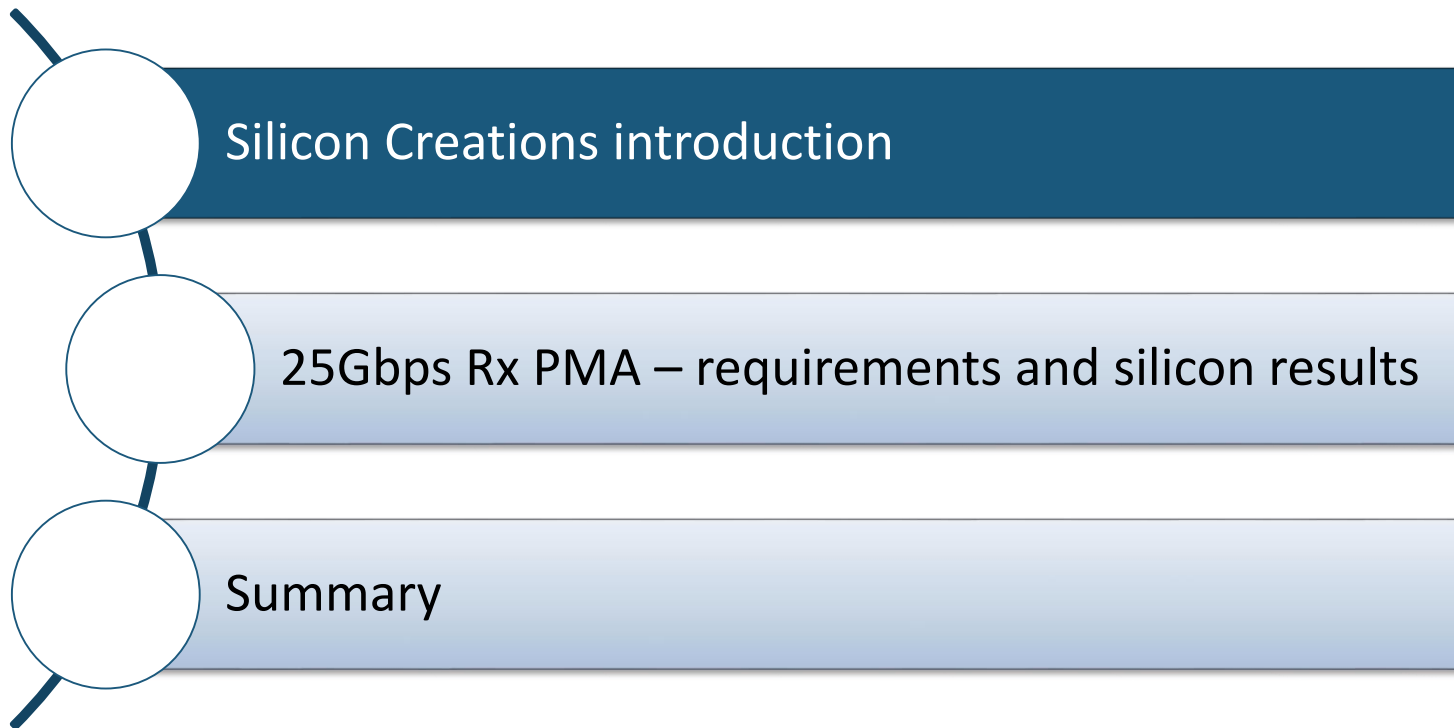


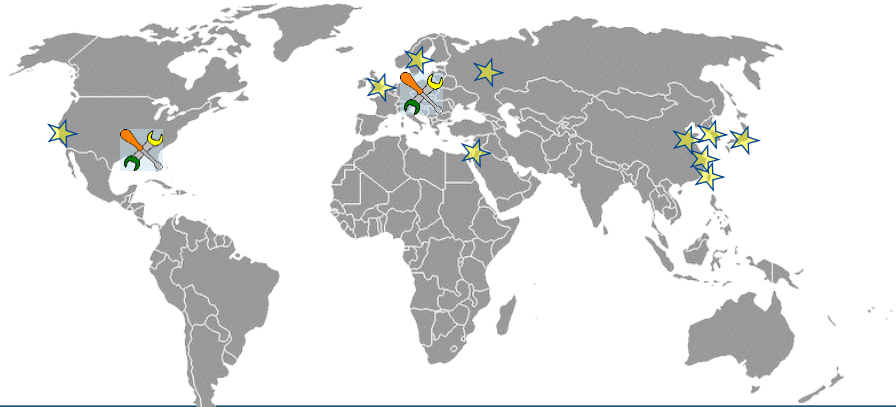
# Comparing silicon to simulations for a 1.3pJ/bit 25Gbps SerDes Rx in 28nm

Andrew Cole, Blake Gray, Jeff Galloway at Silicon Creations



# Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interface
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- IP in mass production from 7nm to 180nm, multiple 5nm PLLs ready



# Some statistics



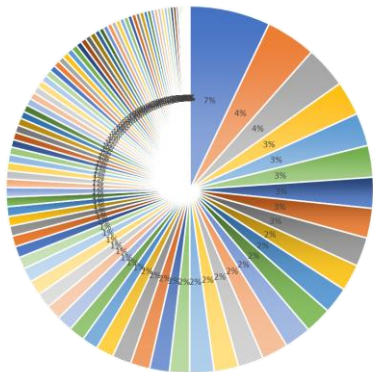
> 200 customers ...

Growing >3/month

> 300 IP products ...

Growing >4/month

> 500 chips in production using our IP... Growing >5/month

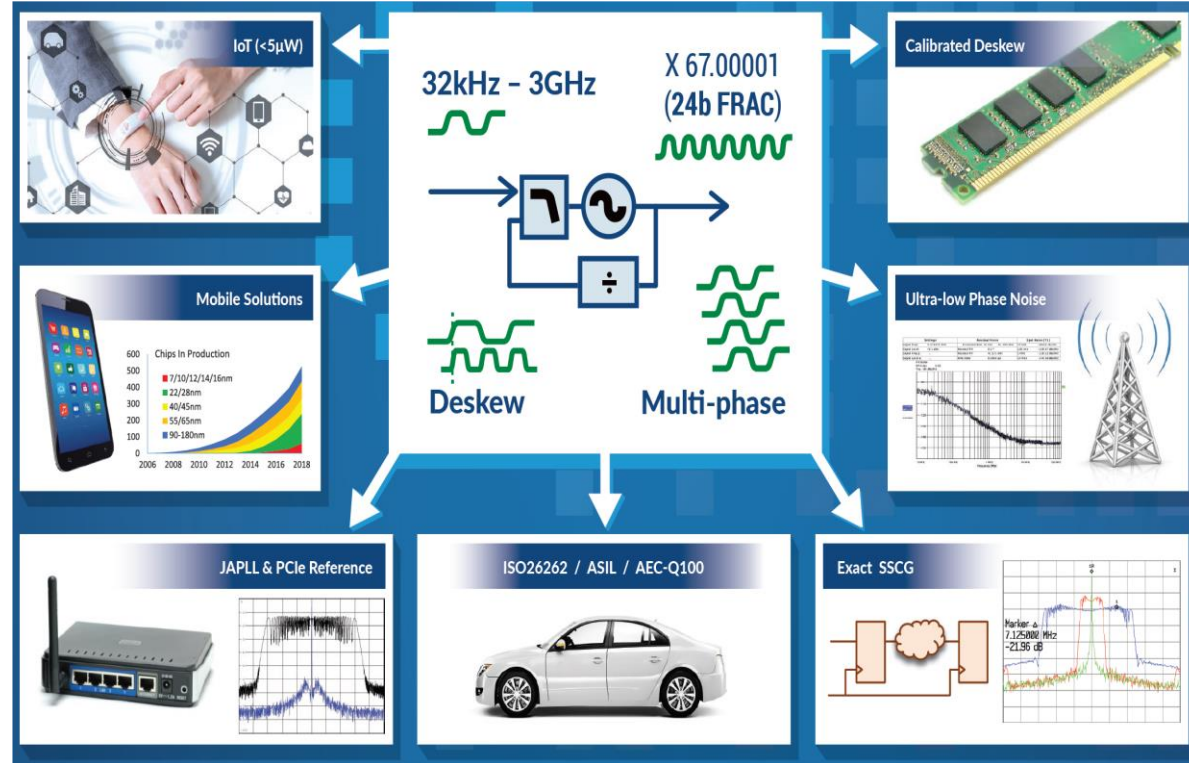


Income from >95 customers in 2018

... we don't depend on any one customer and will be here when you need us to be

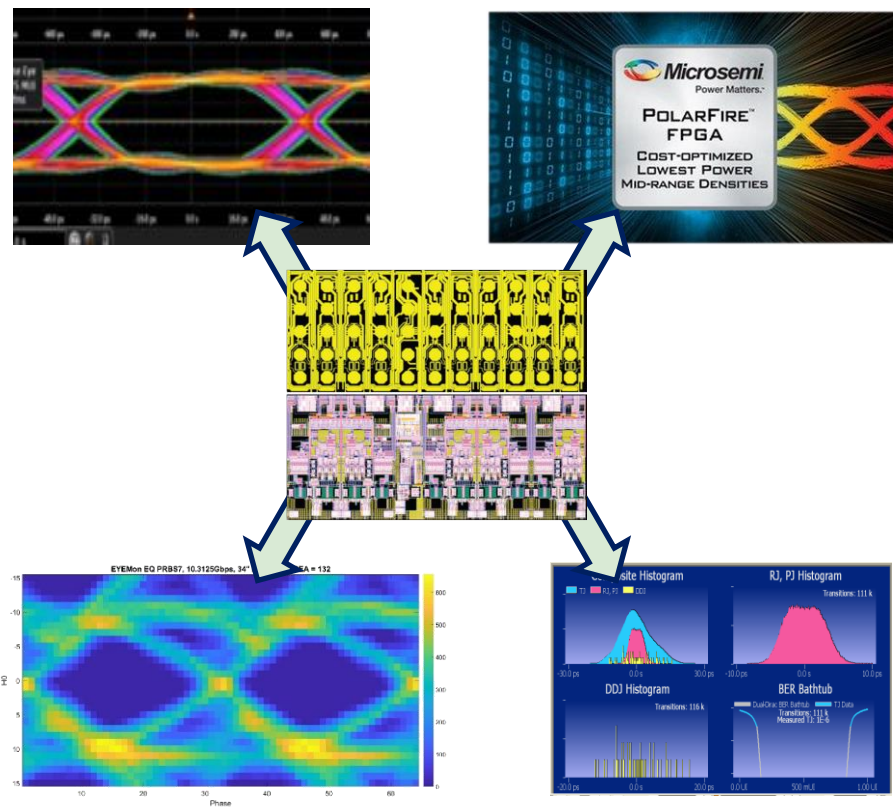
# PLLs from Silicon Creations

- Highest volume analog IPs – robust design and good QA are essential  
e.g. Fractional-N PLL:
  - > 300 MP chips
  - > 3M wafers
  - ... Many billions of these PLLs produced
- PLL products include general purpose, fractional, low jitter AFE,  $\mu$ W IoT, Automotive



# SerDes from Silicon Creations

- Robust and proven from 28nm to 180nm and from <100Mbps to 25Gbps
- Multiprotocol (for FPGA) and targeted protocols
  - SGMII, XAUI, RapidIO, V-by-1 HS/US, CameraLink, FPDLink, JESD204, CPRI, PCIe1-4, 10G-KR, ...
- Come to our booth to learn about our TSMC 12FFC/16FFC multiprotocol PMA





# Lab Testing

Test lab with Matlab controlled equipment – 12 benches



> 100 IP test reports from 7nm to 180nm

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# Awards for quality & support

## TSMC

- 2018 & 2017: “Mixed-Signal IP Partner of the year”
- 2017: “Audience choice paper” – USA OIP
- 2014: “Best Emerging IP vendor”



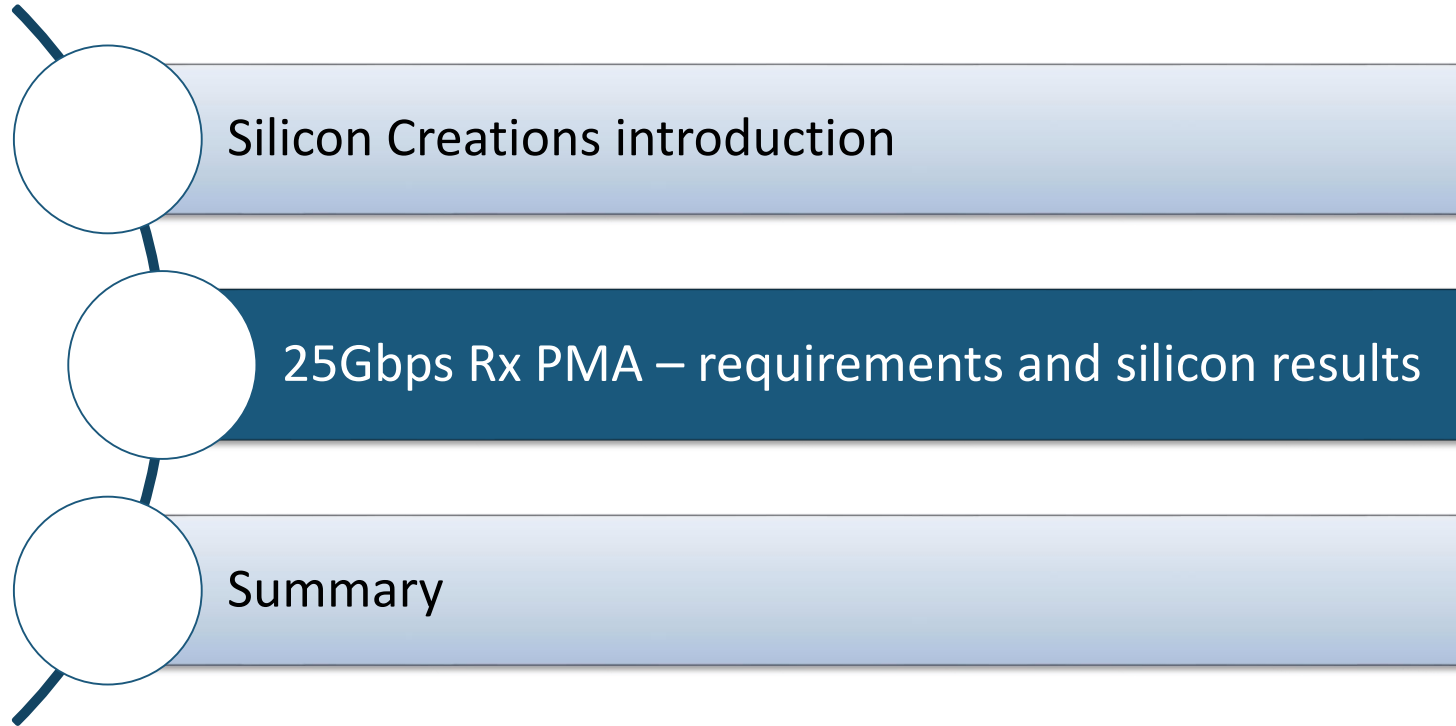


# Awards for quality & support

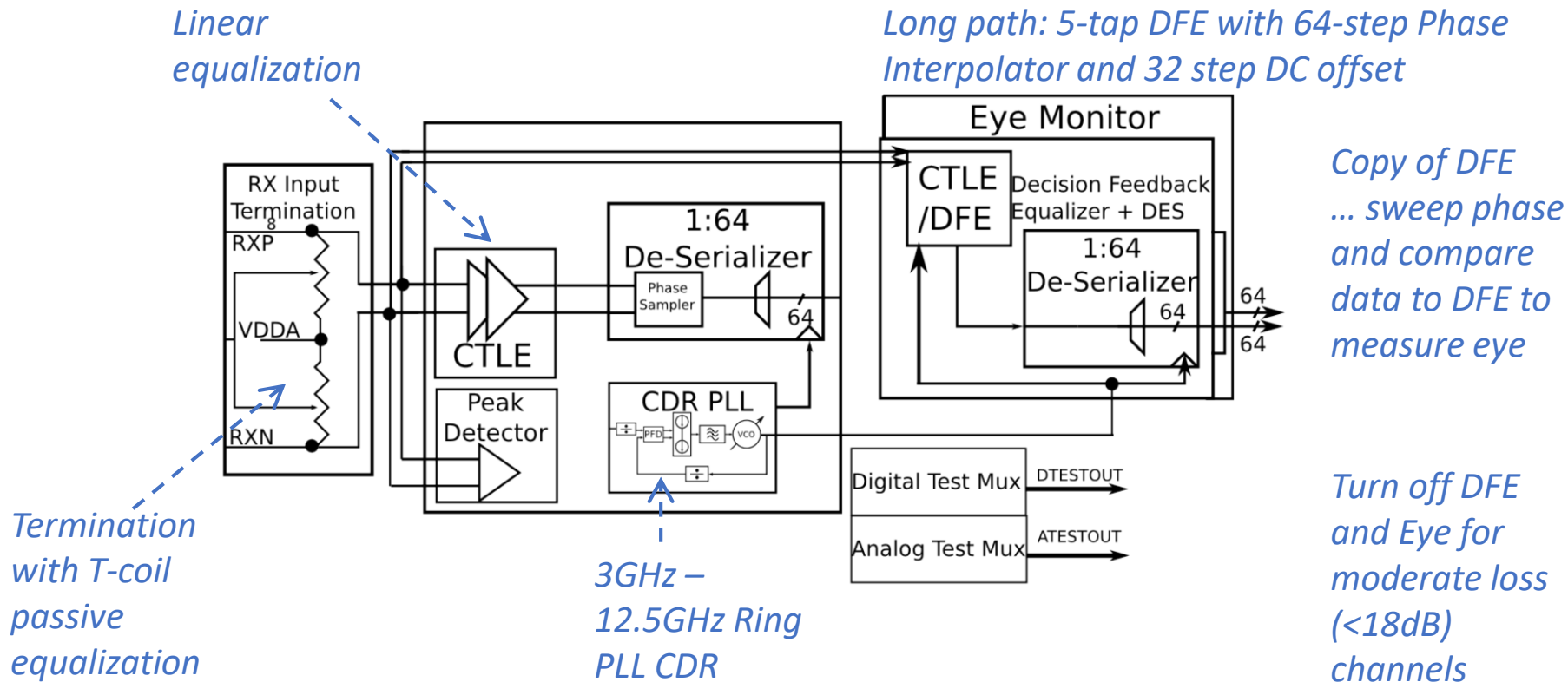
## SMIC

- 2015 & 2016: Best support
- 2014: Production volume growth
- 2013: Best Analog IP



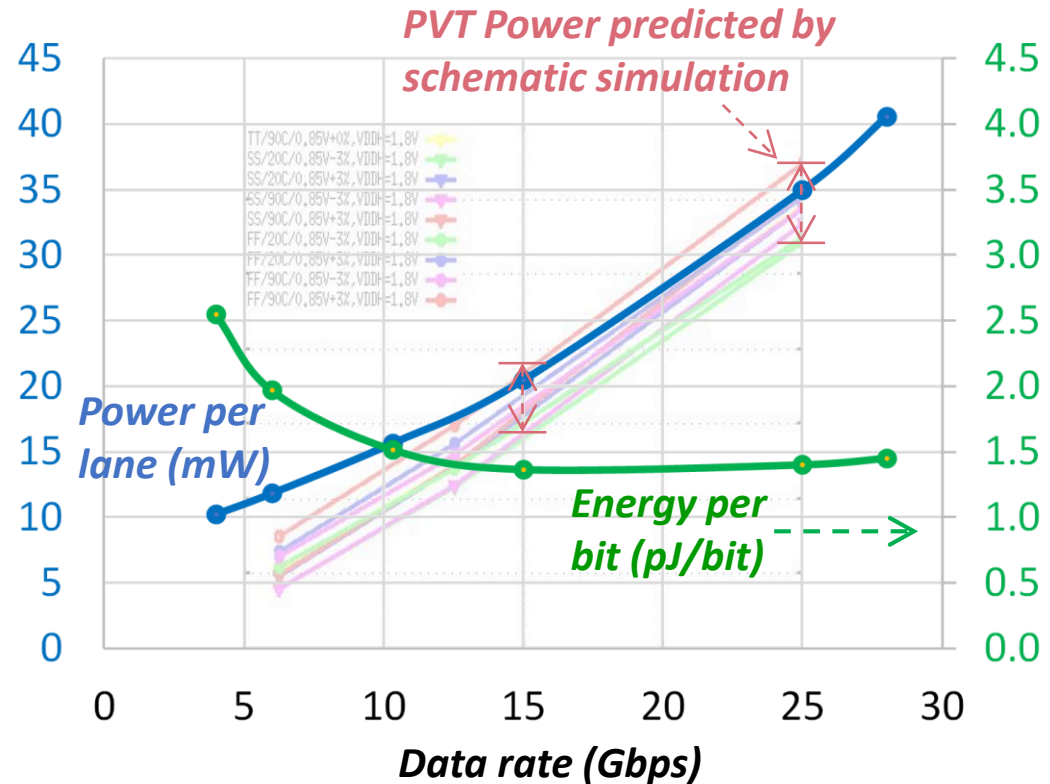


- Customer chip needs to receive  $>5,000\text{Gbps}$  of data
- TSMC 28 HPC+ was determined by other circuits
- Chip will operate in limited temperature range, but has limited heat sinking
- Target power  $<2\text{pJ/bit}$  ( $\text{mW/Gbps/lane}$ ) with  $>18\text{dB}$  (moderate loss) channel
- Following slides present our design and show how silicon is meeting the difficult target with good margin



# Power measurements

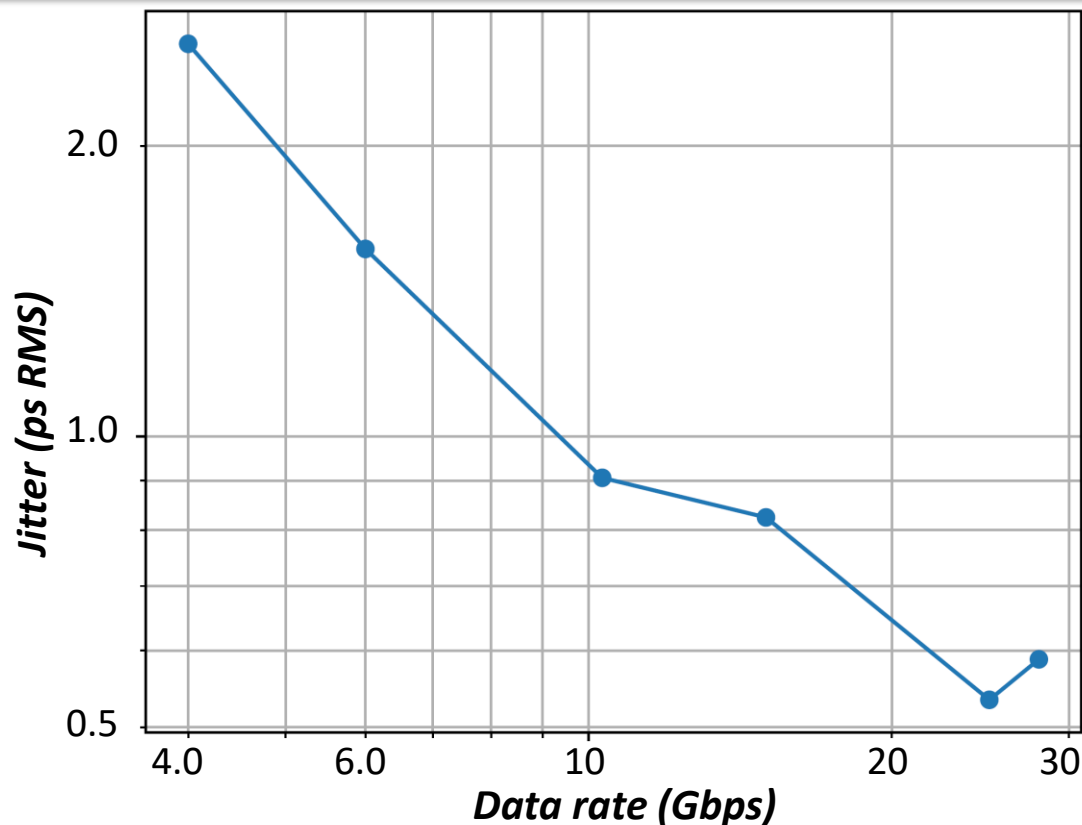
- Typical power measured with DFE off
- Simulations of extracted circuit predicted 1.3pJ/bit at 25Gbps (35mW/lane)
- Simulations and measurements with DFE on (supporting 25dB channel loss) show <2pJ/bit
- Silicon uses only 65% of 2pJ/bit design target for short channels
- Silicon works at 28Gbps over PVT





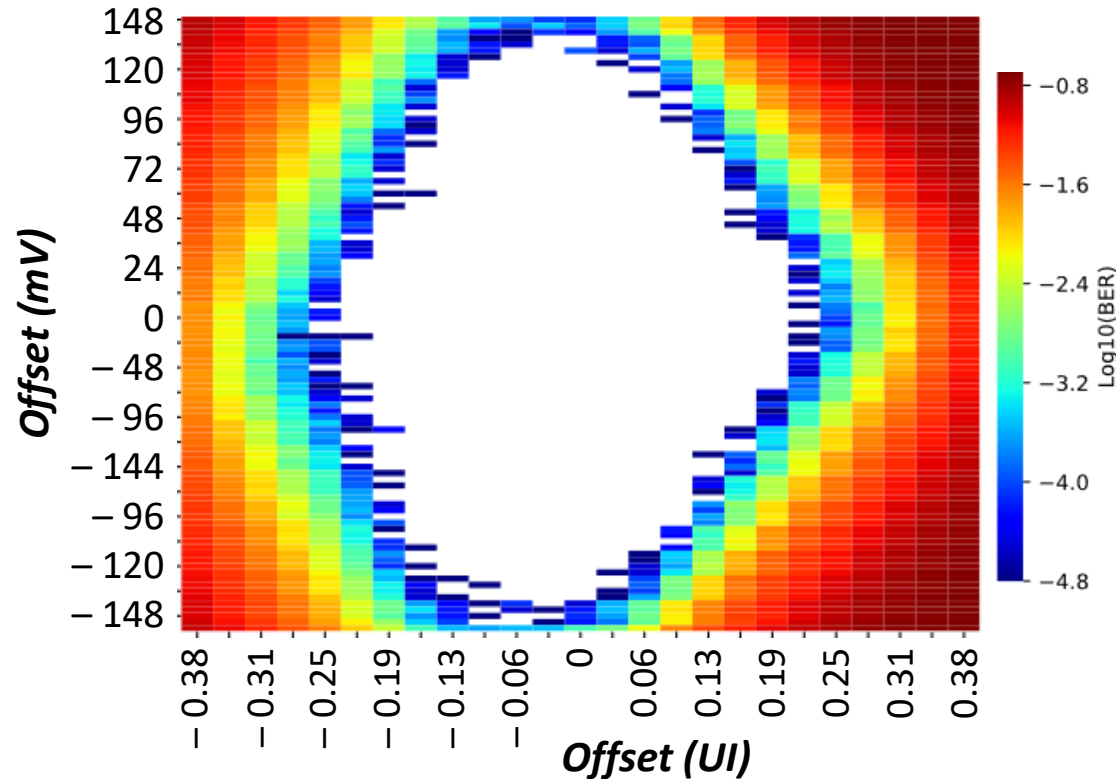
# Jitter in recovered clock

- Ring PLL used for CDR balances power and performance
- Random jitter needs to be low enough for acceptable BER
- Results match expected jitter and are low enough for good BER over design range



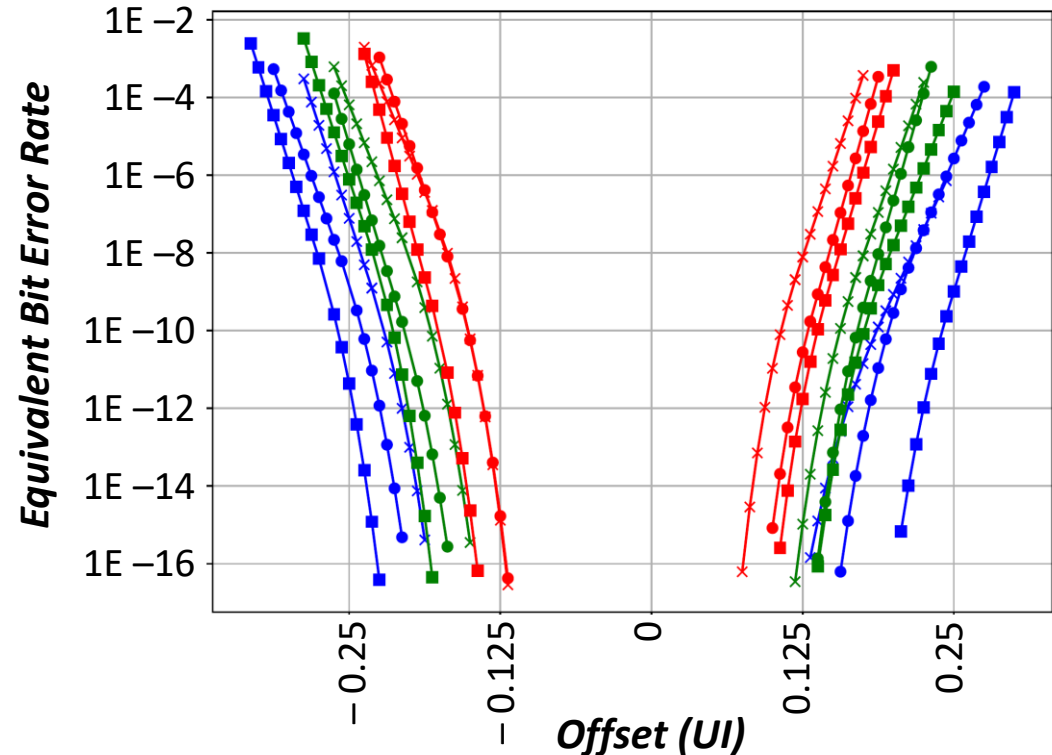
# Eye Diagram at Slicer

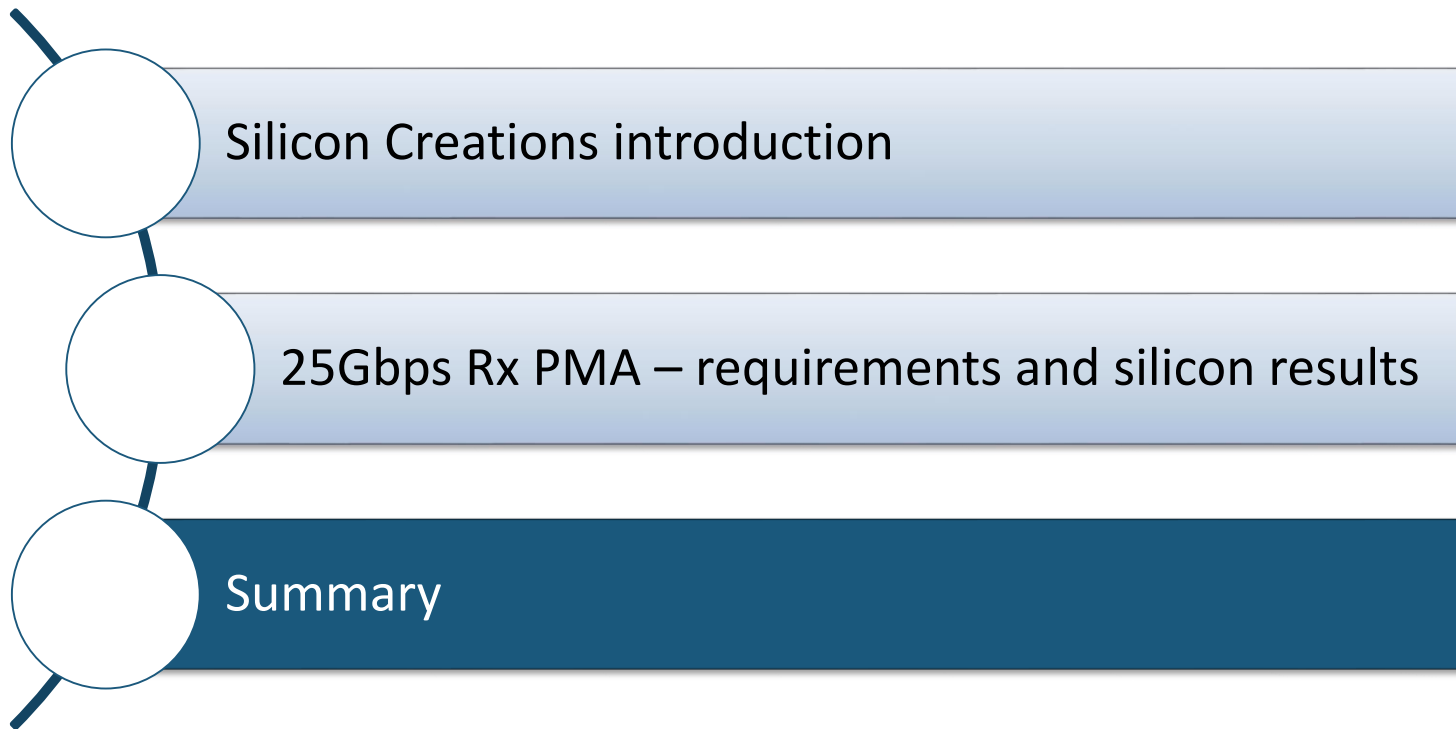
- Eye monitor at slicer can non-destructively measure the eye by sweeping phase and DC offset in copy of DFE
- CTLE/DFE calibration operates to maximize received eye area



# Bathtub at Slicer

- Eye monitor can be used to measure eye opening for large numbers of bits
- Measurements of eye opening with PRBS31 at 25Gbps after CTLE/DFE calibration with 16dB channel loss (20°C to 90°C)
- Results show expected closure with BER and plenty of margin over design range





- Silicon Creations has been providing reliable, high performance clocking and SerDes solutions since 2006
- Our IP is in very high volume production from 7nm, and already available in TSMC 5nm FinFET
- Our versatile ring PLL has excellent PPA, and this has enabled us to build a 25Gbps SerDes receiver in TSMC 28 HPC+
- This receiver beats our lead customer's aggressive power target and operational range with good margin