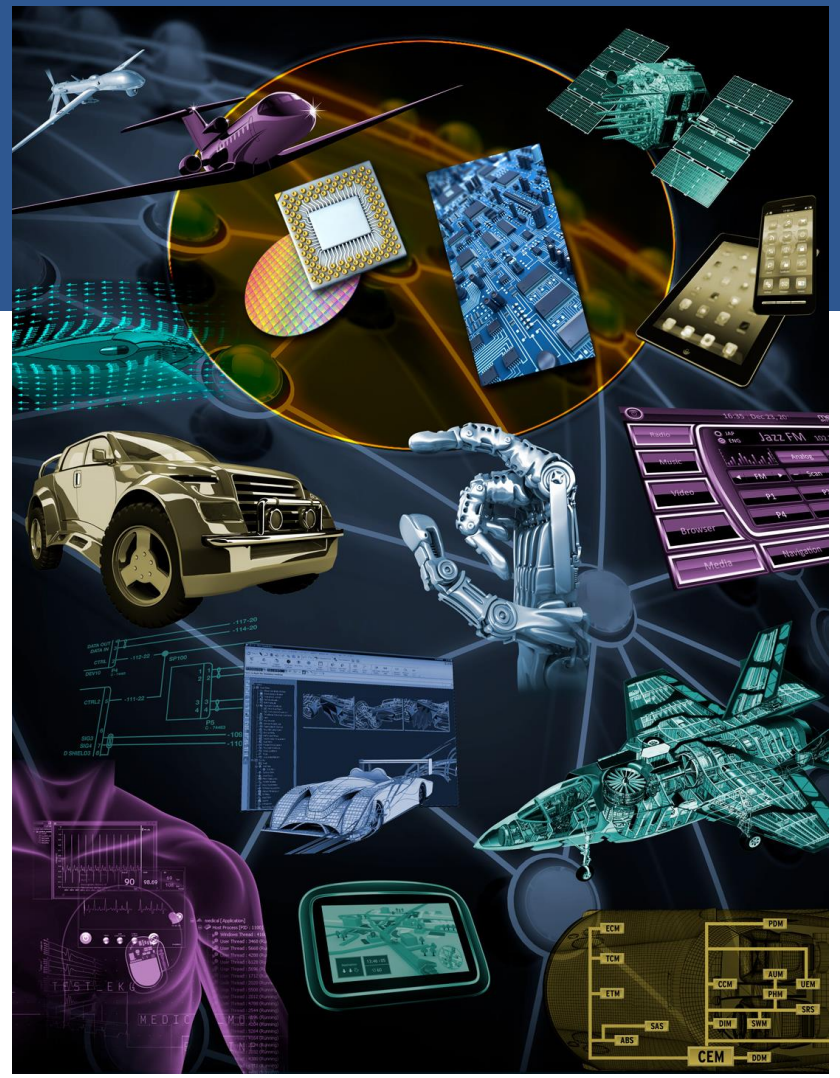
IP SoC, Santa Clara

Top 10 Techniques to Reduce Power & Cost with Optimum Selection of Memory IPs for SOCs



Farzad Zarrinfar

Managing Director of IP Division

https://www.mentor.com/products/ip/

April 9, 2019

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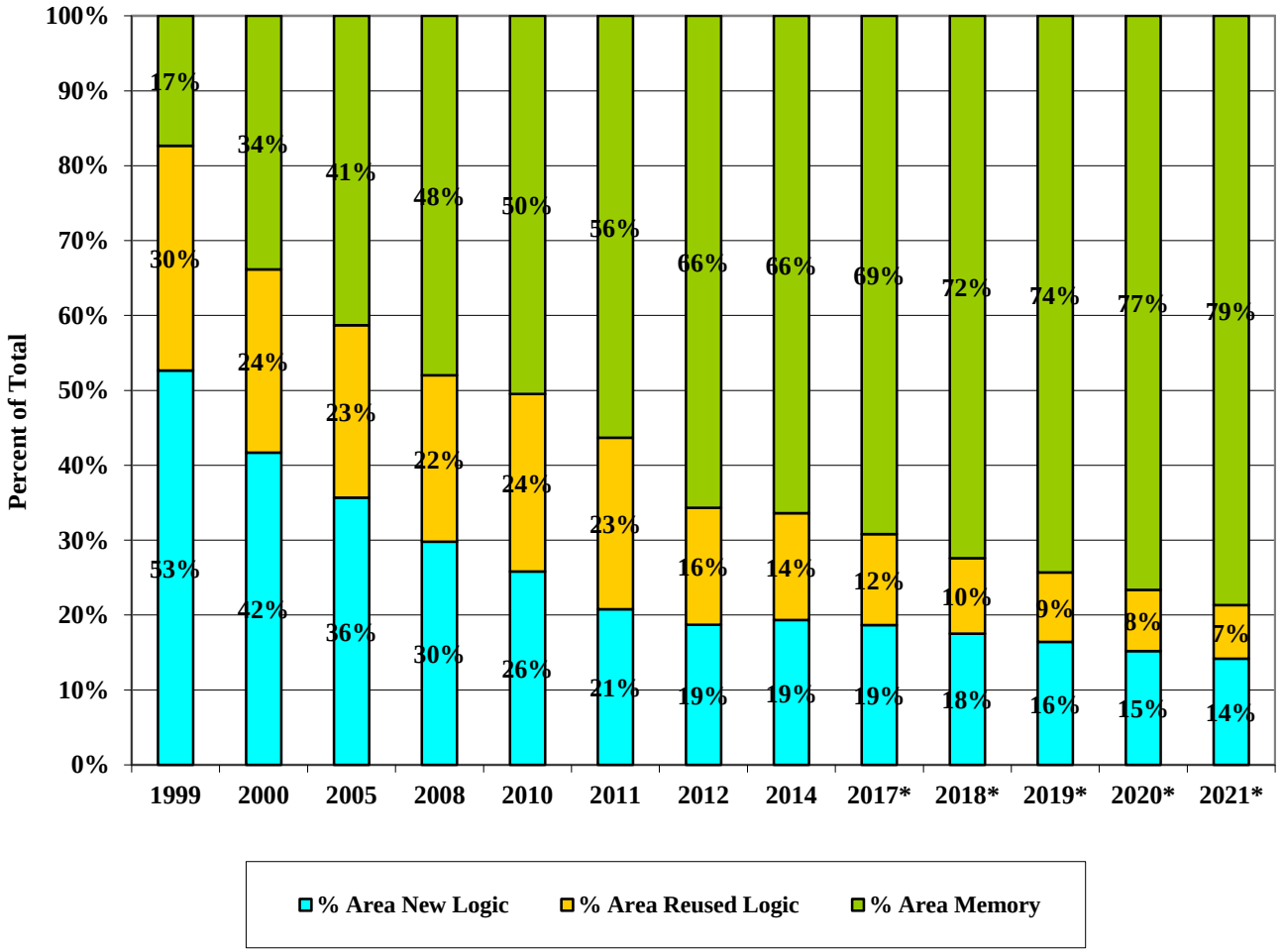
Agenda

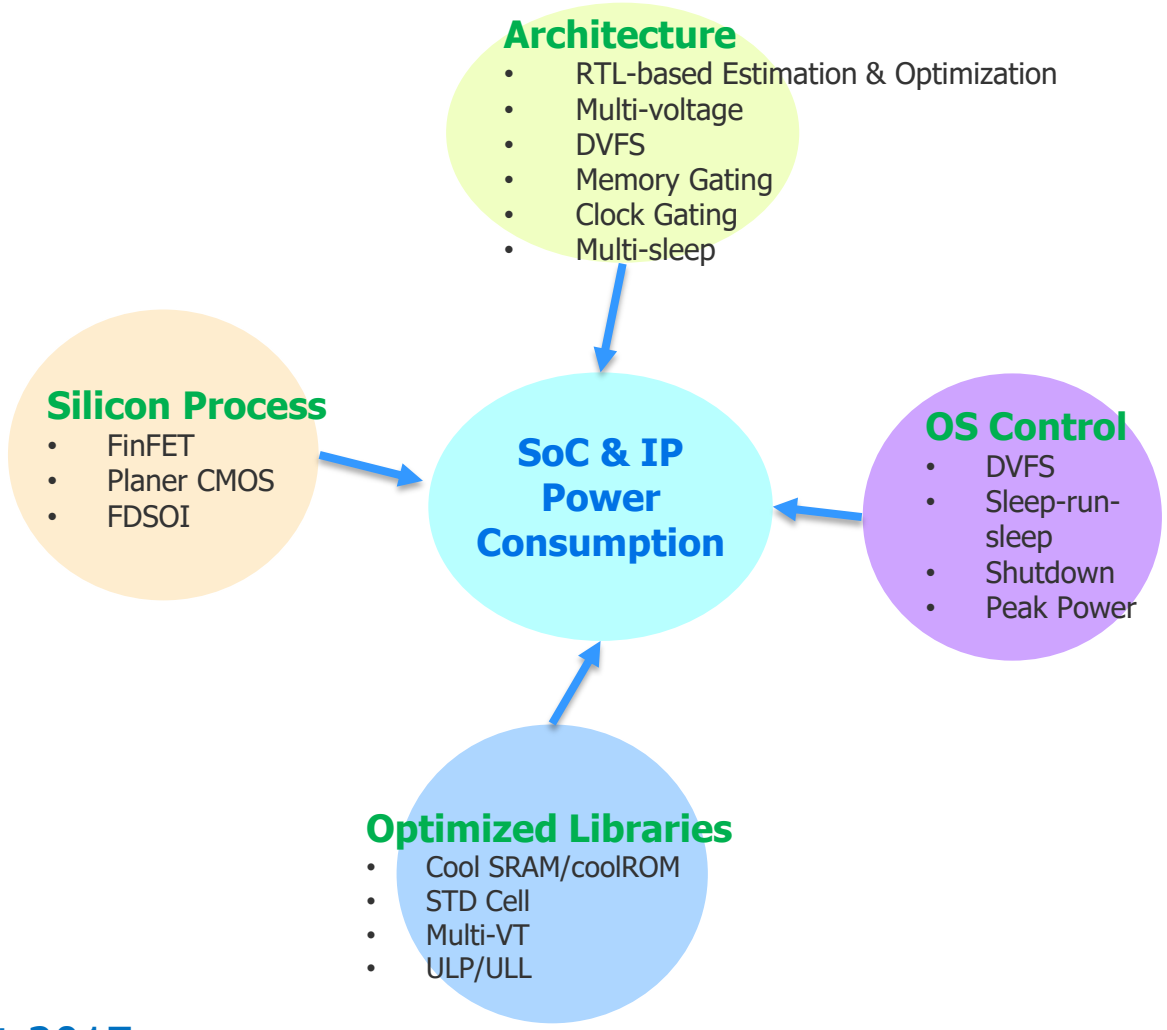
- SoC Market & Drivers
- Top 10 Techniques to Reduce Power & Cost for SoC Designs
  1. Level of Abstraction
  2. Clock Gating
  3. TLS
  4. Deep Sleep
  5. Shutdown
  6. Voltage Impact (Multi-voltage)
  7. Multi-VT & ULP
  8. Dual-Rail & DVFS
  9. MemQuest Configuration Tradeoff
  10. coolSRAM-1T & coolROM Impact for cost Saving
- Differentiated Memory IPs for SoCs to Reduce Power & Cost
- Informative White Papers to Minimize Power & Die Size
  - https://www.mentor.com/products/ip/
- Q & A

Average SoC Die Area Partitioning

Source: SemicoResearch Corp.- SOC Market Analysis & Forecast 2017

SoC Area Trend & Effective Techniques to Minimizing IP & IC Power





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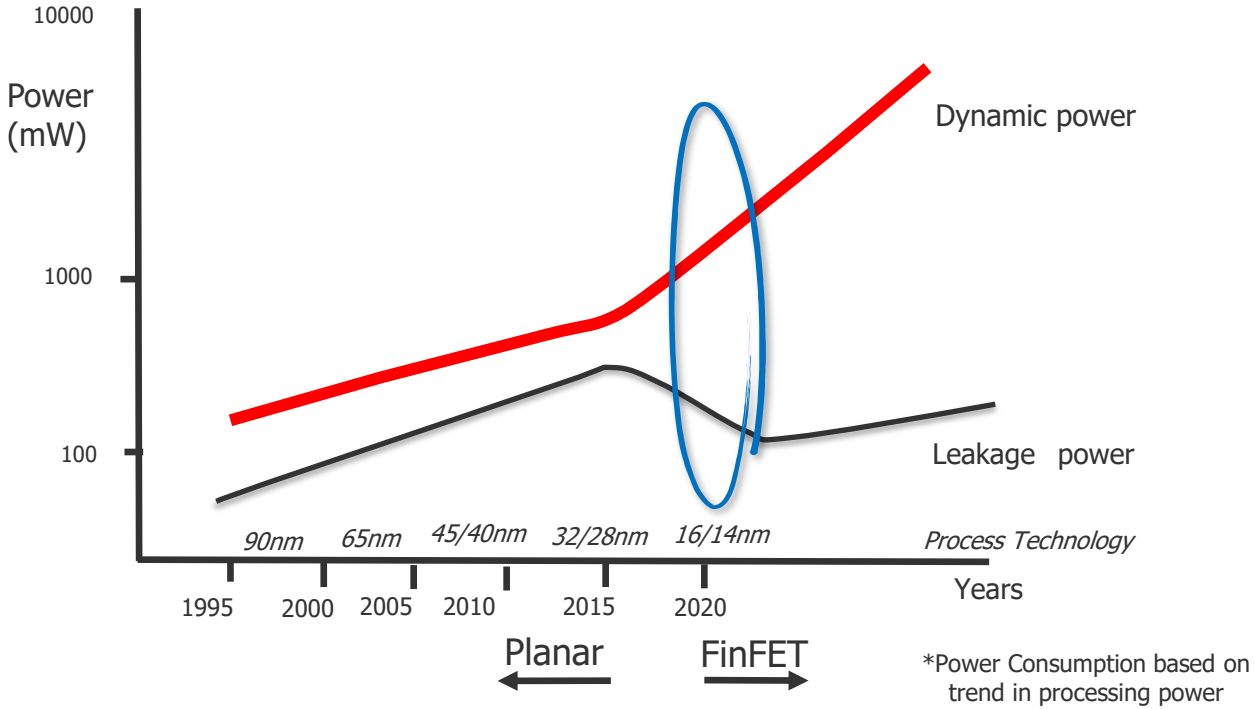
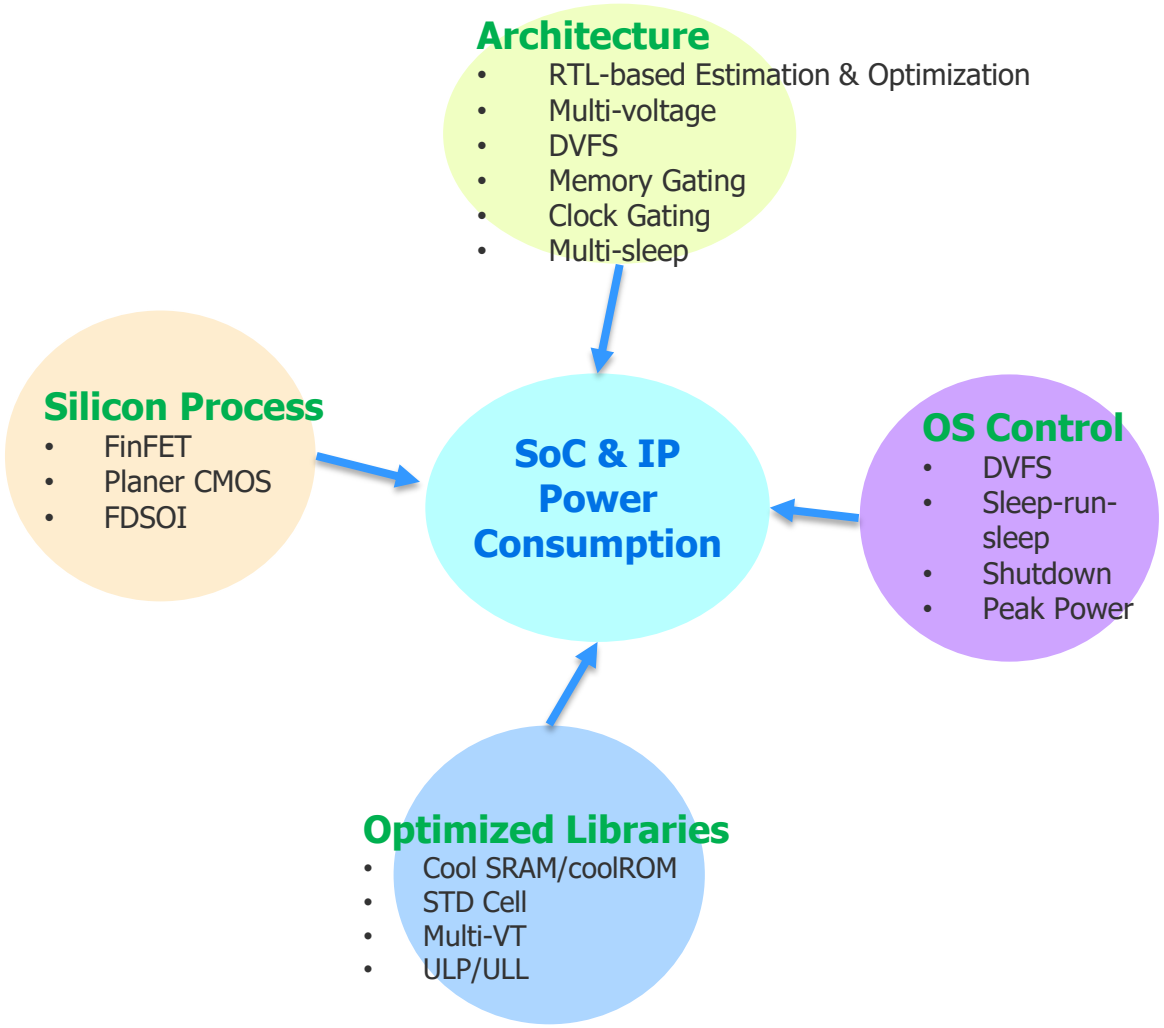
SoC Power Consumption Trend & Techniques to Minimizing IP & IC Power

Total power dissipated by a CMOS device $P = ACV^2f + V\ I\ leak$



*Power Consumption based on trend in processing power requirement and extrapolation of current technology

ITRS SoC-CP Power Consumption Trend*



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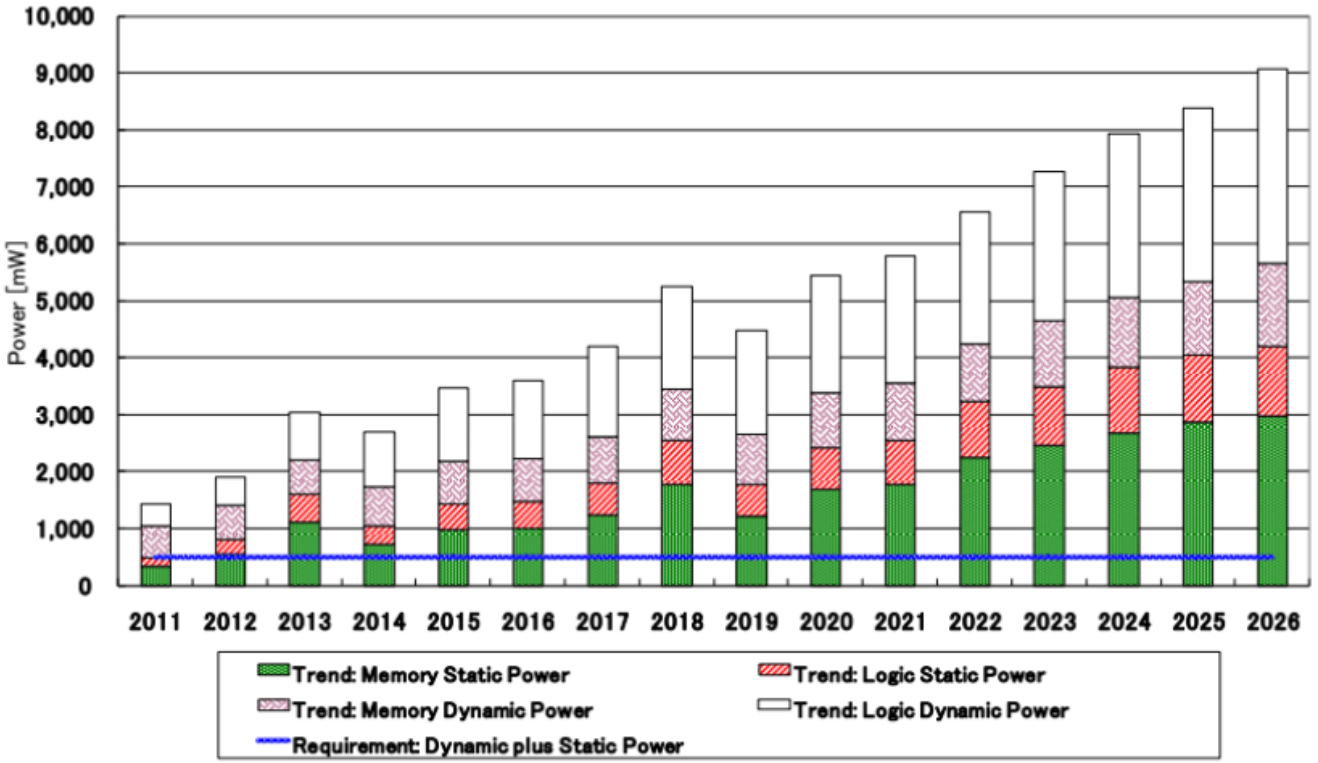
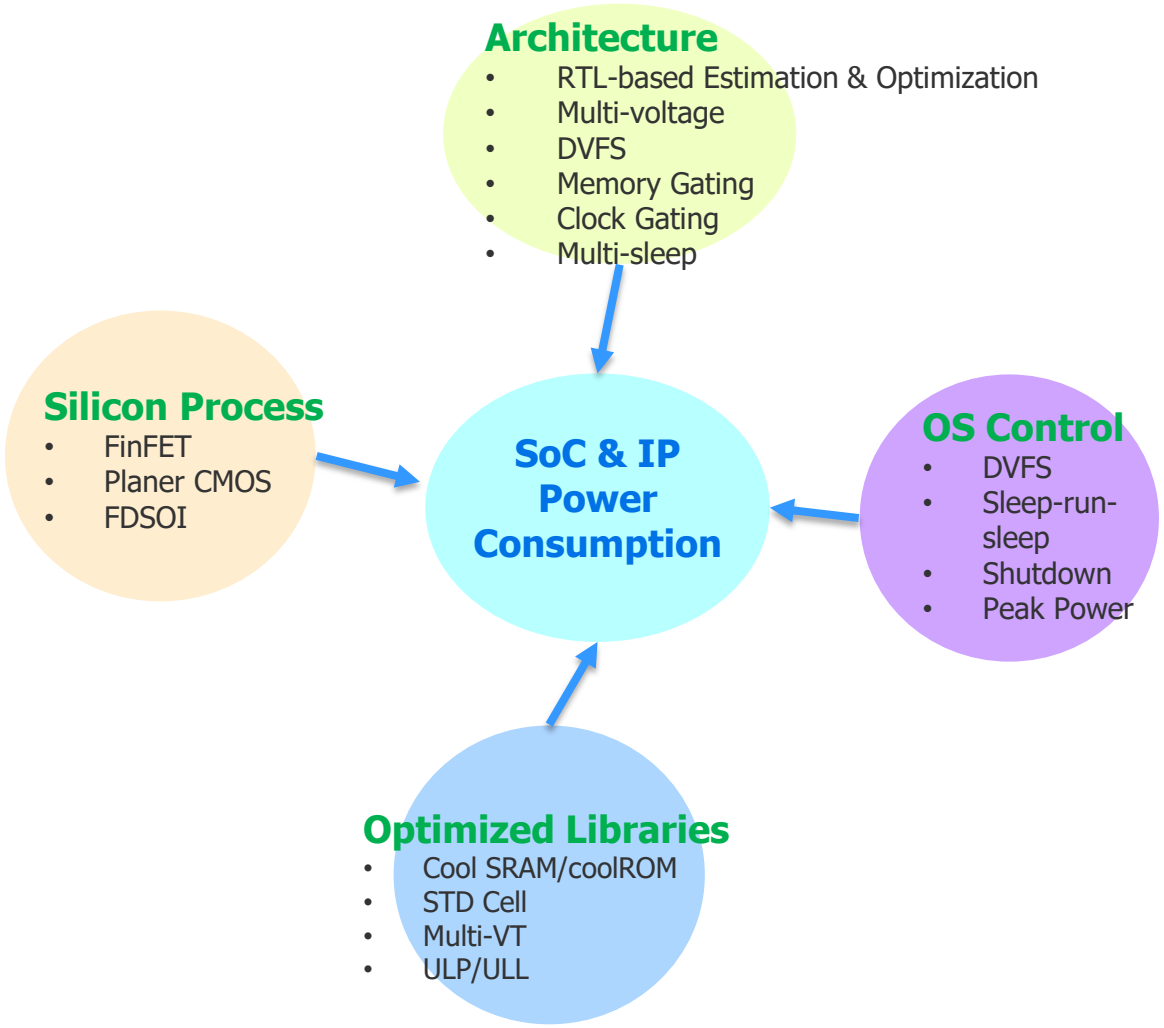
SoC Power Consumption Trend & Techniques to Minimizing IP & IC Power

Total power dissipated by a CMOS device $P = ACV^2f + V\ I\ leak$



ITRS SoC-CP Power Consumption Trend*



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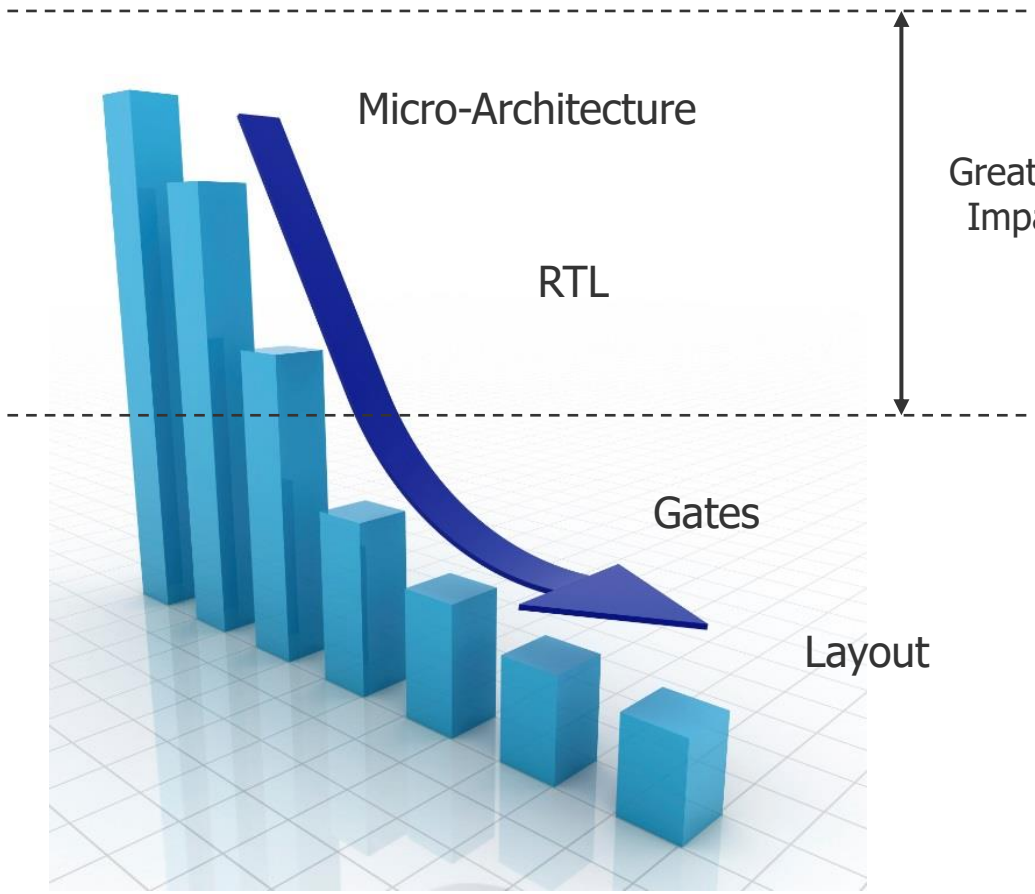
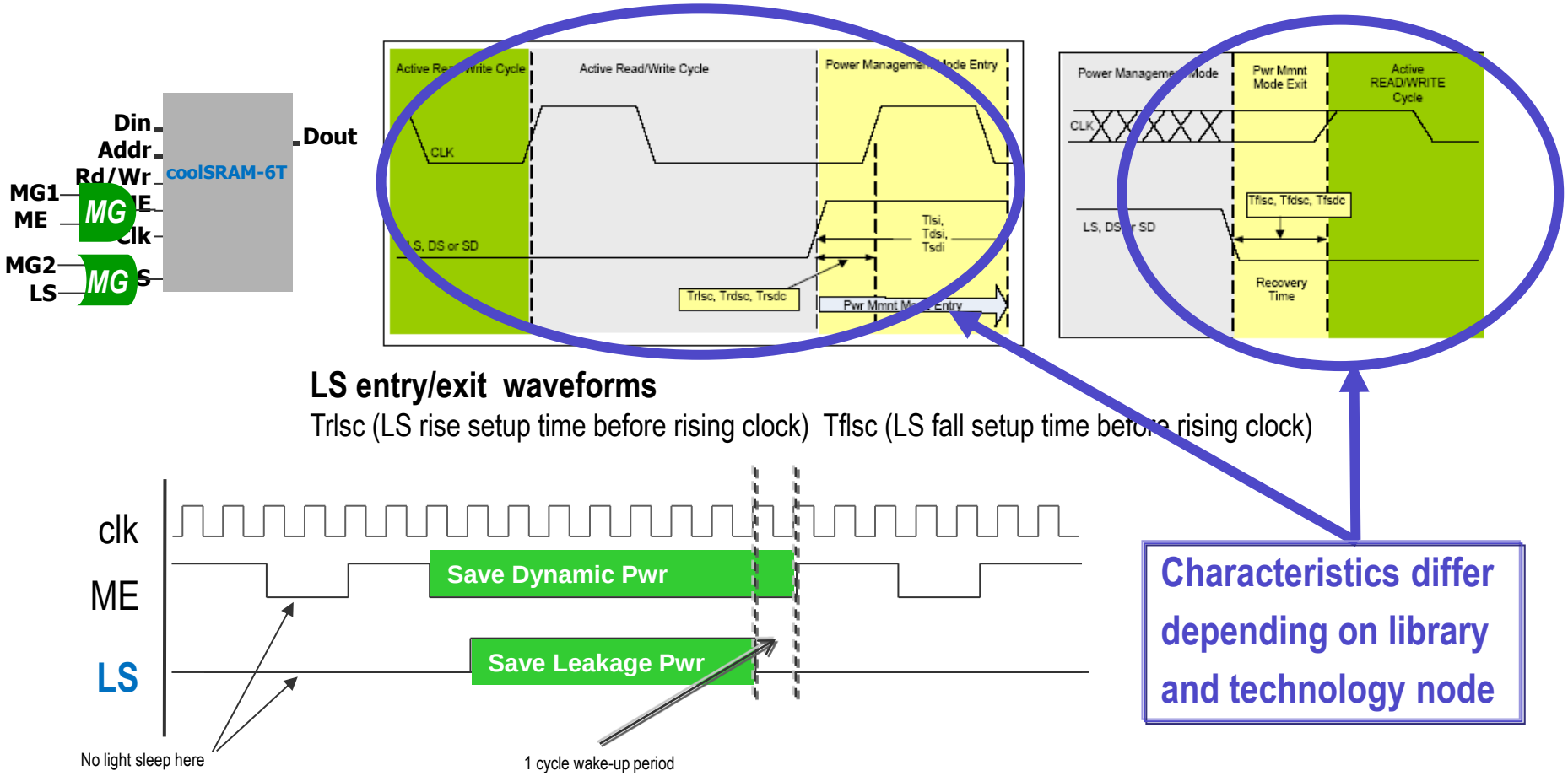
Greatest Impact on Power is at RTL and Above

- **Micro-Architecture**
  - Block level clock gating
  - Shift registers to pointer structures
  - Flop cloning/sharing
  - Memory/register file banking
  - Memory caching
- **RTL**
  - Combinational clock gating
  - Sequential clock gating
  - Memory gating
  - Data gating
- **Physical Implementation**
  - Multi-Vdd, Multi-Vth technology mapping
  - Clock network optimization
  - High-k transistors
  - Novel circuit structures/logic families



Ability to Impact Power

PowerPro® Takes into Account Timing Specs and Power Trade-offs to Reduce the Power of memory intensive SoC

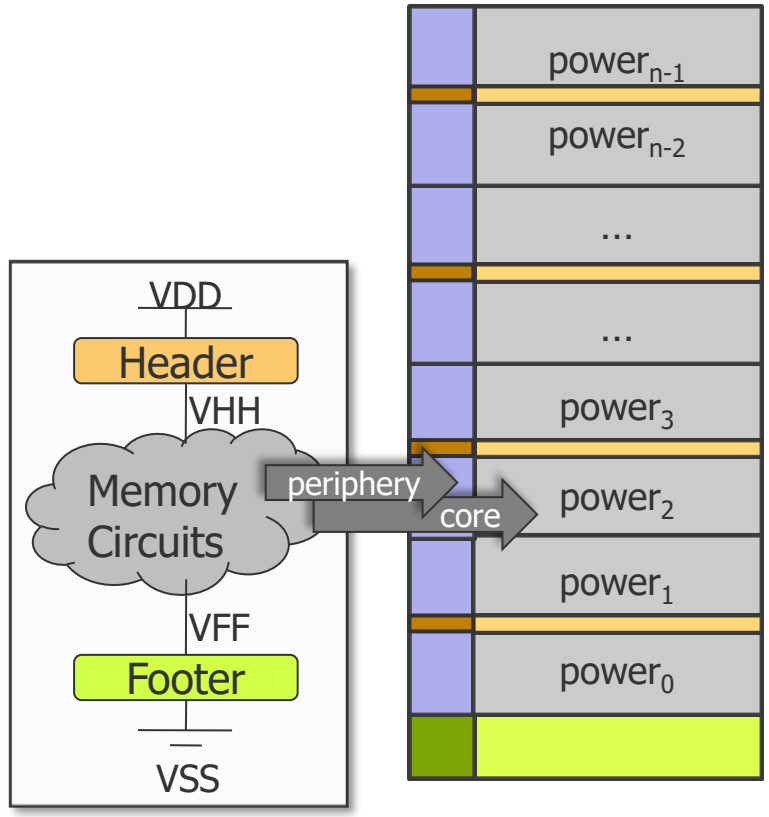


PowerPro Memory Gating insures “Light Sleep” (LS or TLS) signal meets Trlsc and Tflsc requirements

PowerPro, an automation tool for **Estimation** & **Optimization**

coolSRAM-6T
Power Reduction Techniques

- Transparent Light Sleep, full data retention
  - Patented Automatic Transparent Source Biasing Leakage Reduction
  - Leakage Reduction > 50%
  - Zero Latency
- Deep Sleep for Power Gating
  - Periphery shutdown with full data retention
  - Optional isolation cells on input/output pins
  - Leakage reduction > 70%
- Shut Down for Power Gating
  - No data retention
  - Leakage reduction > 95%
  - Output Isolation options (Pull down or floating)
- Multi-VT support in Periphery
  - HVT to reduce leakage
  - LVT to maximize speed
  - SVT to minimize wafer cost
  - MemQuest selectable



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TSMC-28HPCplus Power Reduction Features (coolSRAM-6T)

- 512Kb TSMC-28HPC+ coolSRAM-6T SVT Bitcell

	Leakage Reduction Feature	Active Leakage	Deep Sleep Leakage	Shutdown Leakage
8192x64 **Basic IP Supplier**	None	1	N/A	N/A
8192x64 **Mentor coolSRAM-6T**	**TLS, Deep Sleep, Shutdown**	**0.52**	**0.34**	**0.07**

TSMC-28HPCplus Benchmark Comparison (coolSRAM-6T)

- 540Kb coolSRAM-6T SVT Bitcell SVT Periphery Comparison

	Area	WC Leakage	Typ Leakage	Customer Use-case WC Total Power	Customer Use-case Typ Total Power
Mentor / Competitor	95%	22%	25%	33%	80%
Mentor / Foundry Provided	**98%**	**20%**	**25%**	**25%**	**25%**

- 540Kb coolSRAM-6T ULL Bitcell HVT/UHVT Periphery Comparison

	Area	Speed	Typ Leakage	Typ Dynamic Power	Customer Use-case Typ Total Power
Mentor / Competitor	~Same	**150%**	**85%**	**65%**	**60%**

ULP and uLL Technology for Power Reduction

- Memory IP Offering in TSMC ULP and uLLTechnologies
  - 40ULP: nominal voltage 0.9v, write-assist required
  - 55ULP: nominal voltage 0.9v, write-assist required for UHD bitcell
  - 28HPC+ uLL: nominal voltage 0.9v, write-assist required,
- ULP/uLL vs. LP
  - Lower voltage / power / leakage
  - Slower speed
- Multi-vt Periphery Further Reduces Leakage
  - 40ULP and 55ULP: hvt, uhvt
  - 28nm HPC+: hvt, uhvt
- Custom Features
  - Dual rail for additional dynamic power reduction
  - coolROM with Novelics bitcell runs at ultra-low voltage
  - Forward body-bias in slow corners for performance enhancement

TSMC-55ULP vs TSMC-55LP Benchmark Comparison (coolSRAM-6T)

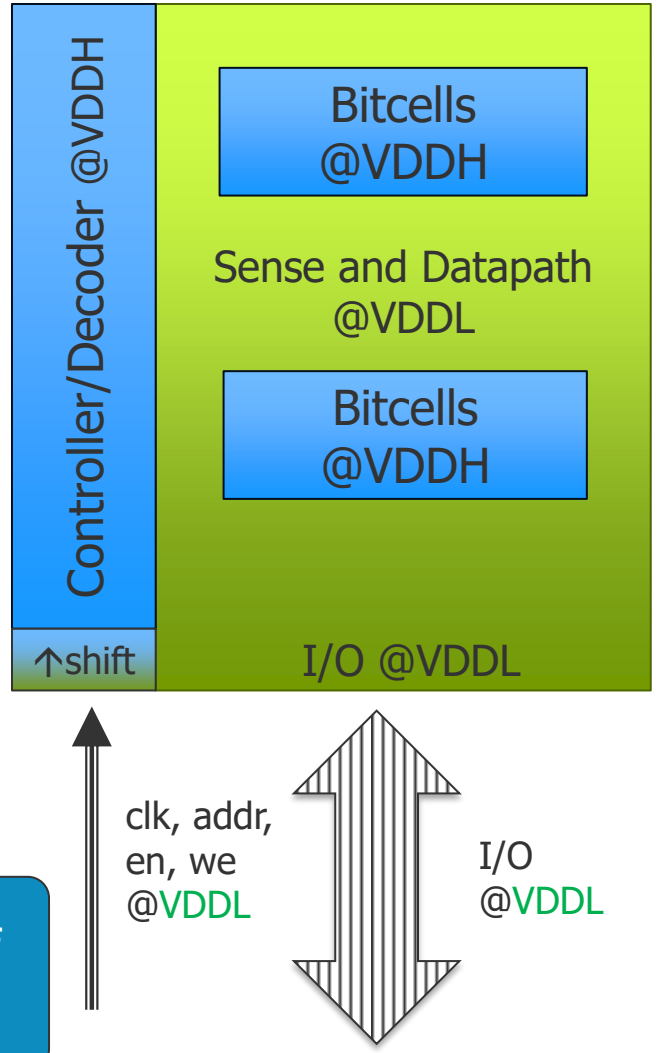
- 5120 x 32 coolSRAM-6T Instance With TLS, Deep Sleep, and Shutdown

Vendor	INSTANCE	Area	Access Time	Max Frequency	Active Power	Active Leakage	Deep Sleep Leakage
		(mm^2)	(ns)	(MHz)	(uW/MHz)	(mA)	(mA)
	coolSRAM-6T	(pre-shrink)	WC	WC	TC	BC	BC
TSMC-55LP	5120x32						
TSMC-55ULP	5120x32						
Comparison = 55ULP / 55LP		**Same**	**221%**	**38%**	**56%**	**40%**	**29%**

- PVT Conditions:
  - TSMC-55LP: WC = SS 1.08V 125C; TC = TT 1.20V 25C; BC = FF 1.32V 125C
  - TSMC-55ULP: WC = SS 0.81V -40C; TC = TT 0.90V 25C; BC = FF 0.99V 125C
- Comparison Results
  - 55LP is 2.6x faster
  - 55ULP dynamic power is 44% less
  - 55ULP active leakage is 60% less
  - 55ULP retention leakage is 71% less
    - 55LP Vnom = 1.2V; 55ULP Vnom = 0.9V

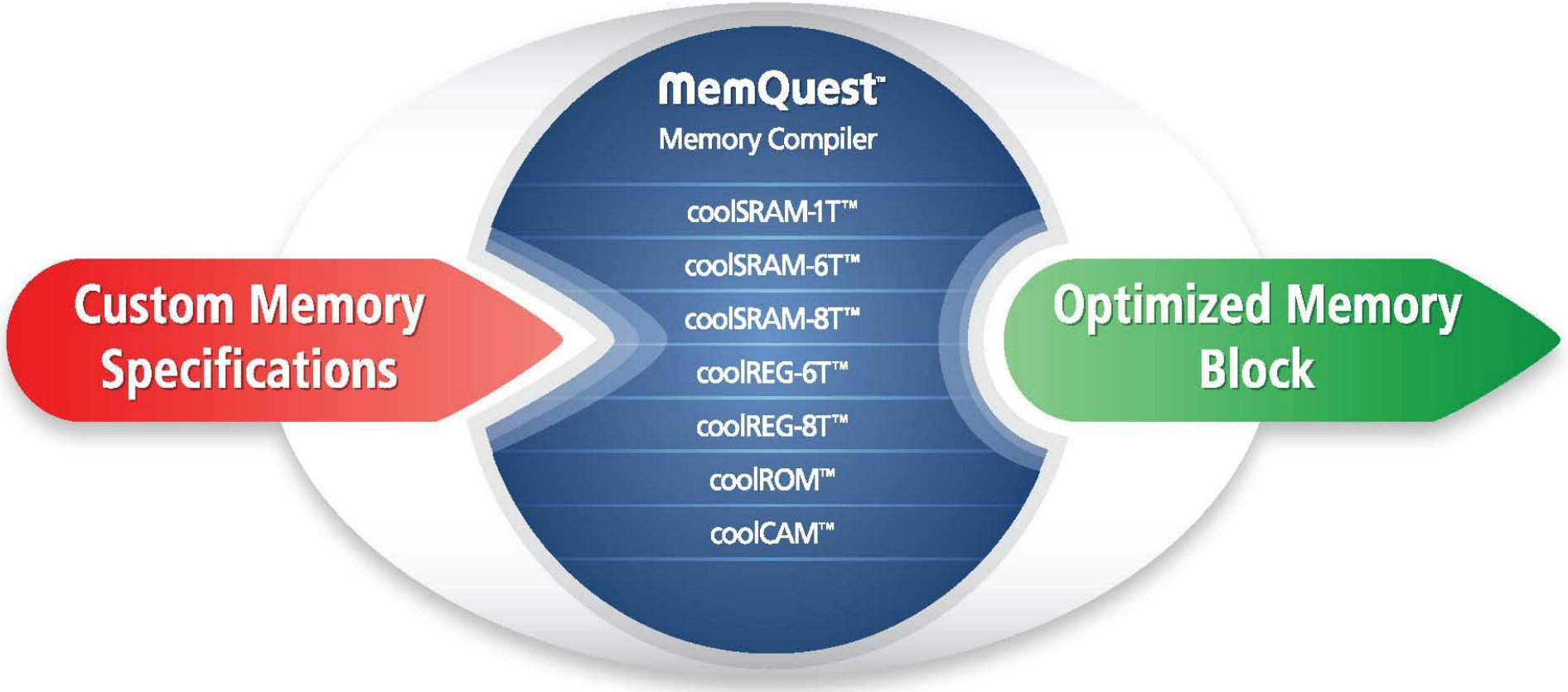
coolSRAM-6T / Dual Rail Supply for Power Minimization

- Power is provided on two rails
  - Normal supply voltage VDDH down to VDD-10% for the bitcell and memory controller circuits
  - Low supply voltage VDDL down to VDD-35% for the memory datapath
- Huge savings for Dynamic Power
  - Dynamic power dissipation is split 1/3 to VDDH and 2/3 to VDDL
- Big savings for Leakage Power
  - Fully compatible with Automatic LPM, Sleep with data retention and full shut down.
- Minimal area impact
- Can still operate at high speed



Comparing of DR to SR, Dual Rail saves 20% of dynamic power and 15% of static power. As a trade-off, it is 3% bigger and 47% slower than Single Rail

MemQuest™: Web-based Memory Compiler



Full nodes: 180nm, 130nm, 90nm, 65nm, 45nm

Half nodes: 160nm, 152nm, 110nm, 55nm, 40nm, 28nm HPM/HPC+

Roadmap –16/12 nm, 10/7 nm FF+

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MemQuest / Instance Specification Page

novelics MemQuest™

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Logout (zchen)
memquest.ies.mentorg.com

Project:	ulp_uLL / TSMC-28HPC+	
Type:	coolSRAM-6T	
Version:	2013.R1-rc3b	
Name:	NVIC _SRM6T_8192x64	
Depth:	8192	Number of entries or words in the memory (e.g., a 512Kbit memory organized as 8Kx64 has 8192 entries)
Width:	64	Number of parallel data I/O lines (e.g., a 512Kbit memory organized as 8Kx64 has 64 data I/O lines)
Size:	512 Kbits	
Subword Capability:	Byte	***Bit*** or ***Byte***: Add Bit/Byte writable subword capability.
Bitcell options:	ULL	***SVT*** is Default, ***ULL*** is slower with lower leakage.
VT options:	UHVT	***SVT*** is Default, ***HVT*** is slower with lower leakage, ***UHVT*** is slowest with lowest leakage.
Leakage Power Management:	Shutdown	Leakage Power Management (LPM) reduces overall leakage. Transparent Light Sleep (***TLS***) will reduce leakage, and does not require customer control. ***TLS*** can be applied separately to the Periphery and Core. ***Deep Sleep*** will disable power to all peripheral circuits while maintaining data retention. ***Shutdown*** will disable power to all circuits and lose data retention. ***Shutdown*** comes with ***TLS***. ***Shutdown*** comes with ***Deep Sleep***.
Redundancy:	Tessent-Column	Select a redundancy option for yield enhancement. ***Tessent-Column*** is compatible with Tessent flow.

Submit Cancel

MemQuest for TSMC Customers

Shorten Design Cycle for Architectural Analysis & in sync with TSMC Silicon

Sort by Dynamic Power

Selection	Area (mm^2)	X (mm)	Y (mm)	Max Frequency (MHz)	Access Time (ns)	Dynamic Power (µW/MHz)	Active Leakage (mA)
Operating Conditions (PVT):				wc *	wc *	tc	tc
1	**0.494**	1.19	**0.415**	262	2.05	65.7	**0.0538**
3	0.531	1.19	0.446	295	1.79	57.2	0.055
2	0.502	0.634	0.792	278	2.07	43	0.0604
9	0.614	1.19	0.515	303	1.74	56.8	0.0608
4	0.542	0.634	0.855	**312**	1.82	39.4	0.0619
12	0.642	1.19	0.540	307	**1.69**	57	0.062
15	0.726	1.19	0.610	296	1.82	59.3	0.0644
6	0.563	0.634	0.888	296	1.95	41.3	0.0664
17	0.810	1.19	0.681	292	1.86	62.5	0.0668
11	0.630	0.634	0.994	297	1.98	40.6	0.0686
13	0.661	0.634	1.04	297	2	41.9	0.07
18	0.840	1.19	0.706	291	1.87	62	0.0748
5	0.553	**0.358**	1.55	255	2.17	31.3	0.0751
8	0.599	0.358	1.67	252	2.32	**30.6**	0.0769

Selection	Area (mm^2)	X (mm)	Y (mm)	Max Frequency (MHz)	Access Time (ns)	Dynamic Power (µW/MHz)	Active Leakage (mA)
Operating Conditions (PVT):				wc *	wc *	tc	tc
8	0.599	0.358	1.67	252	2.32	**30.6**	0.0769
10	0.622	0.358	1.74	243	2.44	31.3	0.0826
5	0.553	**0.358**	1.55	255	2.17	31.3	0.0751
14	0.723	0.358	2.02	236	2.63	33.1	0.0963
7	0.584	0.358	1.63	232	2.44	34.5	0.0812
4	0.542	0.634	0.855	**312**	1.82	39.4	0.0619
11	0.630	0.634	0.994	297	1.98	40.6	0.0686
6	0.563	0.634	0.888	296	1.95	41.3	0.0664
13	0.661	0.634	1.04	297	2	41.9	0.07
16	0.731	0.634	1.15	292	2.07	42.5	0.0798
2	0.502	0.634	0.792	278	2.07	43	0.0604
9	0.614	1.19	0.515	303	1.74	56.8	0.0608
12	0.642	1.19	0.540	307	**1.69**	57	0.062
3	0.531	1.19	0.446	295	1.79	57.2	0.055
15	0.726	1.19	0.610	296	1.82	59.3	0.0644
18	0.840	1.19	0.706	291	1.87	62	0.0748

Sort by Leakage Current

MemQuest / Architectural Analysis

Selection	Area (mm^2)	X (mm)	Y (mm)	Max Frequency (MHz)	Access Time (ns)	Dynamic Power (µW/MHz)	Active Leakage (mA)	Sleep Leakage (mA)
Operating Conditions (PVT):				wc *	wc *	tc	tc	tc
1 ◉	**0.369**	0.634	0.582	247	2.46	47.4	0.0393	**0.0029**
2 ○	0.397	1.19	**0.334**	275	2.03	62.5	**0.0379**	0.0038
3 ○	0.398	0.634	0.627	292	2	39.5	0.0412	0.0037
4 ○	0.402	0.358	1.12	250	2.52	39.5	0.0468	0.0037
5 ○	0.435	0.358	1.22	293	2.06	**36.3**	0.0493	0.0048
6 ○	0.451	1.19	0.379	300	1.8	56.5	0.0403	0.0051
7 ○	0.456	0.634	0.719	**316**	1.78	37.6	0.0441	0.0053
8 ○	0.485	**0.219**	2.21	226	2.78	44.8	0.0625	0.0058
9 ○	0.500	0.358	1.40	286	2.17	37.4	0.0534	0.0071
10 ○	0.525	0.219	2.39	226	2.96	44.6	0.0662	0.0077
11 ○	0.552	1.19	0.463	309	**1.7**	57.1	0.0446	0.0077
12 ○	0.563	0.634	0.887	301	1.92	40.9	0.0496	0.0086
13 ○	0.770	1.19	0.647	292	1.89	64.6	0.0529	0.0128

MemQuest, for Greatest Architectural Freedom

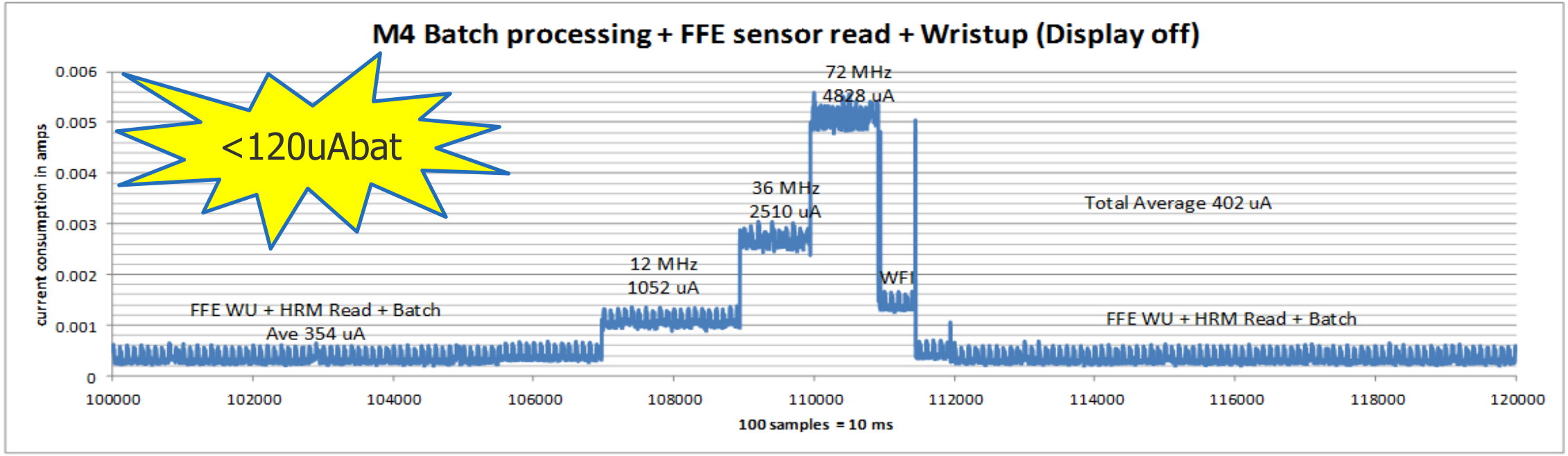
Field-Of-Use For Memory IPs

Foundry			Novelics ported Fabs			
Process			180nm – 28nm (Varies by Technology & process Nodes)			
Options	Description	coolSRAM-6T (SP), Optimized for large instances	coolREG-6T (SP), Optimized for small instances	coolREG-8T (2P & DP), Optimized for small instances	coolROM	coolSRAM-1T
		Range	Range	Range	Range	Range
WORD_DEPTH		64 - 64K	16 - 2K	4 – 1K	128 - 64K	2K – 64K
WORD_WIDTH		2 - 288	2 - 144	1 - 144	4 – 256	8-512
MUX		2, 4, 8, 16, 32	2, 4, 8	1, 2, 4	4, 8, 16, 32, 64	8, 16, 32
Banking	number of blocks	1-8	1	1	1-8	1-8
Bit/byte write	select bit/byte write	0, 1, 8	0, 1, 8	0, 1, 8		0, 1, 8
maximum bits per instance		1M bit	72K bit	36K bit	1M bit 1/2 M bit for 28 nm HPC+	4M bit 180nm to 55nm

Wearable use case – power profile

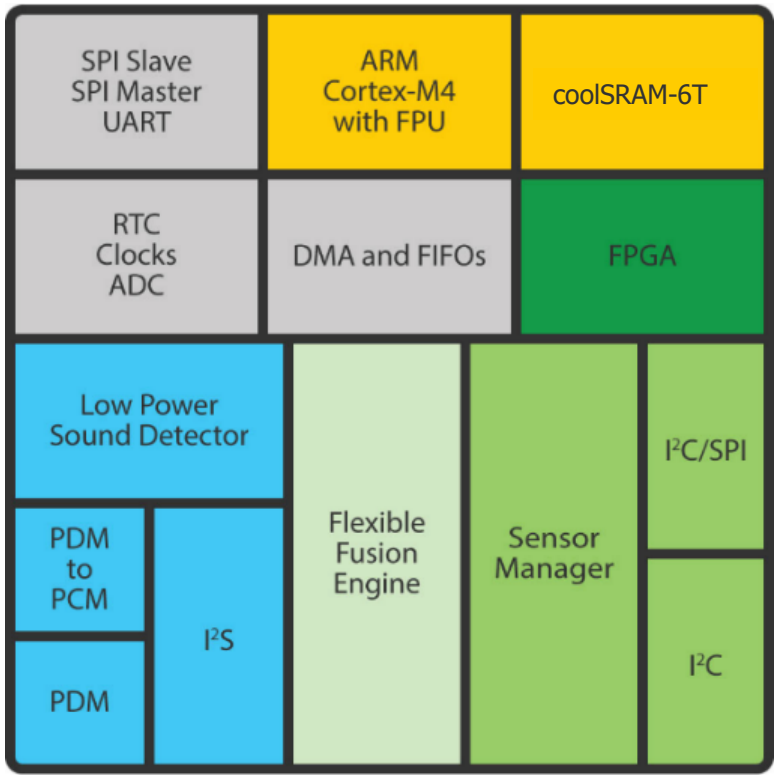
- Battery: 150mAh
- Lifetime: 1 week
- System current: 892µA at battery

- Budget for always-on: 20% ➔178uA$_{bat}$
- Budget for device: 526µW (subtract regulators)



Total Average : 402 uA

Sensor Architecture

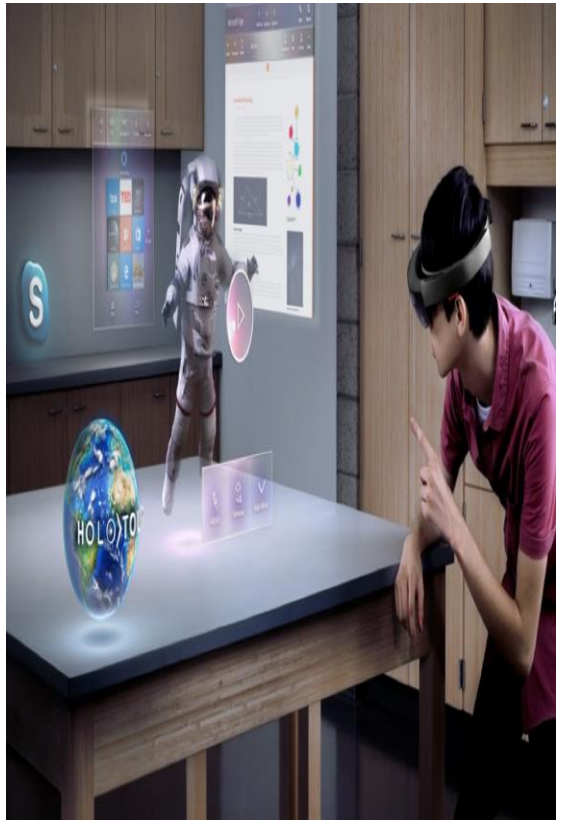


- Multi core processing
  - Dedicated audio processing @50 uA
  - Dedicated sensor compute @35 uA/MHz
  - General purpose ARM CPU @75 uA/MHz
- coolSRAM-6T*
  - 512k (128k Always On) GF 40nm-LP @7 uW/Mhz
  - 2.28 uA leakage current (8k block)

*Mentor coolSRAM-6T offered Lowest leakage & active current which allows ultra low power Always-On processing of audio/sensor data

High volume SOC: Image Sensor design with coolSRAM-6T @ DAC 2017

Ultra Low Power Memory/ High Density IPs for AI Applications



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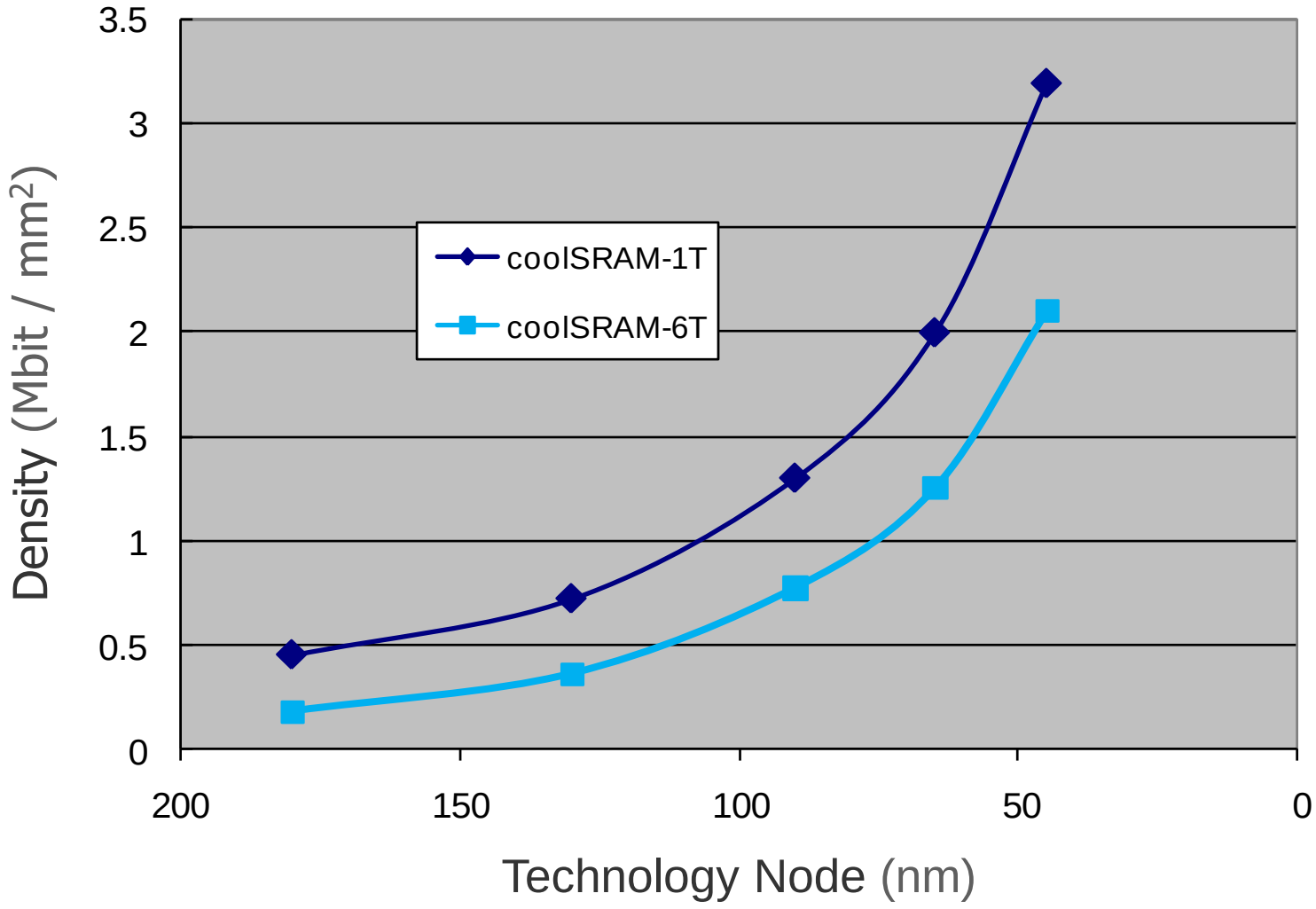
Mentor Memory IPs with ultra low leakage & enables customers audio processing with better performance & die size reduction and minimized power consumption

Mentor Memory IPs with lowest dynamic power for DSP processing in audio application

coolSRAM-1T / Advantages

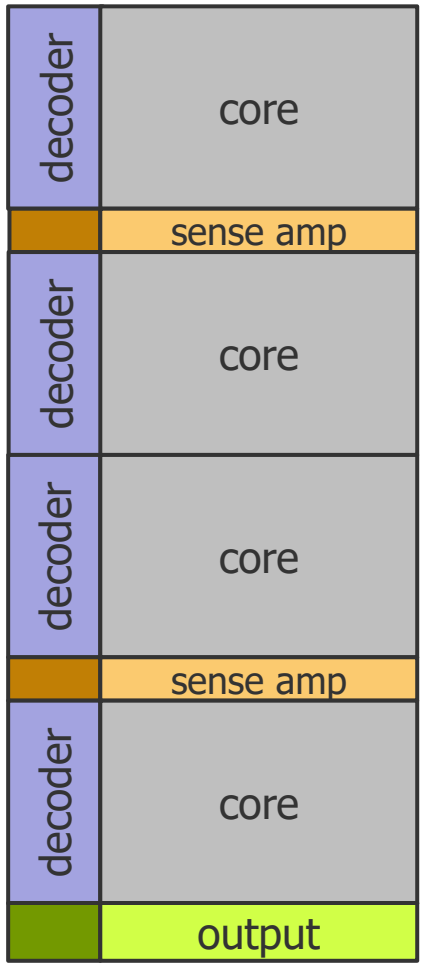
- ✓ **High Density**
  - — Compiled to your exact specification
  - — Save up to 25%-50% area compared to SRAM-6T
- ✓ **100% Standard CMOS Process**
  - — No special layer
  - — No extra mask
- ✓ **Low Leakage**
  - — Single transistor bitcell (vs 6 transistor for SRAM-6T)
  - — IO transistor bitcell (vs core device for SRAM-6T)
  - — Large percentage of periphery is also IO device
- ✓ **Silicon Proven**
  - — Silicon success in 180nm-65nm
  - — Across multiple foundries

coolSRAM-1T / Memory Density Scaling



coolROM / Architecture

- Novelics Proprietary NAND bitcell
- Up to **2Mbit** per Macro
  - Logical: Max 128K entries, 256 wide bus
  - Physical: Max 2K rows, 1024 columns
- Multiple Banks
  - MemQuest selectable up to 8 banks
  - Smaller bank size → Higher speed
  - Active power dissipation localized to the active bank



28HPCplus Benchmark Comparison (coolROM)

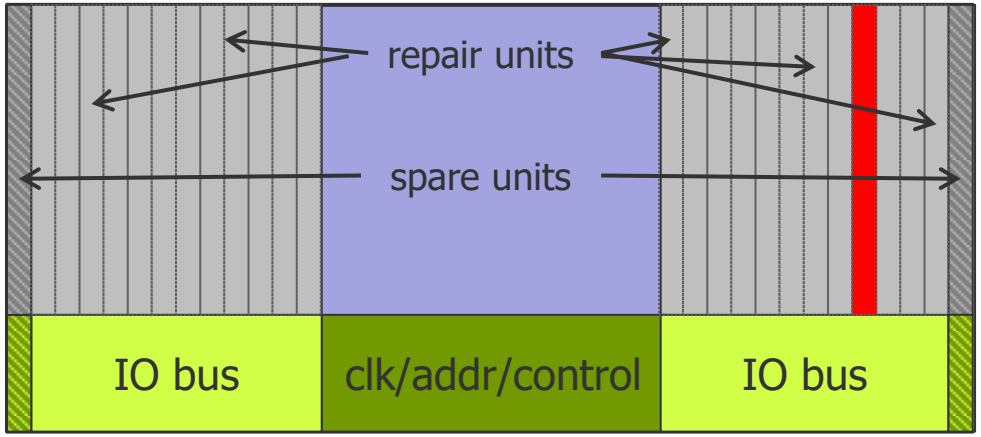
Vendor	Configurations				
	3328 x 9	5120 x 24	4096 x 4	8192 x 32	7680 x 8
Foundry Area (um^2)					
Mentor Area (um^2)					
Mentor Area Saving	53%	60%	46%	61%	59%

- Novelics IP Advantage:
  - **Up to 61% area saving**

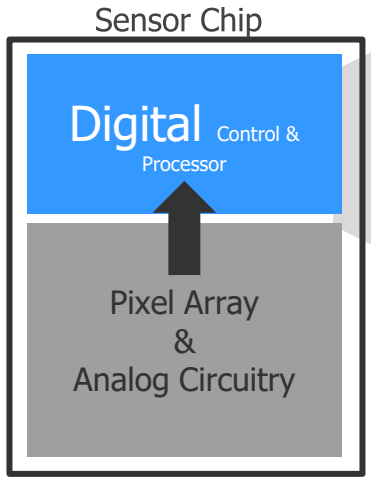
coolSRAM / Column Redundancy

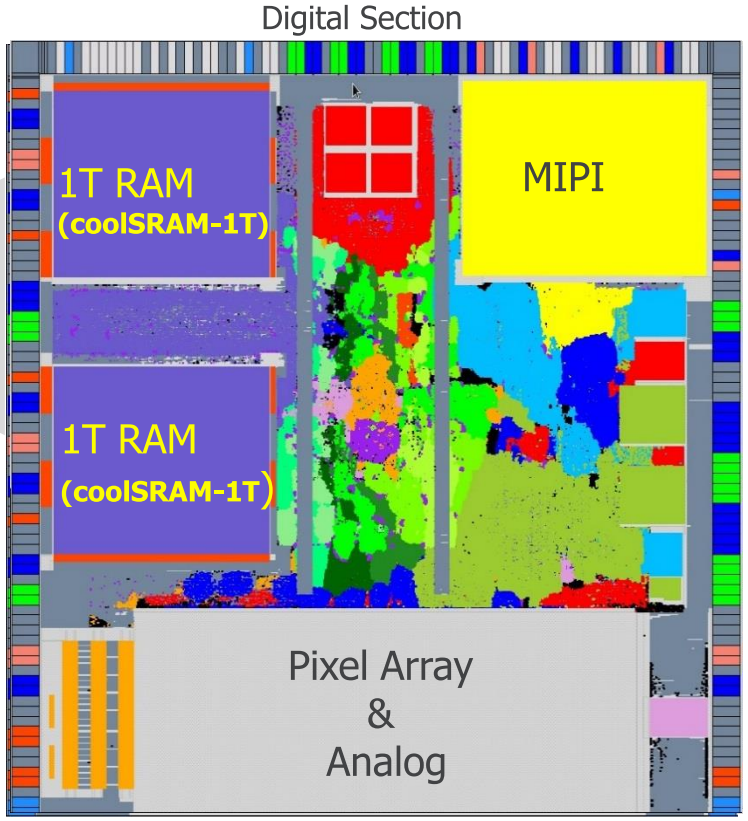
Yield Enhancement for Cost Saving

- One spare unit per butterfly wing
- Consider when aggregate memory is > 2Mbits
  - For macros > ¼ MBit
- Small area overhead, negligible performance overhead
- Fully compatible with Tessent for automation of BIST/BISR



High volume SOC: Image/Depth Sensor design with coolSRAM-1T @ DAC 2016

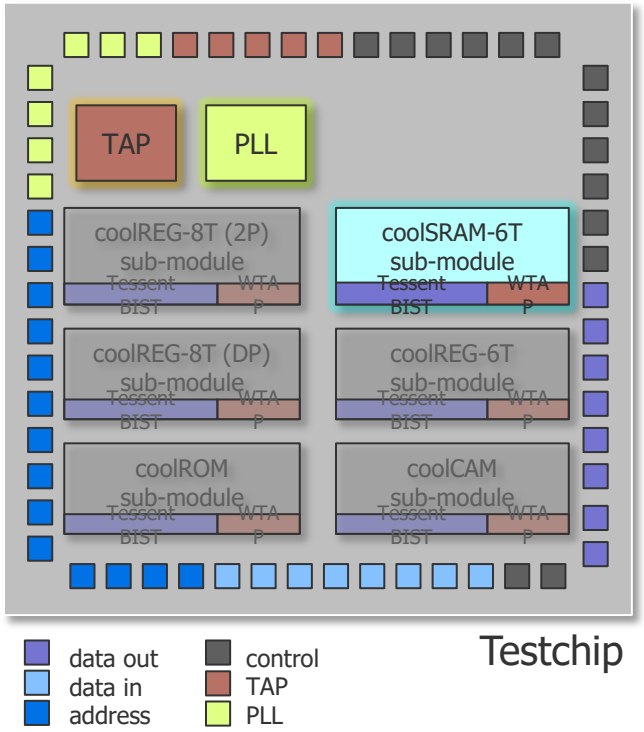




Higher Density IPs & Cost Saving

IP Type Used	Memory in Chip	IP Area Saving	Die Cost	Cost Saving	Average ICs/Month	Months of Life	Cost Saving
coolSRAM-6T, coolREG-6T/8T, coolROM	40%	25%	$4.00	$0.40	500,000	18	**$3,600,000**
coolSRAM-1T	50%	50%	$4.00	$1.00	500,000	18	**$9,000,000**

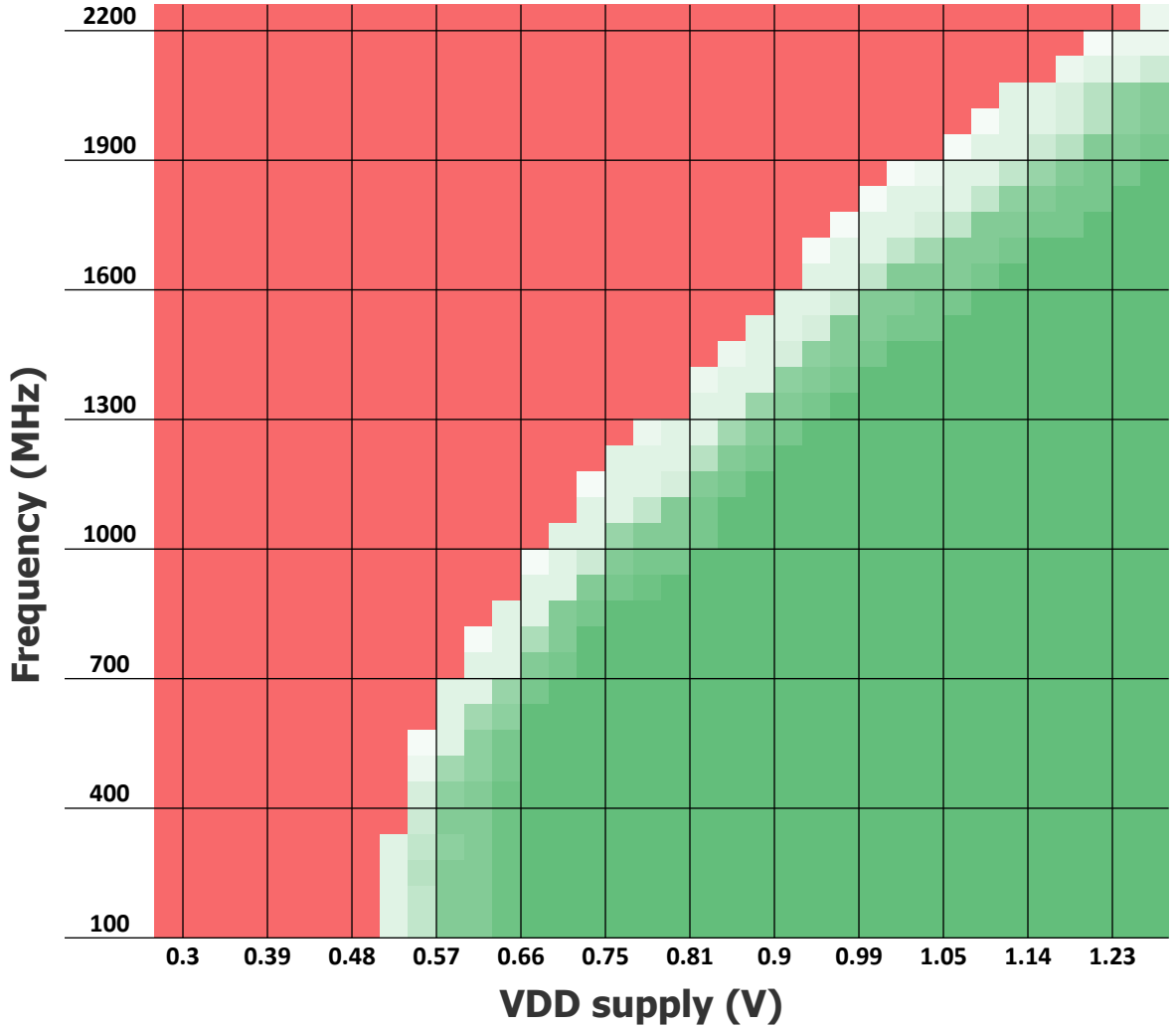
28nm HPC+ Test Chip



Testchip

- Testchip for 6 Novelics IP
  - **coolSRAM-6T**
  - **coolREG-6T**
  - **coolREG-8T (DP)**
  - **coolREG-8T (2P)**
  - **coolROM**
  - **coolCAM**
- 5 corner lots
  - TT, SS, FF, SF, FS
  - Lower voltage introduces higher level of Variability
  - Leakage controled, -40 D C to 125 D C
  - Mentor Tessent MBIST
  - PLL for at-speed
    - True Circuits, Inc.
- Direct access to memory pins for setup/hold testing

coolSRAM-6T 28nm HPC+ Shmoo MED 8192x16 (125C)



- 15 parts tested
- 3 parts per corner :
  - TT
  - SS
  - FF
  - FS
  - SF

15 parts pass
12 parts pass
9 parts pass
6 parts pass
3 parts pass
0 part pass

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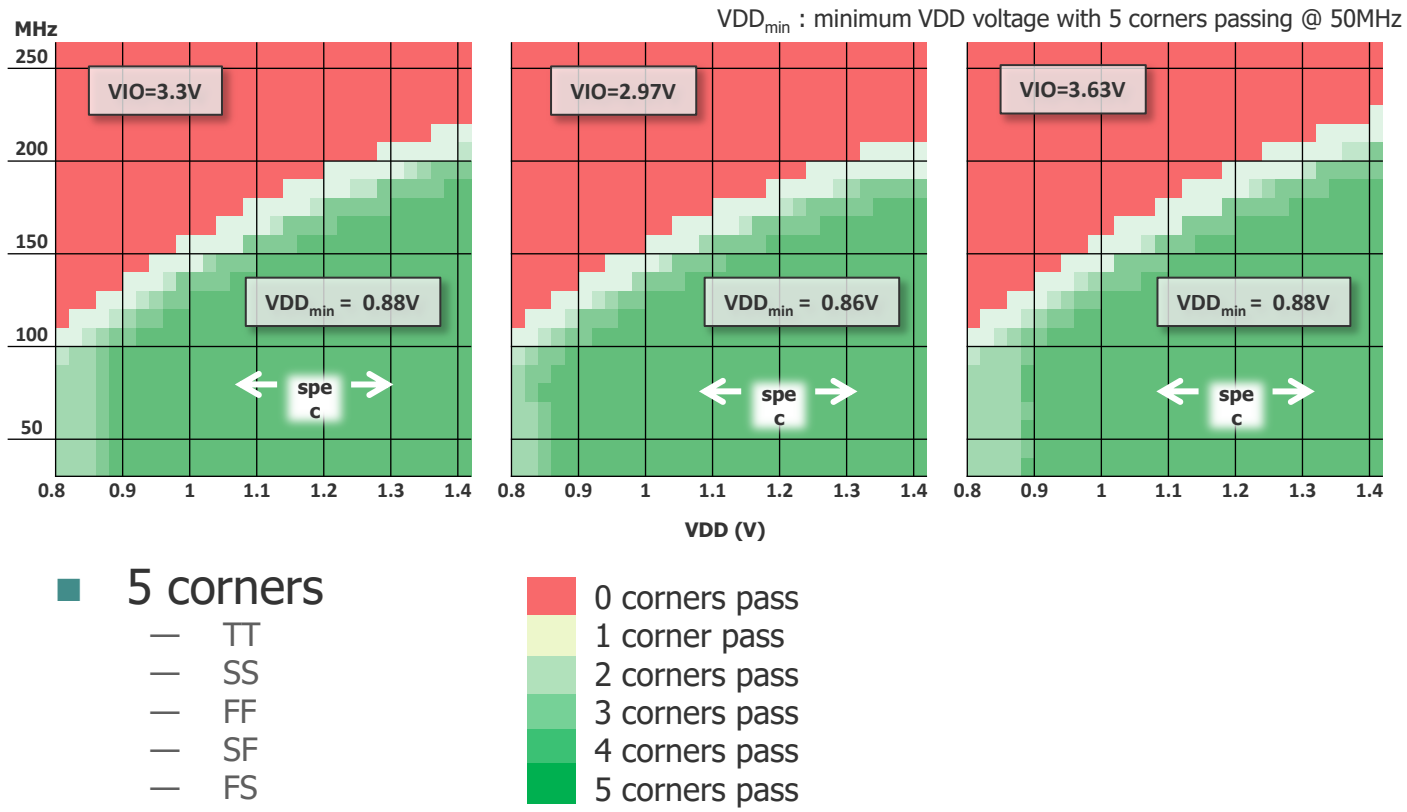
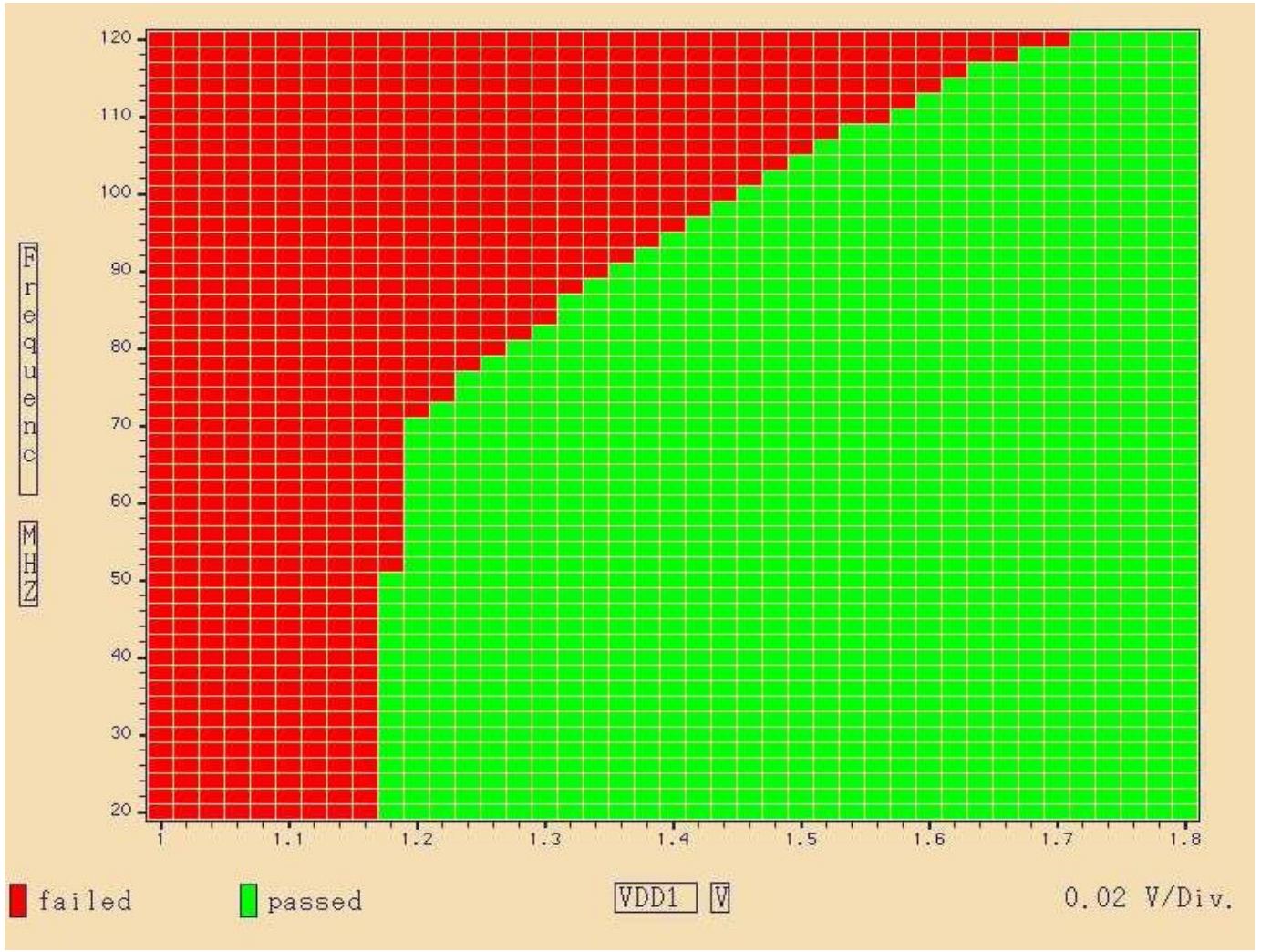
coolSRAM-1T "VDD vs Clk Freq" Shmoo (upto 120 Mhz in spec Voltage)
WIDE 512x256 @ 125C (SMIC 110nm)
Standard CMOS Process, No special layer, No extra mask



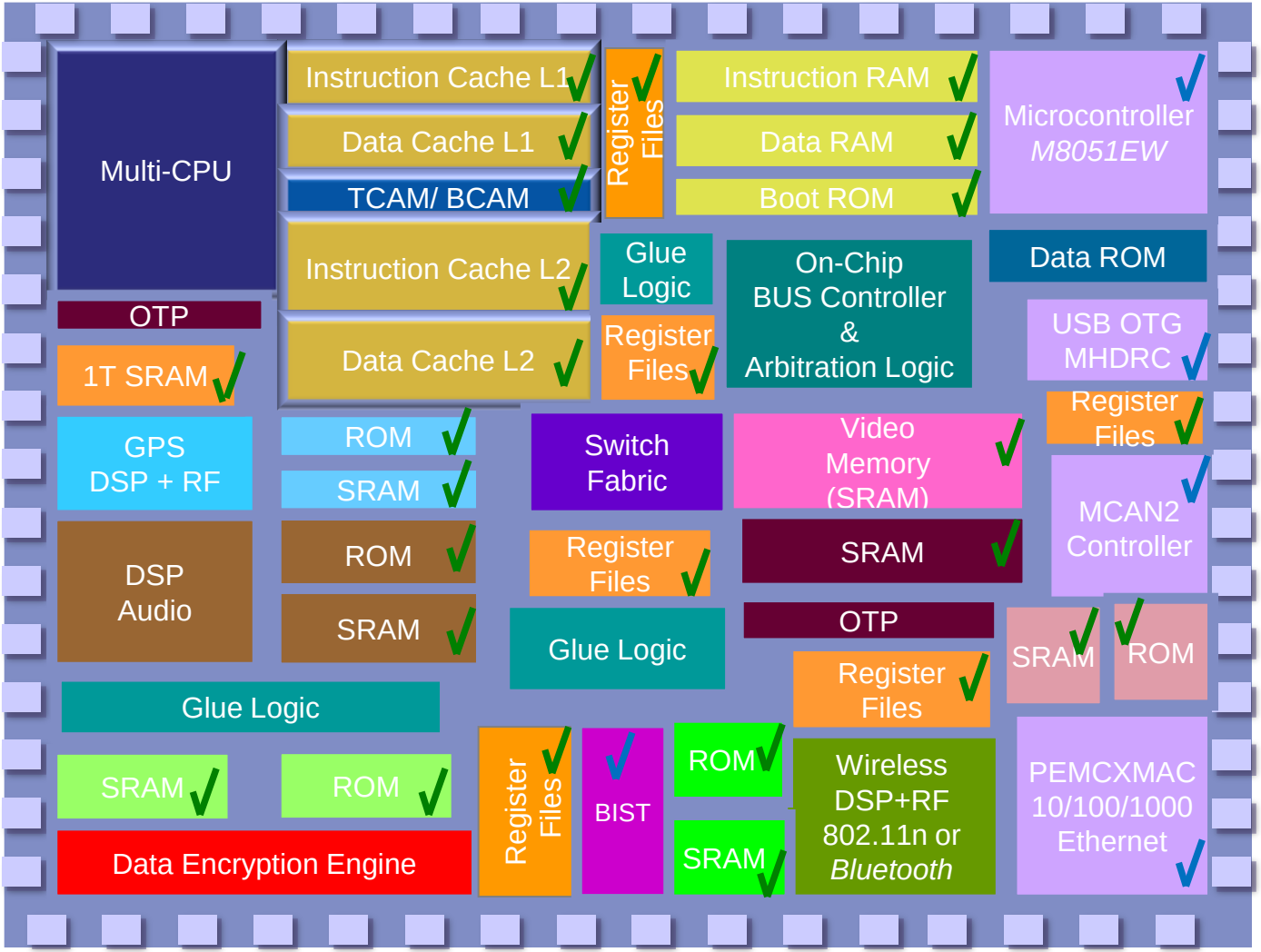
coolSRAM-1T / Shmoo (TSMC 130nm) 1.5V Process



Growth Opportunities

- AI/VR/ MR/ ML/ Wearable:
  - 65nm LP/ 55nm ULP/ 40 LP/ 28nm HPC+
- IOT
  - 28nm HPC+/ 40 ULP/110nm LP/152nm LP
- Automotive:
  - 28nm HPC+/ 110nm LP/65nm LP/ 55nmLP
    - EMI

Differentiated IPs For Adding Value to Customer SOCs



Differentiated Memory IPs enable SOC designers to Reduce Power & Cost

- Architectural Analysis (Dynamic Power, Leakage, speed, area)
  - Using MemQuest with wide Field-Of-Use
- Lowest Dynamic Power & Leakage
  - HD/ULL bitcell & SVT/LVT/HVT/uHVT Periphery
  - Dual-VDD offering
- Smallest Area
- Fastest Speed
- Highest Quality with Transistor-based Verification
- Creative Value Added **Services**
  - Special PVT corner , PPA, & EMI analysis
  - Deep N-Well compatibility analysis
  - Write assist support for minimum VDD
  - Minimize routing congestion
  - Test Chip & Characterization Report
  - Full Integration with Tessent BIST/BISR/ATPG
  - Engineering & pre/post Support team

Microsoft Point of View: Advantages of on-chip memory & Mentor's coolSRAMs

- On-chip memories preferred to going off chip
  - Interface power loss
  - Transmission power
  - Board real estate / components / cost
- We have used Mentor's 1-T memories in the past to get high density
- Current chip had complex constraints : high speed, low power, area & shutdown modes
- Employed 6T SRAMs and 6T (8T) single (dual) ported register files
- Selection based on a comprehensive set of evaluation criteria which considered the following
  - Speed
  - Dynamic Power
  - Leakage
  - Area
  - Interoperability with our BIST / DFT tools
  - Power down features
  - Max memory size
  - Compiler flexibility
  - Support

Summary

- Mentor & Novelics Provide Increased Value to Customers
- Embedded Memory Plays a Critical Role in Today's Designs Because it is a Large Portion of the Chip
- Selecting the Correct Memory will Impact
  - Your chip and system power consumption
  - Your chip and system speed
  - Your chip and system manufacturing cost
- Selecting the Right Memory IP and the Right Architecture will Help You Differentiate Your Product
- Q & A

Lets Work Together to Create Differentiated Products

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