Top 10 Techniques to Reduce Power & Cost with Optimum Selection of Memory IPs for SOCs

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Managing Director of IP Division

https://www.mentor.com/products/ip/

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Agenda

SoC Market & Drivers

Top 10 Techniques to Reduce Power & Cost for SoC Designs
1. Level of Abstraction
2. Clock Gating
3. TLS
4. Deep Sleep
5. Shutdown
6. Voltage Impact (Multi-voltage)
7. Multi-VT & ULP
8. Dual-Rail & DVFS
9. MemQuest Configuration Tradeoff
10. coolSRAM-1T & coolROM Impact for cost Saving

Differentiated Memory IPs for SoCs to Reduce Power & Cost

Informative White Papers to Minimize Power & Die Size
— https://www.mentor.com/products/ip/

Q & A
Average SoC Die Area Partitioning

Source: SemicoResearch Corp.- SOC Market Analysis & Forecast 2017

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SoC Area Trend & Effective Techniques to Minimizing IP & IC Power

Source: SemicoResearch Corp.- SOC Market Analysis & Forecast 2017
SoC Power Consumption Trend & Techniques to Minimizing IP & IC Power

Total power dissipated by a CMOS device: \( P = \frac{1}{2} C V^2 f + V I_{\text{leak}} \)

- Power (mW)
- Process Technology
- Years
- Dynamic power
- Leakage power
- 90nm 65nm 45/40nm 32/28nm 16/14nm

**Silicon Process**
- FinFET
- Planar CMOS
- FDSOI

**Architecture**
- RTL-based Estimation & Optimization
- Multi-voltage
- DVFS
- Memory Gating
- Clock Gating
- Multi-sleep

**Optimized Libraries**
- Cool SRAM/coolROM
- STD Cell
- Multi-VT
- ULP/ULL

**OS Control**
- DVFS
- Sleep-run-sleep
- Shutdown
- Peak Power

ITRS SoC-CP Power Consumption Trend*

*Power Consumption based on trend in processing power requirement and extrapolation of current technology

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SoC Power Consumption Trend & Techniques to Minimizing IP & IC Power

Total power dissipated by a CMOS device: \[ P = AV^2f + VI_{\text{leak}} \]

### Architecture
- RTL-based Estimation & Optimization
- Multi-voltage
- DVFS
- Memory Gating
- Clock Gating
- Multi-sleep

### Silicon Process
- FinFET
- Planer CMOS
- FDSOI

### OS Control
- DVFS
- Sleep-run-sleep
- Shutdown
- Peak Power

### Optimized Libraries
- Cool SRAM/coolROM
- STD Cell
- Multi-VT
- ULP/ULL

ITRS SoC-CP Power Consumption Trend*
Greatest Impact on Power is at RTL and Above

- Micro-Architecture
  - Block level clock gating
  - Shift registers to pointer structures
  - Flop cloning/sharing
  - Memory/register file banking
  - Memory caching

- RTL
  - Combinational clock gating
  - Sequential clock gating
  - Memory gating
  - Data gating

- Physical Implementation
  - Multi-Vdd, Multi-Vth technology mapping
  - Clock network optimization
  - High-k transistors
  - Novel circuit structures/logic families
PowerPro® Takes into Account Timing Specs and Power Trade-offs to Reduce the Power of memory intensive SoC

PowerPro Memory Gating insures “Light Sleep” (LS or TLS) signal meets Trlsc and Tflsc requirements

PowerPro, an automation tool for Estimation & Optimization
coolSRAM-6T
Power Reduction Techniques

- **Transparent Light Sleep**, full data retention
  - Patented Automatic Transparent Source Biasing Leakage Reduction
  - Leakage Reduction > 50%
  - Zero Latency

- **Deep Sleep for Power Gating**
  - Periphery shutdown with full data retention
  - Optional isolation cells on input/output pins
  - Leakage reduction > 70%

- **Shut Down for Power Gating**
  - No data retention
  - Leakage reduction > 95%
  - Output Isolation options (Pull down or floating)

- **Multi-VT support in Periphery**
  - HVT to reduce leakage
  - LVT to maximize speed
  - SVT to minimize wafer cost
  - MemQuest selectable
### TSMC-28HPCplus Power Reduction Features (coolSRAM-6T)

- 512Kb TSMC-28HPC+ coolSRAM-6T SVT Bitcell

<table>
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<tr>
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<th>Leakage Reduction Feature</th>
<th>Active Leakage</th>
<th>Deep Sleep Leakage</th>
<th>Shutdown Leakage</th>
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# TSMC-28HPCplus Benchmark Comparison (coolSRAM-6T)

## 540Kb coolSRAM-6T SVT Bitcell SVT Periphery Comparison

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<th></th>
<th>Area</th>
<th>WC Leakage</th>
<th>Typ Leakage</th>
<th>Customer Use-case WC Total Power</th>
<th>Customer Use-case Typ Total Power</th>
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<td>Mentor / Competitor</td>
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<td>22%</td>
<td>25%</td>
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<td>80%</td>
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<tr>
<td>Mentor / Foundry Provided</td>
<td>98%</td>
<td>20%</td>
<td>25%</td>
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## 540Kb coolSRAM-6T ULL Bitcell HVT/UHVT Periphery Comparison

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<th>Typ Dynamic Power</th>
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<tr>
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<td>150%</td>
<td>85%</td>
<td>65%</td>
<td>60%</td>
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ULP and uLL Technology for Power Reduction

- Memory IP Offering in TSMC ULP and uLL Technologies
  - 40ULP: nominal voltage 0.9v, write-assist required
  - 55ULP: nominal voltage 0.9v, write-assist required for UHD bitcell
  - 28HPC+ uLL: nominal voltage 0.9v, write-assist required

- ULP/uLL vs. LP
  - Lower voltage / power / leakage
  - Slower speed

- Multi-vt Periphery Further Reduces Leakage
  - 40ULP and 55ULP: hvt, uhvt
  - 28nm HPC+: hvt, uhvt

- Custom Features
  - Dual rail for additional dynamic power reduction
  - coolROM with Novelics bitcell runs at ultra-low voltage
  - Forward body-bias in slow corners for performance enhancement
TSMC-55ULP vs TSMC-55LP Benchmark Comparison (coolSRAM-6T)

- 5120 x 32 coolSRAM-6T Instance With TLS, Deep Sleep, and Shutdown

### PVT Conditions:
- TSMC-55LP: WC = SS 1.08V 125C; TC = TT 1.20V 25C; BC = FF 1.32V 125C
- TSMC-55ULP: WC = SS 0.81V -40C; TC = TT 0.90V 25C; BC = FF 0.99V 125C

### Comparison Results
- 55LP is 2.6x faster
- 55ULP dynamic power is 44% less
- 55ULP active leakage is 60% less
- 55ULP retention leakage is 71% less
  - 55LP Vnom = 1.2V; 55ULP Vnom = 0.9V

### Vendor INSTANCE Area Access Time Max Frequency Active Power Active Leakage Deep Sleep Leakage
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<th>Vendor</th>
<th>INSTANCE</th>
<th>Area (mm^2)</th>
<th>Access Time (ns)</th>
<th>Max Frequency (MHz)</th>
<th>Active Power (uW/MHz)</th>
<th>Active Leakage (mA)</th>
<th>Deep Sleep Leakage (mA)</th>
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<tr>
<td>TSMC-55LP</td>
<td>5120x32</td>
<td>0.124155</td>
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<td>10.47</td>
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<td>TSMC-55ULP</td>
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<tr>
<td>Comparison = 55ULP / 55LP</td>
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<td>221%</td>
<td>38%</td>
<td>56%</td>
<td>40%</td>
<td>29%</td>
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coolSRAM-6T / Dual Rail Supply for Power Minimization

- Power is provided on two rails
  - Normal supply voltage VDDH down to VDD-10% for the bitcell and memory controller circuits
  - Low supply voltage VDDL down to VDD-35% for the memory datapath

- Huge savings for Dynamic Power
  - Dynamic power dissipation is split 1/3 to VDDH and 2/3 to VDDL

- Big savings for Leakage Power
  - Fully compatible with Automatic LPM, Sleep with data retention and full shut down.

- Minimal area impact

- Can still operate at high speed

Comparing of DR to SR, Dual Rail saves 20% of dynamic power and 15% of static power. As a trade-off, it is 3% bigger and 47% slower than Single Rail.
MemQuest™: Web-based Memory Compiler

Full nodes: 180nm, 130nm, 90nm, 65nm, 45nm

Half nodes: 160nm, 152nm, 110nm, 55nm, 40nm, 28nm HPM/HPC+

Roadmap – 16/12 nm, 10/7 nm FF+
### MemQuest for TSMC Customers
Shorten Design Cycle for Architectural Analysis & in sync with TSMC Silicon

#### Sort by Dynamic Power

<table>
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<tr>
<th>Selection</th>
<th>Area (mm²)</th>
<th>X (mm)</th>
<th>Y (mm)</th>
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<td>1.82</td>
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#### Sort by Leakage Current
MemQuest / Architectural Analysis

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<th>Y (mm)</th>
<th>Max Frequency (MHz)</th>
<th>Access Time (ns)</th>
<th>Dynamic Power (µW/MHz)</th>
<th>Active Leakage (mA)</th>
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<td>coolSRAM-6T (SP), Optimized for large instances</td>
<td>coolREG-8T (2P &amp; DP), Optimized for small instances</td>
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<td>128 - 64K</td>
<td>2K - 64K</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WORD_WIDTH</td>
<td></td>
<td>2 - 288</td>
<td>2 - 144</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 - 144</td>
<td>4 - 256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 - 512</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MUX</td>
<td>number of blocks</td>
<td>2, 4, 8, 16, 32</td>
<td>4, 8, 16, 32</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1, 2, 4</td>
<td>1 - 144</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 - 144</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Banking</td>
<td>select bit/byte write</td>
<td>0, 1, 8</td>
<td>0, 1, 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0, 1, 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/byte write</td>
<td>select bit/byte write</td>
<td>0, 1, 8</td>
<td>0, 1, 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>maximum bits per instance</td>
<td>1M bit</td>
<td>72K bit</td>
<td>36K bit</td>
<td>1M bit</td>
<td>4M bit</td>
<td>180nm to 55nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1M bit</td>
<td>1/2 M bit for 28 nm HPC</td>
<td>180nm to 55nm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Wearable use case – power profile

- Battery: 150mAh
- Lifetime: 1 week
- System current: 892µA at battery

- Budget for always-on: 20% $ \rightarrow 178 \text{uA}_{\text{bat}}$
- Budget for device: 526µW (subtract regulators)

M4 Batch processing + FFE sensor read + Wristup (Display off)

$< 120 \text{uA}_{\text{bat}}$

Total Average: 402 uA
Sensor Architecture

- Multi core processing
  - Dedicated audio processing @50 uA
  - Dedicated sensor compute @35 uA/MHz
  - General purpose ARM CPU @75 uA/MHz

- coolSRAM-6T*
  - 512k (128k Always On) GF 40nm-LP @7 uW/Mhz
  - 2.28 uA leakage current (8k block)

*Mentor coolSRAM-6T offered Lowest leakage & active current which allows ultra low power Always-On processing of audio/sensor data
High volume SOC: Image Sensor design with coolSRAM-6T @ DAC 2017
Ultra Low Power Memory/ High Density IPs for AI Applications
Mentor Memory IPs with ultra low leakage & enables customers audio processing with better performance & die size reduction and minimized power consumption
Mentor Memory IPs with lowest dynamic power for DSP processing in audio application
coolSRAM-1T / Advantages

✓ **High Density**
   - Compiled to your exact specification
   - Save up to 25%-50% area compared to SRAM-6T

✓ **100% Standard CMOS Process**
   - No special layer
   - No extra mask

✓ **Low Leakage**
   - Single transistor bitcell (vs 6 transistor for SRAM-6T)
   - IO transistor bitcell (vs core device for SRAM-6T)
   - Large percentage of periphery is also IO device

✓ **Silicon Proven**
   - Silicon success in 180nm-65nm
   - Across multiple foundries
coolSRAM-1T / Memory Density Scaling
coolROM / Architecture

- Novelics Proprietary NAND bitcell
- Up to 2Mbit per Macro
  - Logical: Max 128K entries, 256 wide bus
  - Physical: Max 2K rows, 1024 columns
- Multiple Banks
  - MemQuest selectable up to 8 banks
  - Smaller bank size → Higher speed
  - Active power dissipation localized to the active bank
### 28HPCplus Benchmark Comparison (coolROM)

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3328 x 9</td>
</tr>
<tr>
<td>Foundry Area (um^2)</td>
<td></td>
</tr>
<tr>
<td>Mentor Area (um^2)</td>
<td></td>
</tr>
<tr>
<td>Mentor Area Saving</td>
<td>53%</td>
</tr>
</tbody>
</table>

- **Novelics IP Advantage:**
  - Up to **61%** area saving
coolSRAM / Column Redundancy
Yield Enhancement for Cost Saving

- One spare unit per butterfly wing
- Consider when aggregate memory is > 2Mbits
  - For macros > ¼ MBit
- Small area overhead, negligible performance overhead
- Fully compatible with Tessent for automation of BIST/BISR
High volume SOC: Image/Depth Sensor design with coolSRAM-1T @ DAC 2016
## Higher Density IPs & Cost Saving

<table>
<thead>
<tr>
<th>IP Type Used</th>
<th>Memory in Chip</th>
<th>IP Area Saving</th>
<th>Die Cost</th>
<th>Cost Saving</th>
<th>Average ICs/Month</th>
<th>Months of Life</th>
<th>Cost Saving</th>
</tr>
</thead>
<tbody>
<tr>
<td>coolSRAM-6T, coolREG-6T/8T, coolROM</td>
<td>40%</td>
<td>25%</td>
<td>$4.00</td>
<td>$0.40</td>
<td>500,000</td>
<td>18</td>
<td>$3,600,000</td>
</tr>
<tr>
<td>coolSRAM-1T</td>
<td>50%</td>
<td>50%</td>
<td>$4.00</td>
<td>$1.00</td>
<td>500,000</td>
<td>18</td>
<td>$9,000,000</td>
</tr>
</tbody>
</table>
28nm HPC+ Test Chip

- Testchip for 6 Novelics IP
  - coolSRAM-6T
  - coolREG-6T
  - coolREG-8T (DP)
  - coolREG-8T (2P)
  - coolROM
  - coolCAM

- 5 corner lots
  - TT, SS, FF, SF, FS
  - Lower voltage introduces higher level of Variability
  - Leakage controled, -40 D C to 125 D C
  - Mentor Tessent MBIST
  - PLL for at-speed
    - True Circuits, Inc.

- Direct access to memory pins for setup/hold testing
coolSRAM-6T 28nm HPC+ Shmoo
MED 8192x16 (125C)

- 15 parts tested
- 3 parts per corner:
  - TT
  - SS
  - FF
  - FS
  - SF

- 15 parts pass
- 12 parts pass
- 9 parts pass
- 6 parts pass
- 3 parts pass
- 0 parts pass
coolSRAM-1T “VDD vs Clk Freq” Shmoo (upto 120 Mhz in spec Voltage)
WIDE 512x256 @ 125C (SMIC 110nm)
Standard CMOS Process, No special layer, No extra mask

5 corners
- TT
- SS
- FF
- SF
- FS

VDD_{min} : minimum VDD voltage with 5 corners passing @ 50MHz
coolSRAM-1T / Shmoo (TSMC 130nm)
1.5V Process
Growth Opportunities

- **AI/VR/ MR/ ML/ Wearable:**
  - 65nm LP/ 55nm ULP/ 40 LP/ 28nm HPC+

- **IOT**
  - 28nm HPC+/ 40 ULP/110nm LP/152nm LP

- **Automotive:**
  - 28nm HPC+/ 110nm LP/65nm LP/ 55nmLP
    - EMI
Differentiated IPs For Adding Value to Customer SOCs
Differentiated Memory IPs enable SOC designers to Reduce Power & Cost

- Architectural Analysis (Dynamic Power, Leakage, speed, area)
  - Using MemQuest with wide Field-Of-Use

- Lowest Dynamic Power & Leakage
  - HD/ULL bitcell & SVT/LVT/HVT/uHVT Periphery
  - Dual-VDD offering

- Smallest Area

- Fastest Speed

- Highest Quality with Transistor-based Verification

- Creative Value Added Services
  - Special PVT corner, PPA, & EMI analysis
  - Deep N-Well compatibility analysis
  - Write assist support for minimum VDD
  - Minimize routing congestion
  - Test Chip & Characterization Report
  - Full Integration with Tessent BIST/BISR/ATPG
  - Engineering & pre/post Support team
Microsoft Point of View: Advantages of on-chip memory & Mentor’s coolSRAMs

- On-chip memories preferred to going off chip
  - Interface power loss
  - Transmission power
  - Board real estate / components / cost

- We have used Mentor’s 1-T memories in the past to get high density

- Current chip had complex constraints: high speed, low power, area & shutdown modes

- Employed 6T SRAMs and 6T (8T) single (dual) ported register files

- Selection based on a comprehensive set of evaluation criteria which considered the following
  - Speed
  - Dynamic Power
  - Leakage
  - Area
  - Interoperability with our BIST / DFT tools
  - Power down features
  - Max memory size
  - Compiler flexibility
  - Support
Summary

- Mentor & Novelics Provide Increased Value to Customers
- Embedded Memory Plays a Critical Role in Today’s Designs Because it is a Large Portion of the Chip
- Selecting the Correct Memory will Impact
  - Your chip and system power consumption
  - Your chip and system speed
  - Your chip and system manufacturing cost
- Selecting the Right Memory IP and the Right Architecture will Help You Differentiate Your Product
- Q & A
Lets Work Together to Create Differentiated Products

https://www.mentor.com/products/ip/