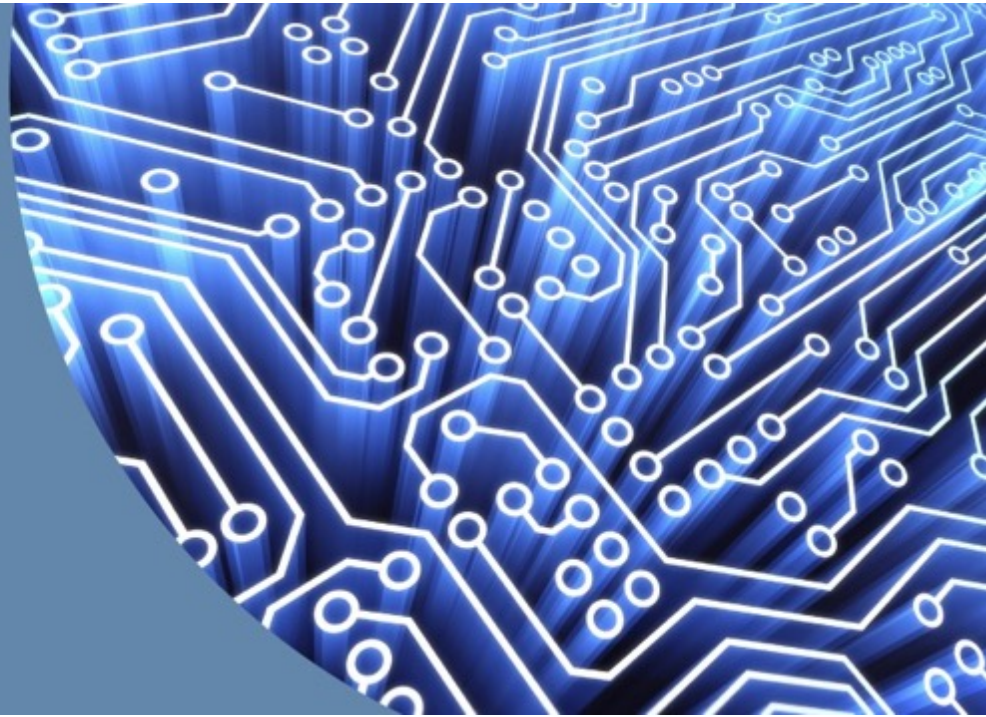
Hardware monitoring and analytics provide the tools for optimization at scale

UltraSoC VP Global Sales – John Hartley

IP SoC Days 2019

- Company Background
- Value Proposition
- Architectural Overview
- Conclusions



Corporate Overview

- VC-funded, Cambridge UK
- Restart 2015
- £4.7M round May ’17
  - New Chairman
    Alberto Sangiovanni-Vincentelli
- 25 patents granted + 16 pending
- Seasoned management team
- Key partners & ecosystem
- Proven technology, proven product-market fit
- Revenue, blue-chip customers, repeat business

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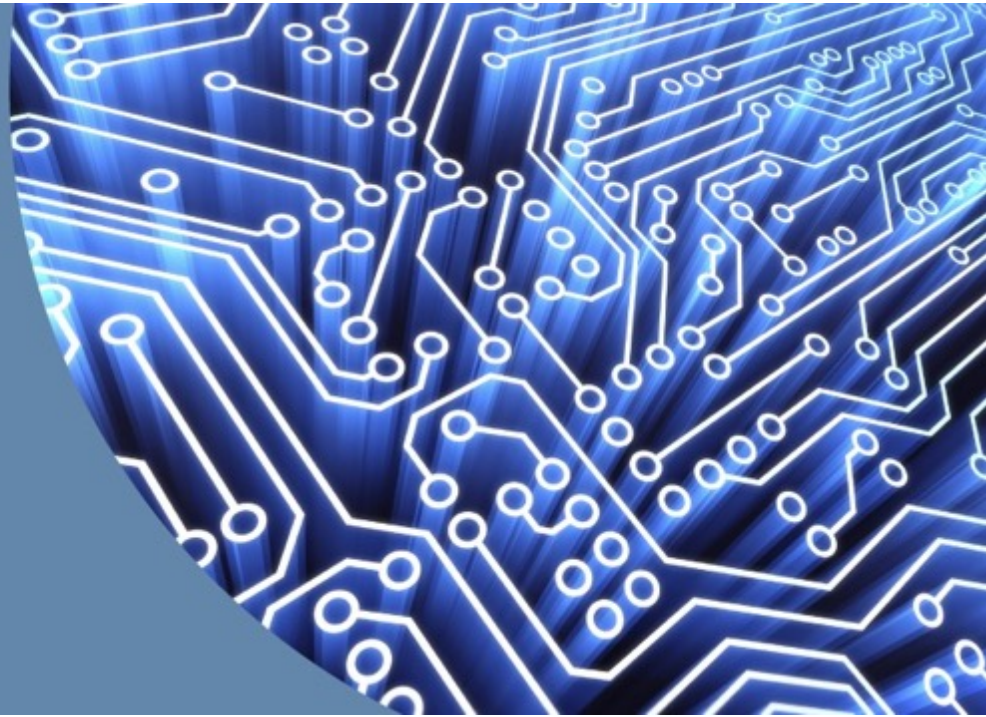
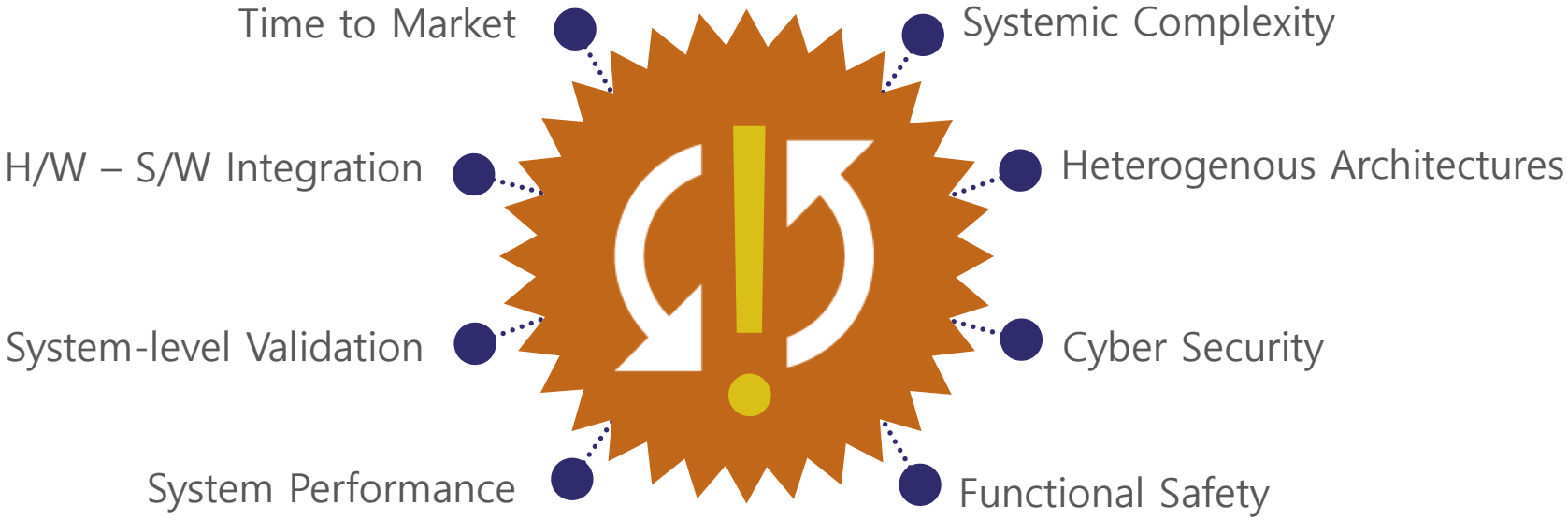


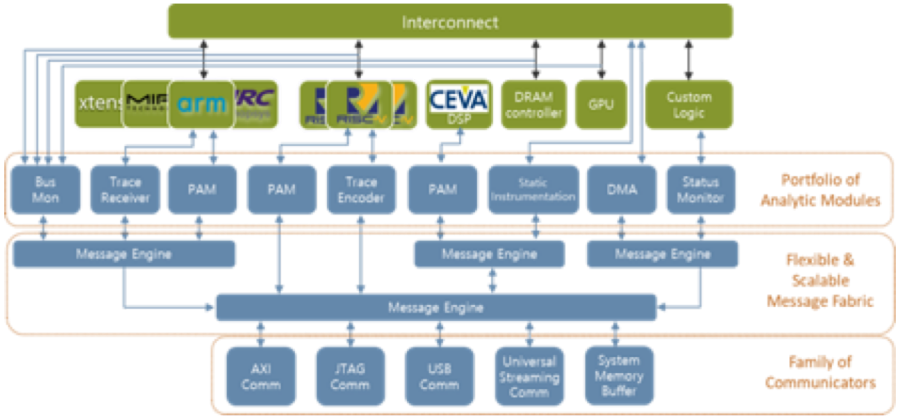
SoC Design Challenges



UltraSoC: on-chip Analytics for SoC as a Whole

A coherent architecture to debug, develop, optimize & secure

- Full SoC visibility, HW & SW
- Support all architectures: Freedom of IP selection
- Real-time & non-intrusive
- Advanced analytics & forensics
- Power/Performance optimization
- “in life” analytics & SLA compliance
- Supports Functional Safety
- Supports Bare Metal Security™
- High-speed debug over USB or SerDes

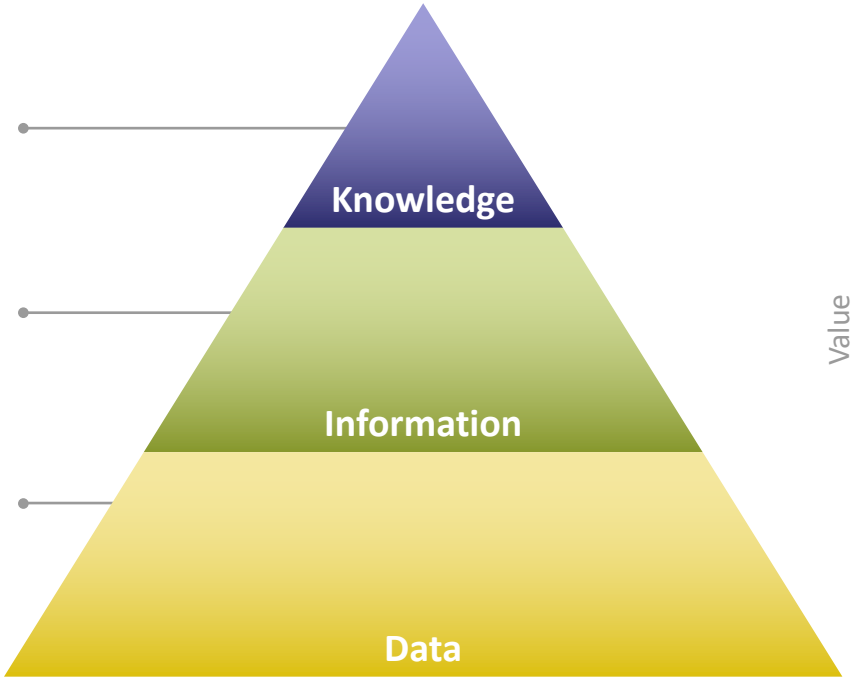


Actionable Insights across the whole SoC

UltraSoC delivers actionable *insights*

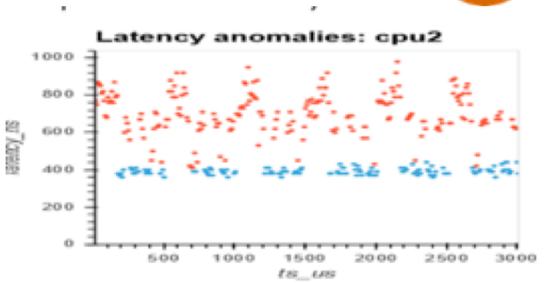
With system-wide *understanding*

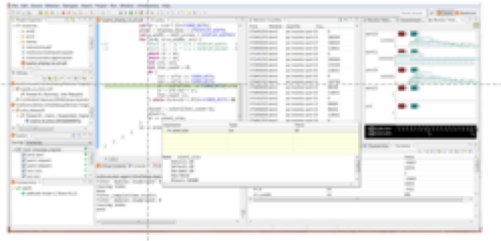
From rich *data* across the whole SoC

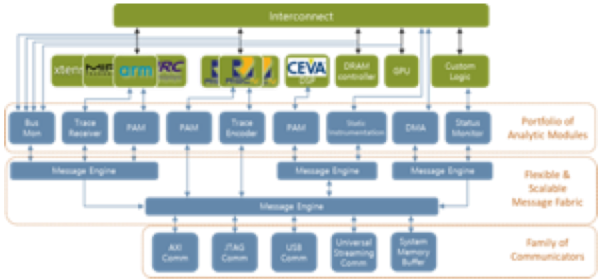


Value

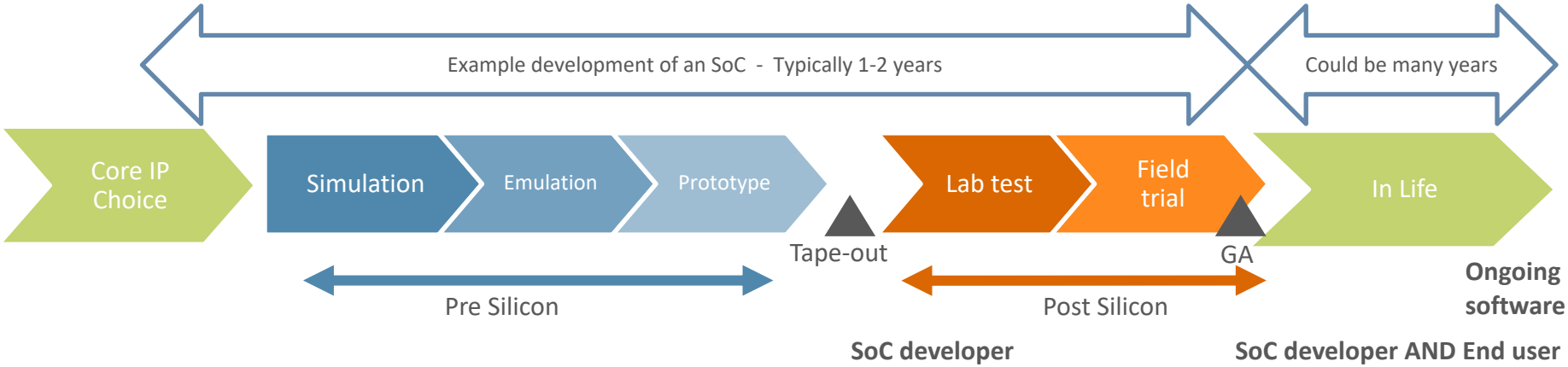
UltraSoC enables *full* visibility of SoC







In development – and beyond



…supports all cores, reducing lock-in, increasing flexibility

…is integrated with the leading simulation and emulation tools

Adds value to emulation & prototyping, accelerates development

…radically improves:

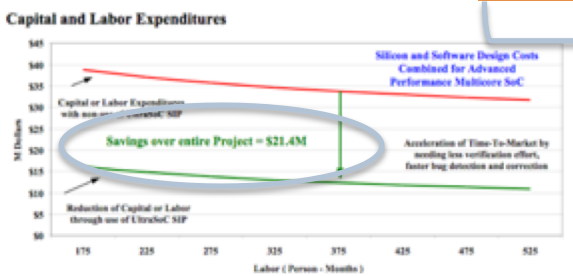
- Time-to-revenue
- Quality / Safety
- Profits due to faster time to market

…detects anomalies:

- optimization, security and functional safety
- Non intrusive

UltraSoC creates value both **in-lab** and **in-life**

Lab test → Field trial → In Life



Comparison of Market Metrics and Sales Results

	Using UltraSoC	Without UltraSoC	Total Market
M Units	41.3	25.6	83.0
Market Share Units	50.0%	30.7%	
Market Revenue M$	$341.9	$181.6	$652.2
Market Share	52.4%	27.9%	
Profits M $	$131.0	$57.3	
Average Gross Margin	38.3%	31.5%	
Breakeven M Units	7.6	14.3	
Aggregate ASP	$8.28	$7.17	Over entire product life

Source: Semico Research Corp.

UltraSoC **accelerates innovation** and maximizes profitability
Faster TTM, higher quality, lower cost & higher margin

UltraSoC **detects threats** and hazards an order of magnitude faster than any other solution – radically increasing security and safety

UltraSoC allows rapid **optimization of application SW**: improving performance, reducing TCO

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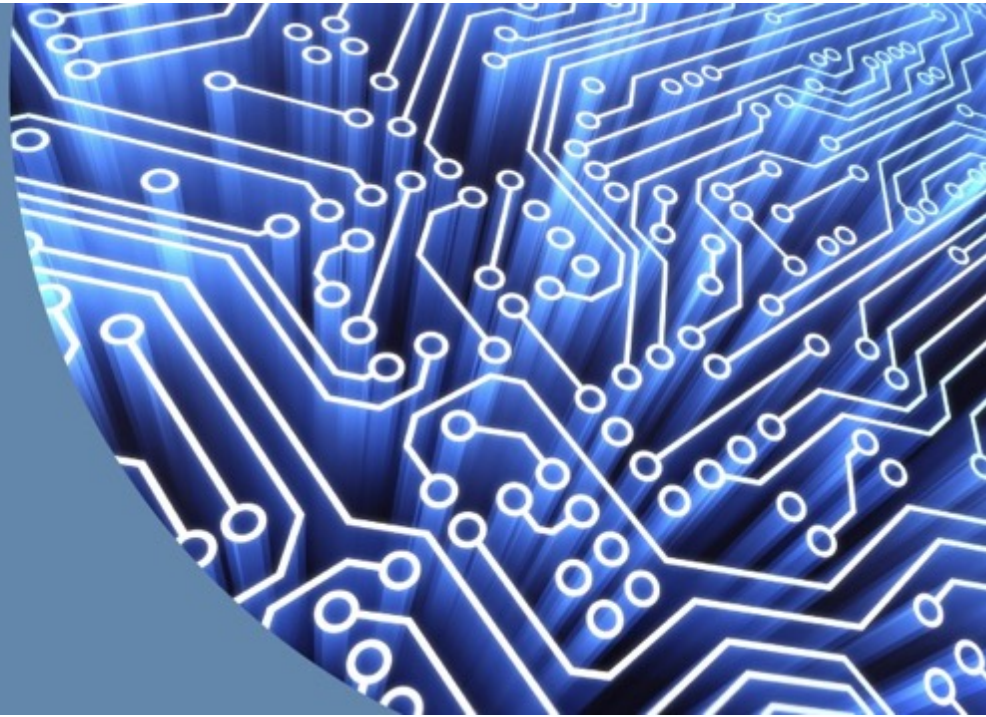
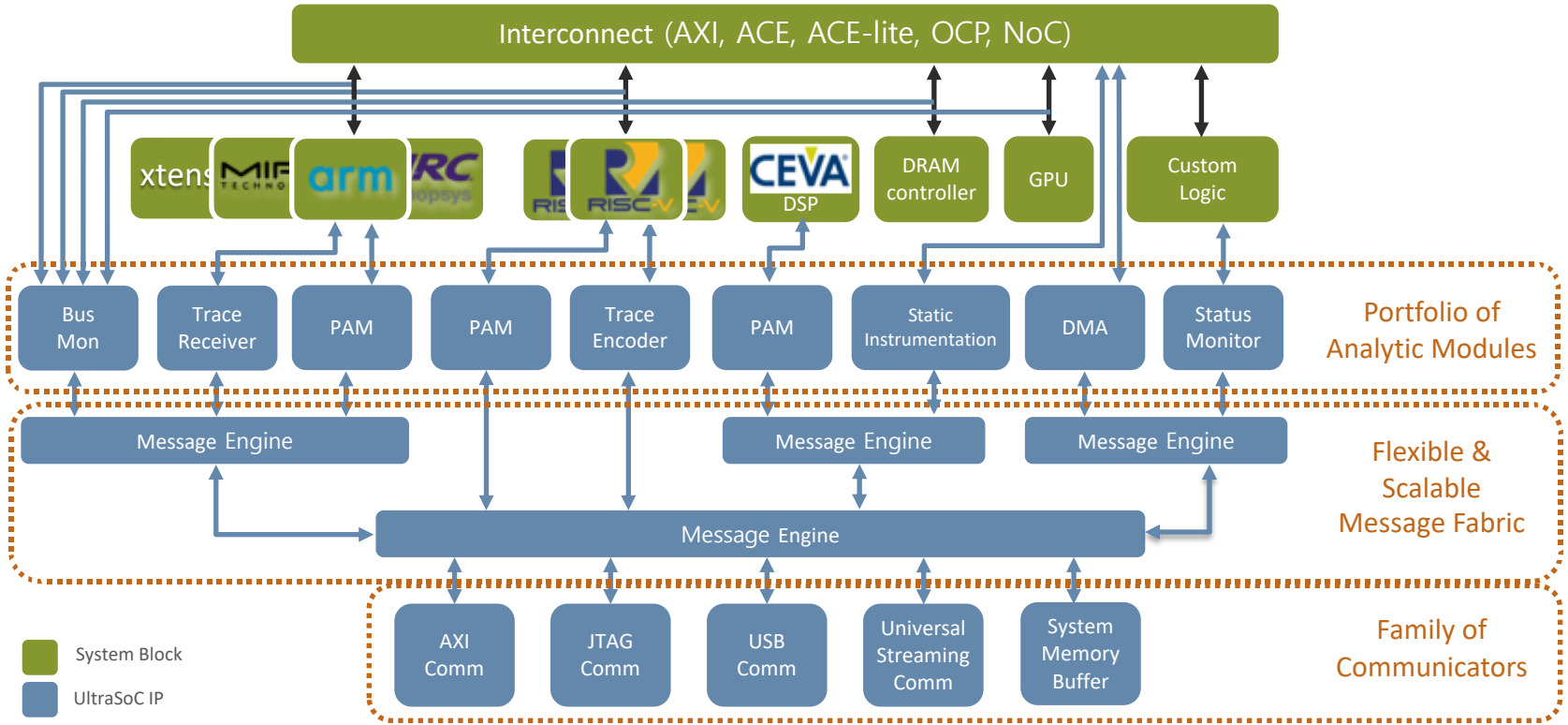
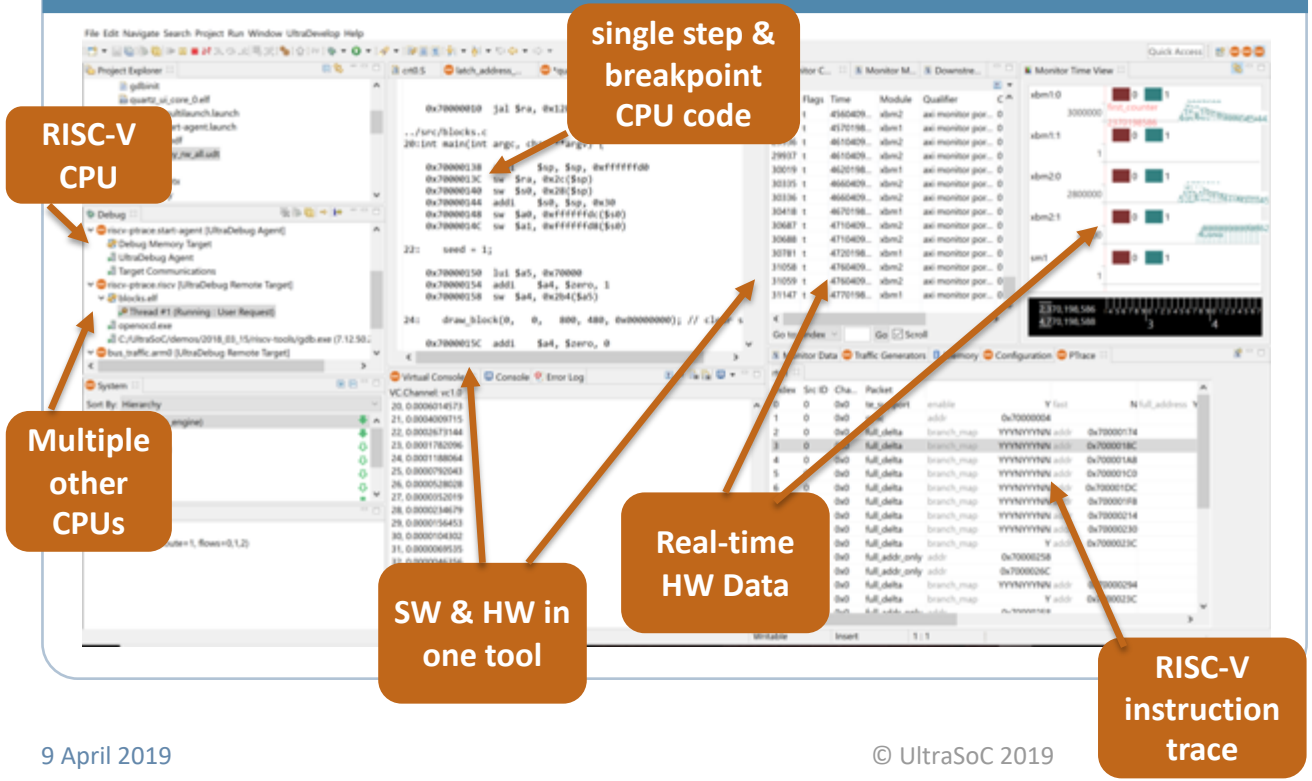


Advanced Debug/Monitoring for the Whole SoC



Software tools for data-driven insights

Eclipse based UltraDevelop 2 IDE



Third Party Tool Vendor Partnerships

UltraDevelop interfaces with almost all common validation and verification solutions:

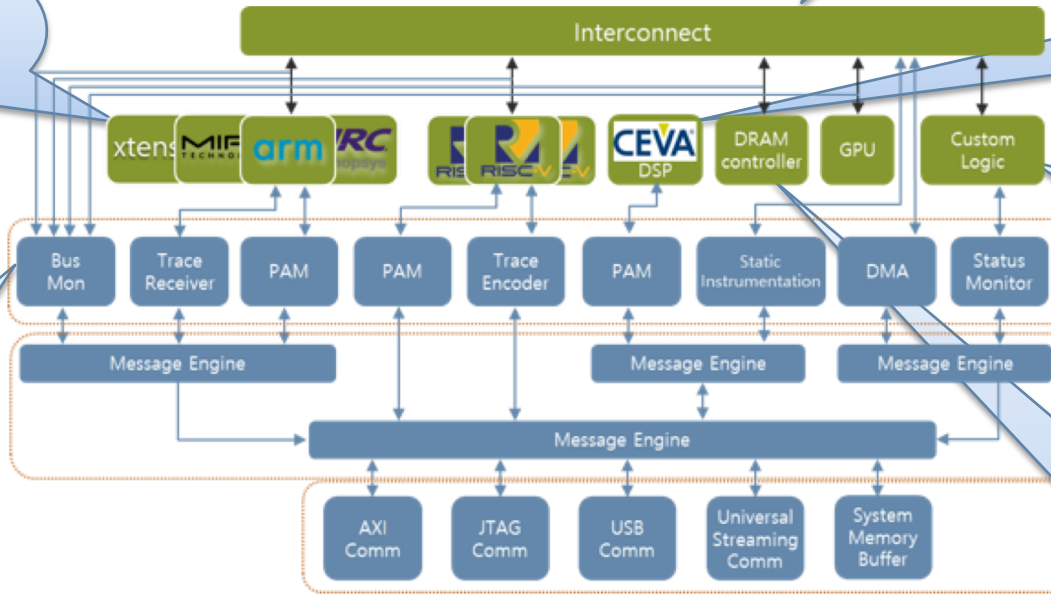
arm
cadence
CEVA
Green Hills SOFTWARE
eclipse
IMG Systems
LAUTERBACH DEVELOPMENT TOOLS
SYNOPSYS
imperas
TELEDYNE LECROY Everywhereyoulook

Technical Problems UltraSoC Solves

Why do some DMA transfers take too long?

What is the mismatch between the host & the DSP?

Why is the CPU not as fast as expected?



Can I trust system security?

Why does the system occasionally hang or deadlock?

What is going on with my memory controller?

UltraSoC is a modular IP platform

[Representative # of gates]

ANALYTIC

Processor [23k]

ARM cadence CEVA Imagination RISC-V SYNOPSYS

Direct interface to CPU or DSP to control core and access rich debug information

Bus Monitor [60k]

AXI3/AXI4/ACE/AHB/OCP/CHI

Protocol-aware analysis of complex interconnects, master or slave, with smart filtering

Status Monitor [11k]

Non-intrusively monitor custom logic or IP blocks (GPU, security etc.)

MESSAGE

Message Infrastructure [8k per Message Engine]

Provides message routing, buffering and event distribution for triggering

COMMUNICATORS

USB

[20k + 1KB RAM]

Standalone IP, utilising the SoC's PHY and requiring no software

JTAG [20k]

Industry-standard IEEE 1149.1 interface

System Memory Buffer [10k]

Directly store data in system memory for analysis

Universal Streaming [20k]

A range of serial links, including SWD and SerDes

+ 20 additional modules

Total area overhead is typically ~1%

Strategic changes in the market - RISC-V

- UltraSoC has the only commercial development environment for RISC-V
  - Includes run control and trace (inst and data)
  - Heterogeneous, massively multicore
  - FPGA demonstrator, Eclipse IDE (gdb, gcc, openOCD, Imperas MPD)
- Silicon proven solution
- Partnerships with leading core vendors
- RISC-V Foundation member since 2016
  - Chair of trace group, member/contributor debug group

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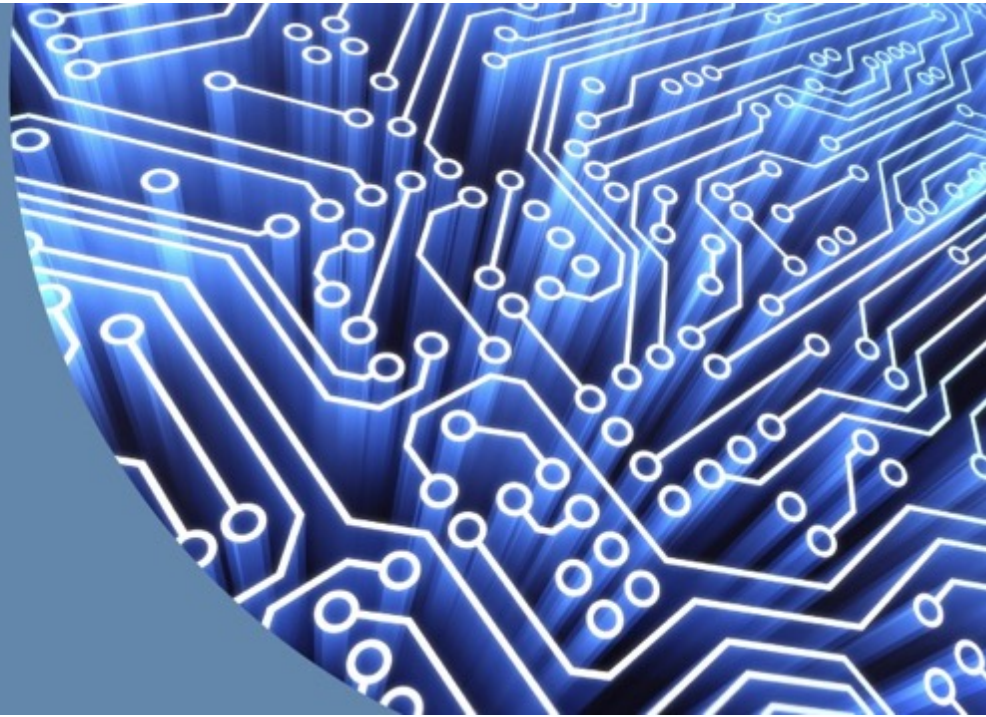

UltraSoC Key Features

Non-intrusive	Debug does not impact/degrade system performance
“Smart” monitors	Detect items of interest in hardware, at wire-speed Massively reduce trace bandwidth & memory Home in on problems efficiently Not necessary to post-process large volumes of data
Protocol-aware bus monitors (AXI, ACE, ACE-Lite, OCP, OCP 2.0, CHI etc)	Identify specific transactions; easily spot problems
Full support for all standard processors (ARM, RISC-V, MIPS, Xtensa, Arc, CEVA, etc)	Uniquely supports heterogeneous architectures; “mix & match” across vendors; fix hardware, software or HW+SW integration
Message-based protocol	Easy to place & route; extensible & versatile; allows local processor for “autonomous” control in the field
Powerful status monitor	Configurable smart logic analyzer for custom logic
Secure	Powerful security architecture

Conclusions

UltraSoC Analytics, Monitoring & Security

- The only commercial heterogeneous solution
- The only commercially available Trace and Debug solution for Risc-V
- Non-intrusive, wire-speed monitors
- Integration Simplicity
- High-speed debug over USB or SerDes
- Enables faster debug, forensics, optimization
  - pre-silicon & post-silicon
- Enables in-life monitoring
  - reliability, compliance & Bare-Metal Security™

UltraSoC – Rich Value Proposition

Time to Market
UltraSoC dramatically accelerates integration & TTM

Systemic Complexity
UltraSoC gives full visibility of whole system

H/W – S/W Integration
UltraSoC gives insight into HW & SW together, in one world

Heterogeneous Architectures
UltraSoC supports all CPUs in one integrated architecture

System-level Validation
UltraSoC enables actionable insight at system-level

Cyber Security
UltraSoC Bare Metal Security™ is a new kind of run-time security

System Performance
UltraSoC enables true run-time system optimization

Functional Safety
UltraSoC improves verification, validation and in-life

Thank you

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