Hardware monitoring and analytics provide the tools for optimization at scale

UltraSoC VP Global Sales – John Hartley

IP SoC Days 2019
Company Background

Value Proposition

Architectural Overview

Conclusions
Corporate Overview

• VC-funded, Cambridge UK
• Restart 2015
• £4.7M round May ’17
  • New Chairman
    Alberto Sangiovanni-Vincentelli
• 25 patents granted + 16 pending
• Seasoned management team
• Key partners & ecosystem
• Proven technology, proven product-market fit
• Revenue, blue-chip customers, repeat business

High profile
Automotive

FAANG
Data centre

ARMv8
Server

Blue chip customers and partners
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SoC Design Challenges

- Time to Market
- H/W – S/W Integration
- System-level Validation
- System Performance
- Systemic Complexity
- Heterogenous Architectures
- Cyber Security
- Functional Safety
A coherent architecture to debug, develop, optimize & secure

- Full SoC visibility, HW & SW
- Support all architectures: Freedom of IP selection
- Real-time & non-intrusive
- Advanced analytics & forensics
- Power/Performance optimization
- “in life” analytics & SLA compliance
- Supports Functional Safety
- Supports Bare Metal Security™
- High-speed debug over USB or SerDes
UltraSoC delivers actionable insights with system-wide understanding from rich data across the whole SoC. UltraSoC enables full visibility of SoC.
In development – and beyond

Example development of an SoC - Typically 1-2 years

To the left: Core IP Choice

- Simulation
- Emulation
- Prototype

To the right: Lab test

- Field trial
- Tape-out
- In Life

Pre Silicon

Post Silicon

SoC developer

SoC developer AND End user

- Core IP Choice
- Supports all cores, reducing lock-in, increasing flexibility

- Simulation
  ...is integrated with the leading simulation and emulation tools
  Adds value to emulation & prototyping, accelerates development

- Lab test
  ...radically improves:
  - Time-to-revenue
  - Quality / Safety
  - Profits due to faster time to market

- Field trial
  ...detects anomalies:
  - optimization, security and functional safety
  - Non intrusive

- Tape-out

- Post Silicon

- Ongoing software

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UltraSoC creates value both in-lab and in-life

- Lab test
- Field trial
- In Life

UltraSoC accelerates innovation and maximizes profitability
Faster TTM, higher quality, lower cost & higher margin

UltraSoC detects threats and hazards an order of magnitude faster than any other solution – radically increasing security and safety

UltraSoC allows rapid optimization of application SW: improving performance, reducing TCO
Software tools for data-driven insights

Eclipse based UltraDevelop 2 IDE

- Single step & breakpoint CPU code
- SW & HW in one tool
- Real-time HW Data
- RISC-V instruction trace

Third Party Tool Vendor Partnerships

UltraDevelop interfaces with almost all common validation and verification solutions:

- arm
- Cadence
- CEVA
- Green Hills Software
- Lauterbach
- eclipse
- Eclipse Development Tools
- Synopsys
- IMAGINE Systems
- Teledyne LeCroy
Technical Problems UltraSoC Solves

Why do some DMA transfers take too long?

What is the mismatch between the host & the DSP?

Can I trust system security?

What is going on with my memory controller?

Why is the CPU not as fast as expected?

Why does the system occasionally hang or deadlock?

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UltraSoC is a modular IP platform

[Representative # of gates]

**Processor [23k]**
Direct interface to CPU or DSP to control core and access rich debug information

**Bus Monitor [60k]**
AXI3/AXI4/ACE/AHB/OCP/CHI
Protocol-aware analysis of complex interconnects, master or slave, with smart filtering

**Status Monitor [11k]**
Non-intrusively monitor custom logic or IP blocks (GPU, security etc.)

**Message Infrastructure [8k per Message Engine]**
Provides message routing, buffering and event distribution for triggering

**USB [20k + 1KB RAM]**
Standalone IP, utilising the SoC’s PHY and requiring no software

**JTAG [20k]**
Industry-standard IEEE 1149.1 interface

**System Memory Buffer [10k]**
Directly store data in system memory for analysis

**Universal Streaming [20k]**
A range of serial links, including SWD and SerDes

**+ 20 additional modules**

**Total area overhead is typically ~1%**

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UltraSoC has the only commercial development environment for RISC-V
- Includes run control and trace (inst and data)
- Heterogeneous, massively multicore
- FPGA demonstrator, Eclipse IDE (gdb, gcc, openOCD, Imperas MPD)

Silicon proven solution
Partnerships with leading core vendors
RISC-V Foundation member since 2016
- Chair of trace group, member/contributor debug group
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## UltraSoC Key Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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<tbody>
<tr>
<td>Non-intrusive</td>
<td>Debug does not impact/degrade system performance</td>
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<tr>
<td>“Smart” monitors</td>
<td>Detect items of interest in hardware, at wire-speed</td>
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<td></td>
<td>Massively reduce trace bandwidth &amp; memory</td>
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<td>Home in on problems efficiently</td>
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<td>Not necessary to post-process large volumes of data</td>
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<tr>
<td>Protocol-aware bus monitors (AXI, ACE, ACE-Lite, OCP, OCP 2.0, CHI etc)</td>
<td>Identify specific transactions; easily spot problems</td>
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<tr>
<td>Full support for all standard processors (ARM, RISC-V, MIPS, Xtensa, Arc, CEVA, etc)</td>
<td>Uniquely supports heterogeneous architectures; “mix &amp; match” across vendors; fix hardware, software or HW+SW integration</td>
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<tr>
<td>Message-based protocol</td>
<td>Easy to place &amp; route; extensible &amp; versatile; allows local processor for “autonomous” control in the field</td>
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<td>Powerful status monitor</td>
<td>Configurable smart logic analyzer for custom logic</td>
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<tr>
<td>Secure</td>
<td>Powerful security architecture</td>
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Conclusions

**UltraSoC Analytics, Monitoring & Security**

- The only commercial heterogeneous solution
- The only commercially available Trace and Debug solution for Risc-V
- Non-intrusive, wire-speed monitors
- Integration Simplicity
- High-speed debug over USB or SerDes
- Enables faster debug, forensics, optimization
  - pre-silicon & post-silicon
- Enables in-life monitoring
  - reliability, compliance & Bare-Metal Security™
UltraSoC – Rich Value Proposition

Time to Market
UltraSoC dramatically accelerates integration & TTM

H/W – S/W Integration
UltraSoC gives insight into HW & SW together, in one world

System-level Validation
UltraSoC enables actionable insight at system-level

System Performance
UltraSoC enables true run-time system optimization

Systemic Complexity
UltraSoC gives full visibility of whole system

Heterogeneous Architectures
UltraSoC supports all CPUs in one integrated architecture

Cyber Security
UltraSoC Bare Metal Security™ is a new kind of run-time security

Functional Safety
UltraSoC improves verification, validation and in-life
Thank you

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