SYNOPSYS®
Silicon to Software™

Enabling 400G Networking with 56G Ethernet PHY IP

D&R IP SoC Days

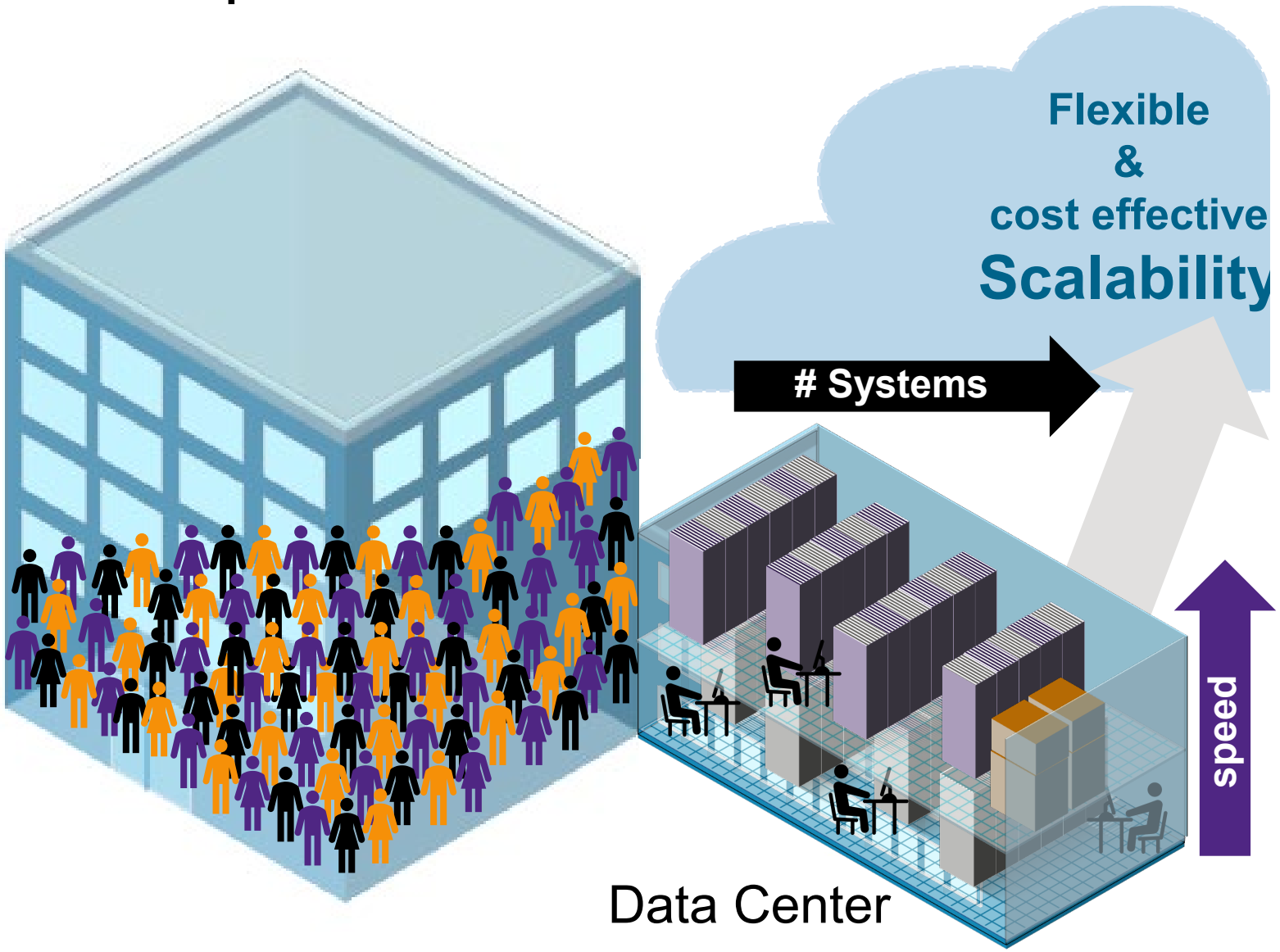
Rita Horner

April 9, 2019

Agenda

- Next-Generation Data Centers
- Multi-Level Modulation
- 56G Ethernet PHY
- High-Speed Ethernet PHY Integration

Enterprise Growth



- **Horizontal Scaling** (a.k.a. scaling out)
  - Additional processing & storage
  - Larger housing area
  - Increased IT management & cooling cost

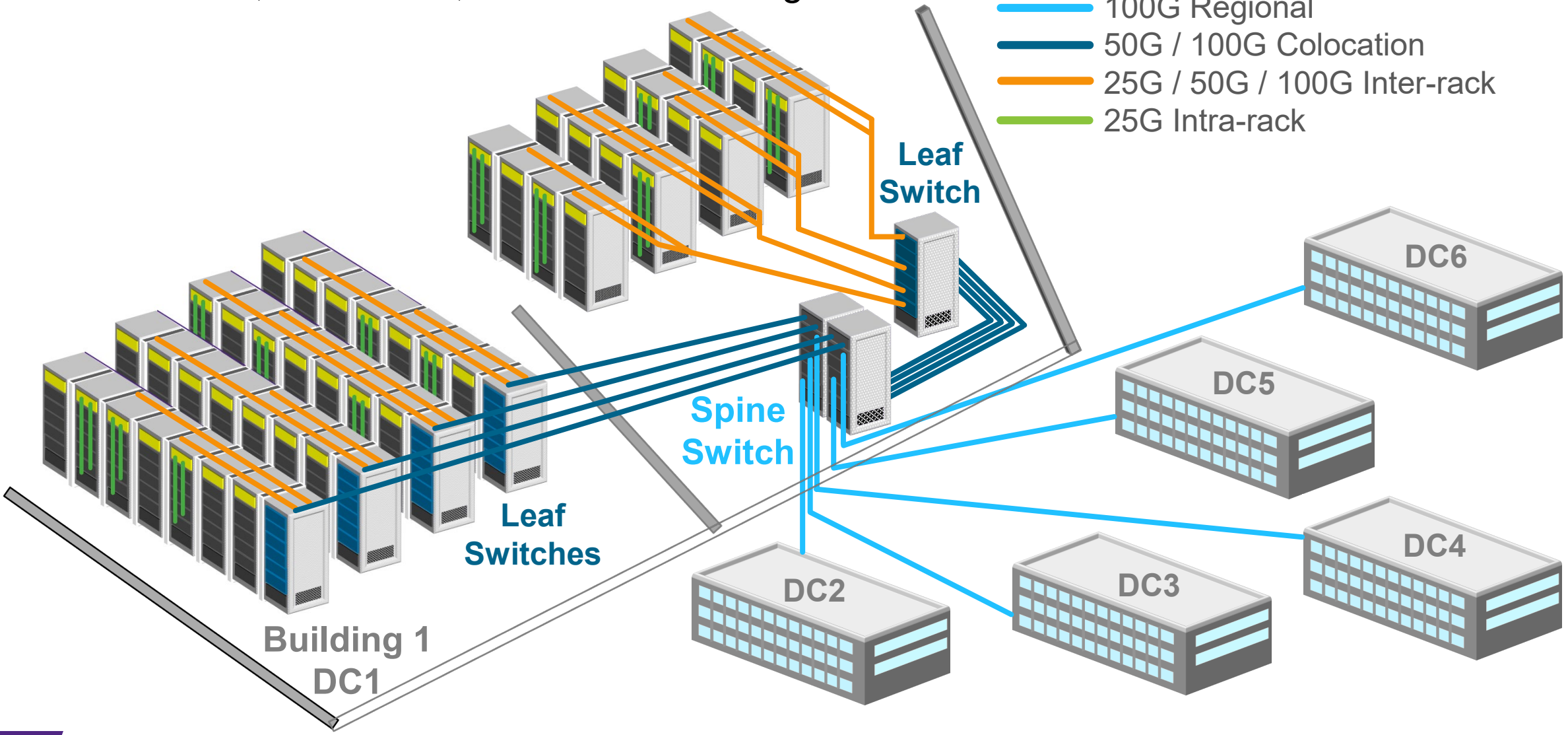
- **Vertical Scaling** (a.k.a. scaling up)
  - Upgraded hardware
  - Potential availability constraints
  - More expensive equipment
  - Ease of control

Facebook Hyperscale Data Center

1.5 Million Square Feet on a 325 Acres (Virginia, US)

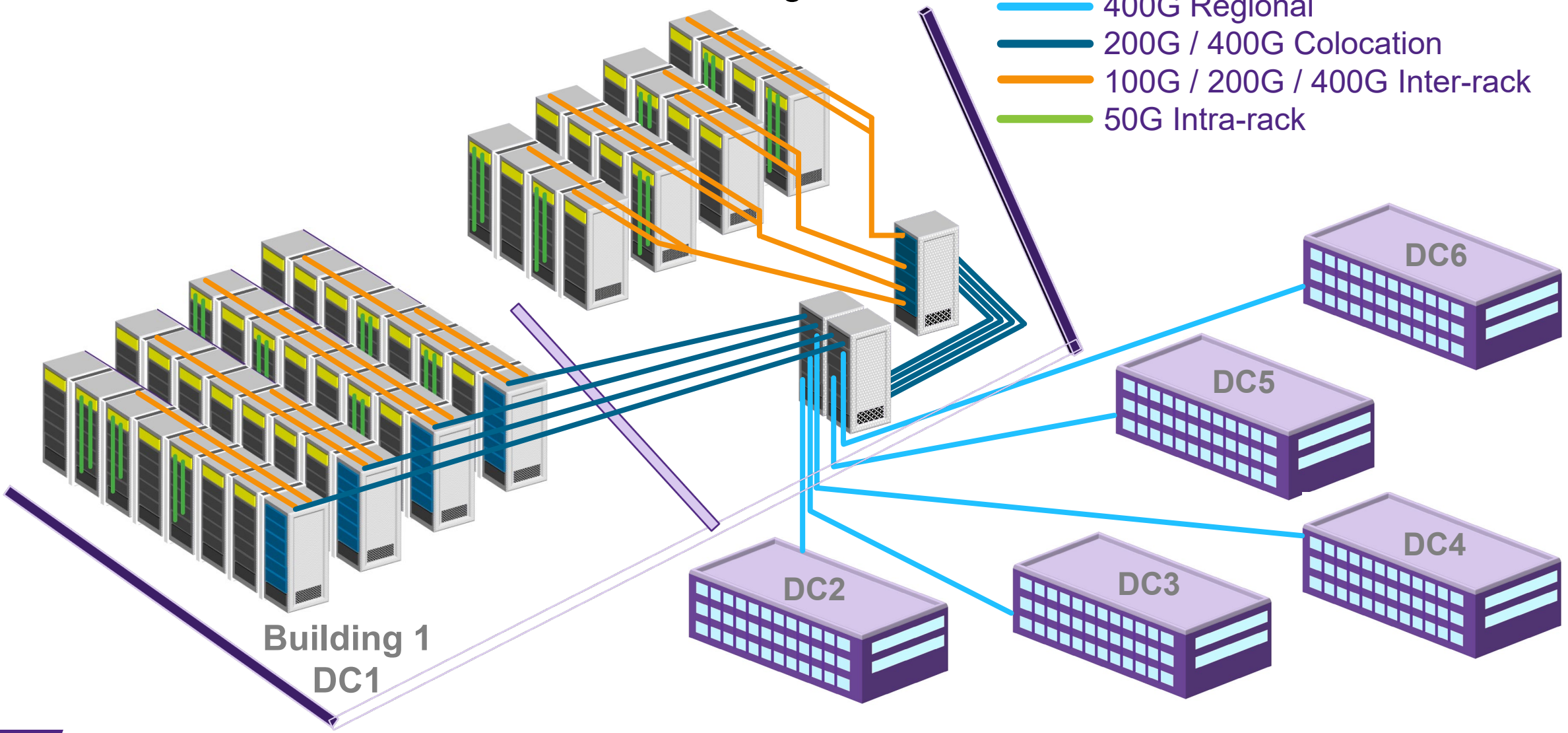
Hyperscale Data Center 100GE Interconnects

Intra-Rack, Inter-Rack, Co-Location & Regional



Hyperscale Data Center 400GE Interconnects

Intra-Rack, Inter-Rack, Co-Location & Regional



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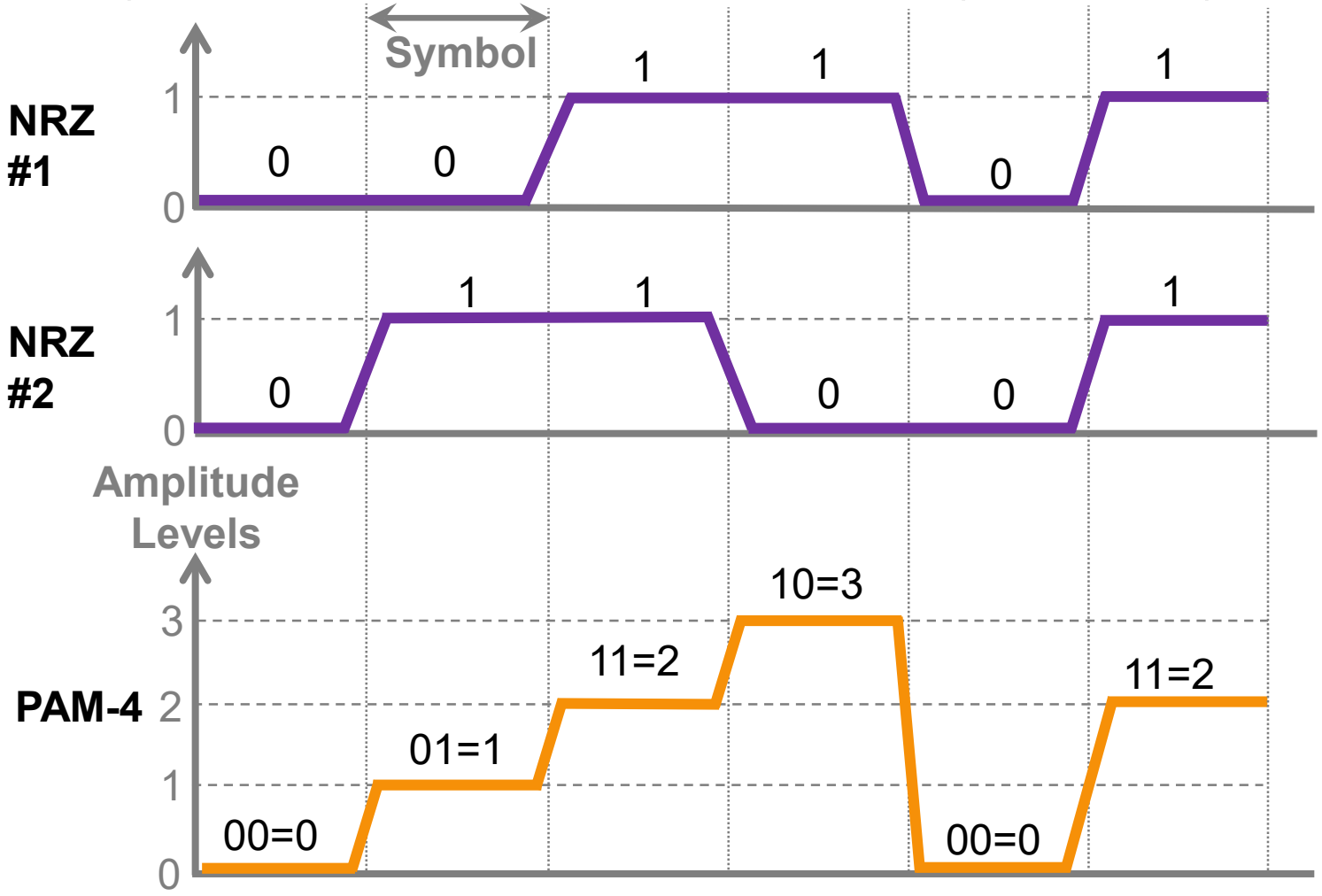
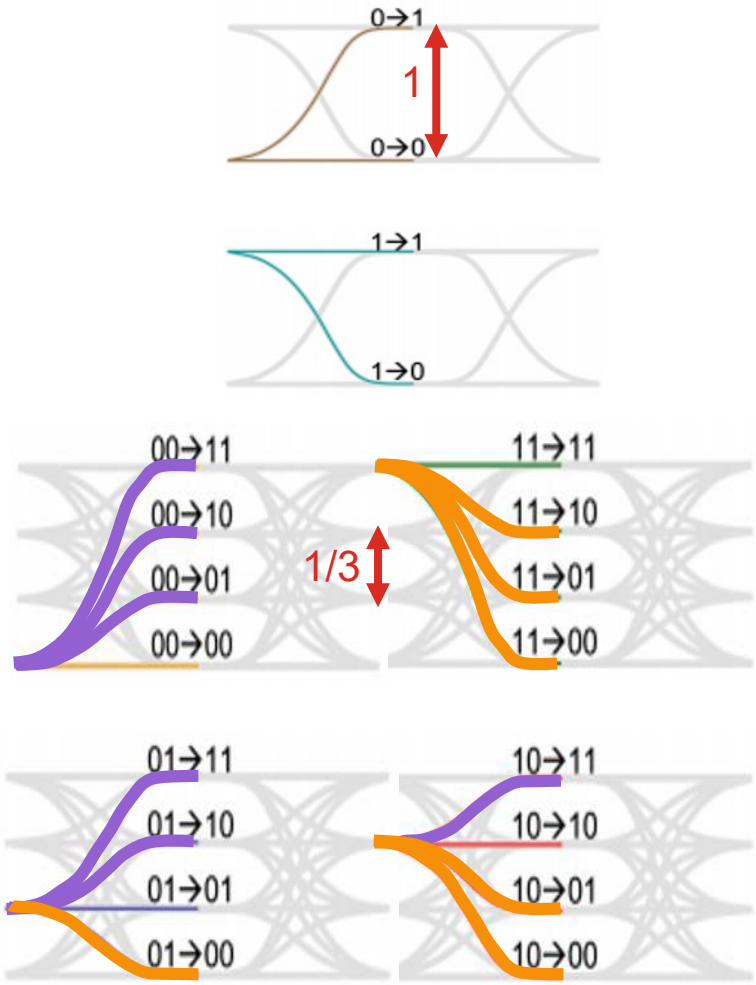
Multi-Level Signaling vs. Binary Modulation

PAM-4 (4-Level Pulse Amplitude Modulation) vs. NRZ (Non Return to Zero)

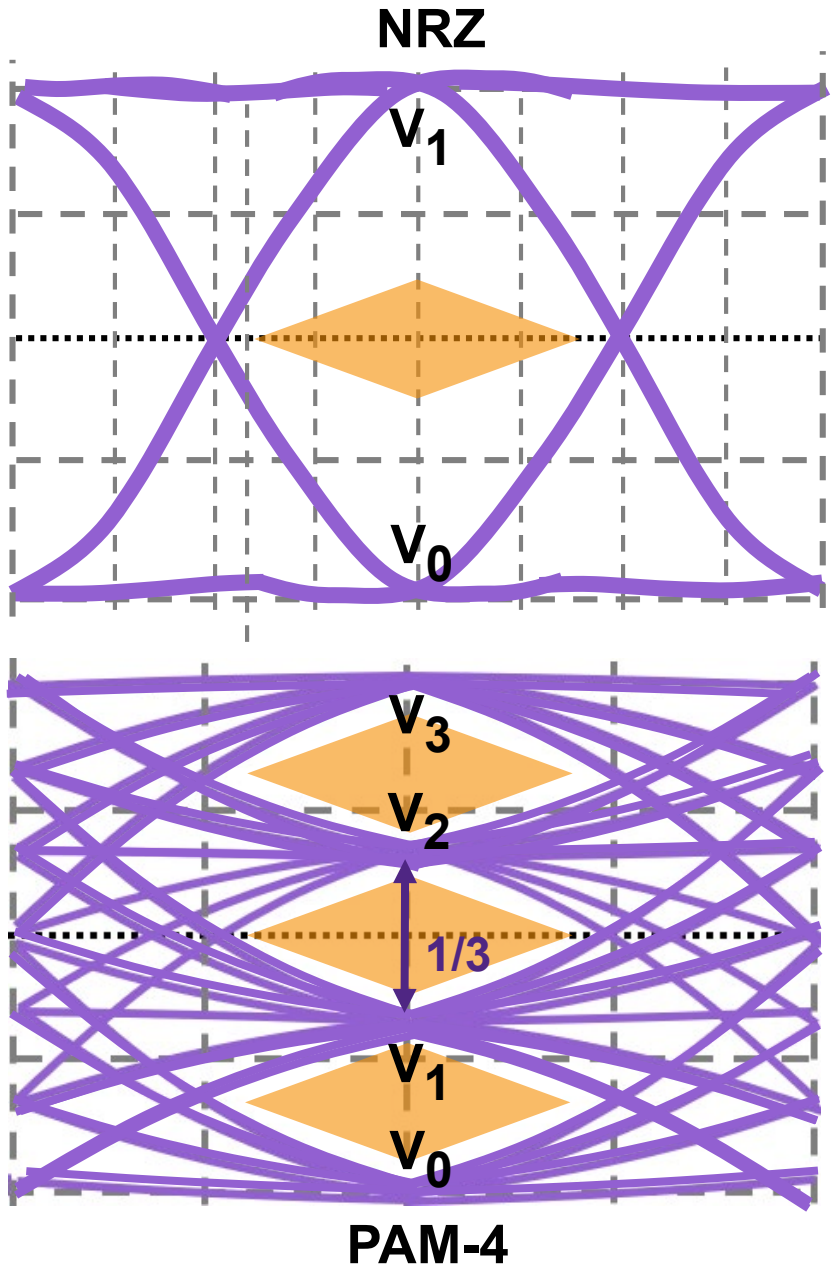




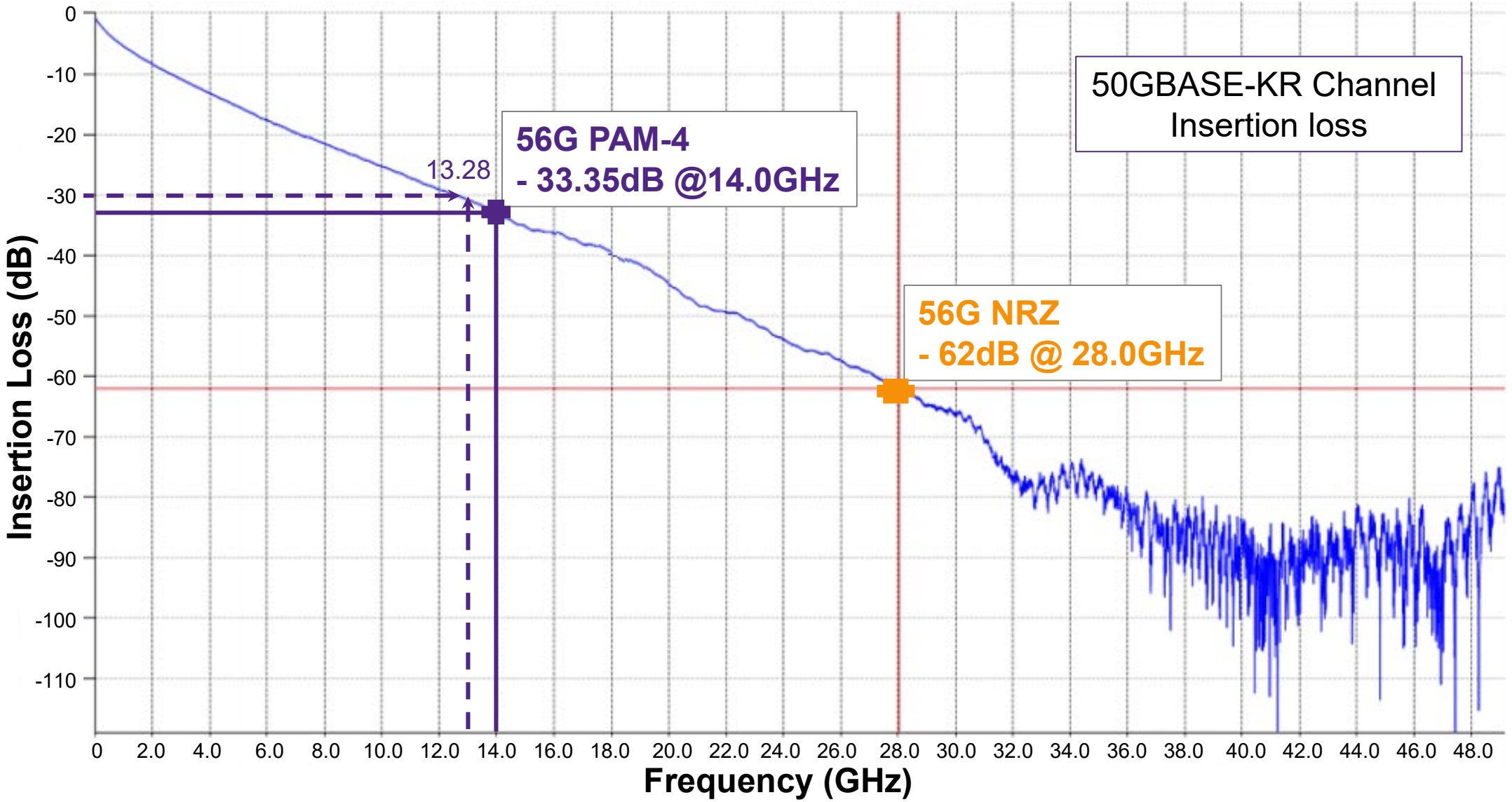
Channel Impairment Impact

PAM-4 vs. NRZ

- Additional voltage levels reduce the eye height by a factor of 3 in PAM-4
  - Signal-to-noise ratio (SNR) degrades
- TX output eye width ➔1/2 to 2/3 of NRZ
  - Middle eye is the most symmetrical
  - Top and bottom eyes do not match the middle eye
- Impairments impact each eye differently
- Nonlinearity can significantly impact bit error rate
- Crosstalk and reflection have greater signal degradation impact



Shift From NRZ To PAM-4



Data Center Interconnects @ 100GE ➔ 400GE

Channel Length, Media, Loss, Width (x4) ➔ *(x8)*

As speeds go up, technology requirements migrate down, and channels shrink

Connection Area	Medium Type	100GE (25G / 50G / 100G)	400GE (50 G / 10G / 200G / 400G)
Regions (Data center-to-data center)	Optical	40km SMF	10km SMF
Colocation (Building-to-building)		10km SMF	2km SMF
Room-to-room		100m MMF	500m SMF
Intra-rack (Rack-to-rack)		30m AOC, MMF	30m AOC, MMF
Inter-rack (within the rack)	Copper -- cable	5m DAC, Twin-axial	3m DAC, Twin-axial
Intra-server	Copper PCB/mezzanine/backplanes	35dB @12.89GHz	30dB @13.28125GHz

Single Mode Fiber (SMF), Multi Mode Fiber (MMF), Active Optical Cable (AOC), Direct Attached Cable (DAC)

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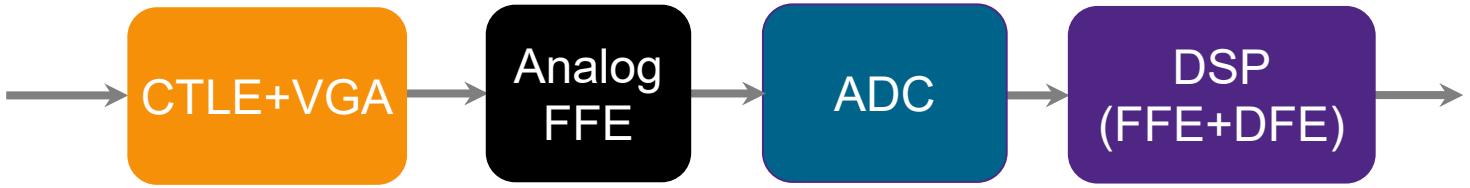
Major Types of PAM-4 Designs

Analog vs. Digital Receiver Architecture

Analog Receiver

- Similar to NRZ receiver design
- PVT variation concern
- Technology scalability
- DFE taps (area + power)
- Ideal for short channels
- Power advantage

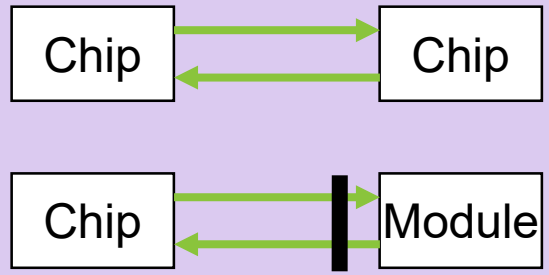
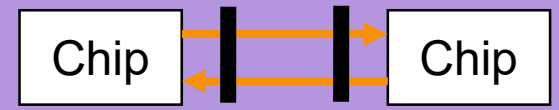


Digital Receiver

- Complex architecture
- Flexibility in process scaling
- More capable signal processing techniques
- Ideal for broad range of channels
- Power disadvantage

IEEE802.3 Standards for Single & Multiple Channel

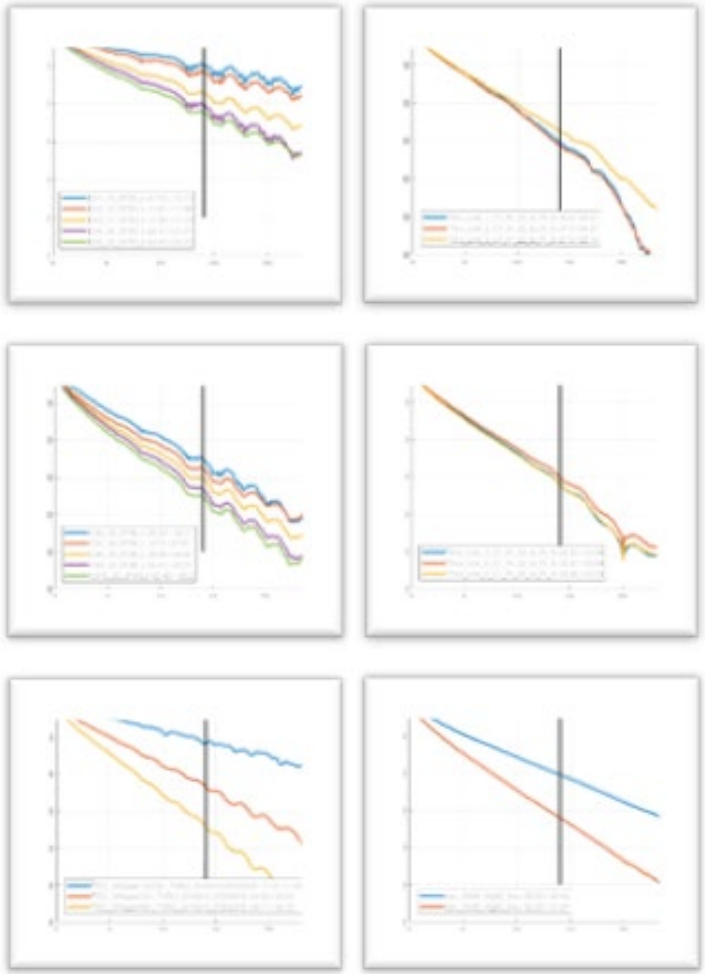
802.3bs (200G & 400G) & 802.3cd (50G, 100G, 200G, 400G) @ 53.125 Gbps

Specifications	Description	
50GAUI-1 100GAUI-2 200GAUI-4 400GAUI-8	Chip-to-chip & Chip-to-module	
50GBASE-CR 100GBASE-CR2 200GBASE-CR4	1-, 2- or 4-lane shielded balanced Twinaxial copper cabling (CR) , 2 m & 3 m	
50GBASE-KR 100GBASE-KR2 200GBASE-KR4	1-, 2- or 4-lane Electrical backplane (KR)	

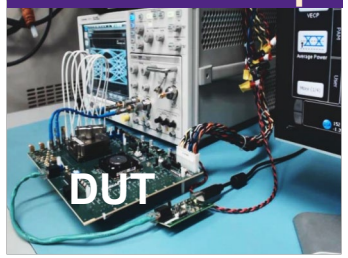
Single & aggregated link rates of up to 400 Gbps

DesignWare 56G Ethernet PHY IP

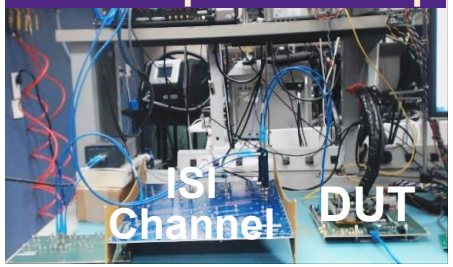
For Next-Generation 400G Hyperscale Data Centers



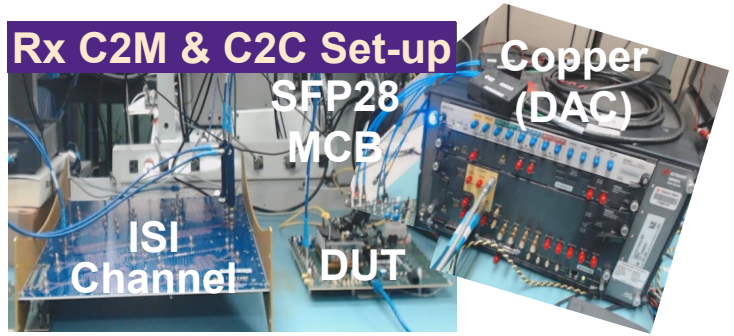
Tx Test Set-up



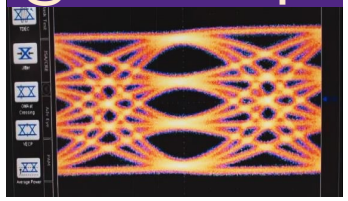
Rx Backplane Set-up



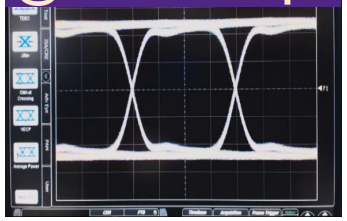
Rx C2M & C2C Set-up

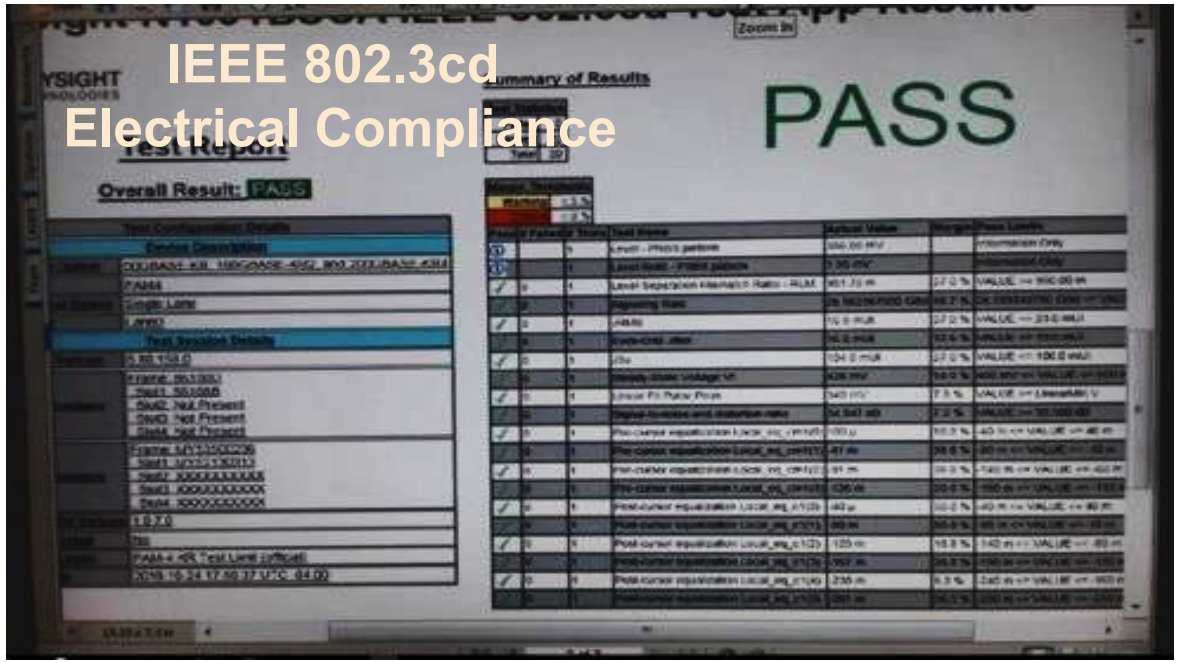


PAM-4 Eye @ 53.125 Gbps



NRZ Eye @10.3125 Gbps





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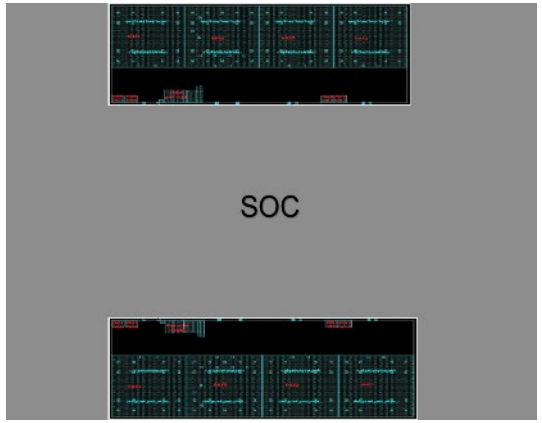
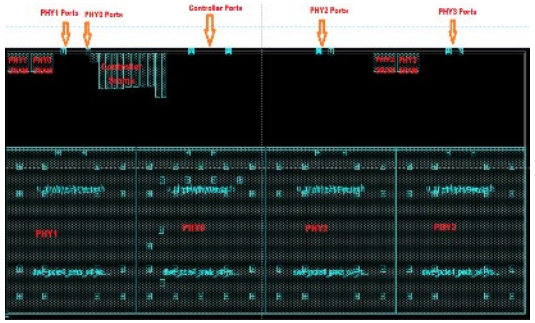
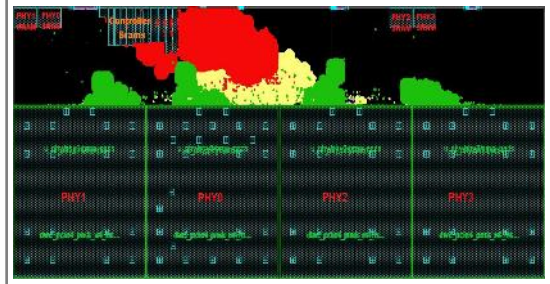
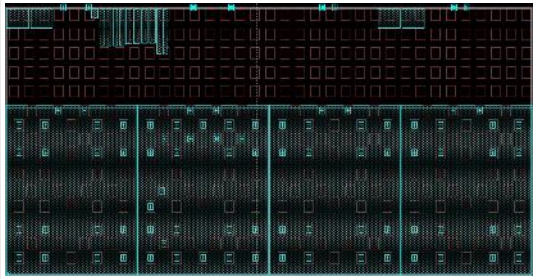
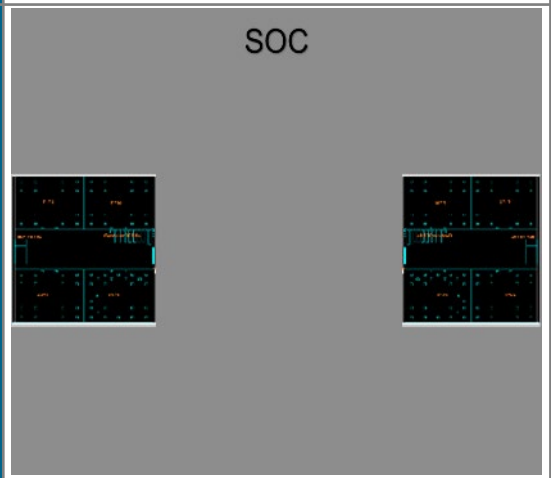
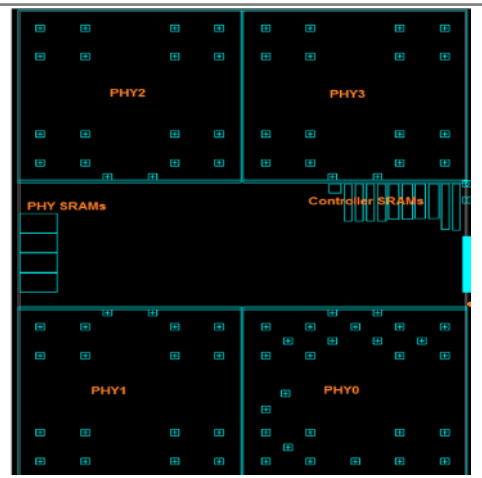
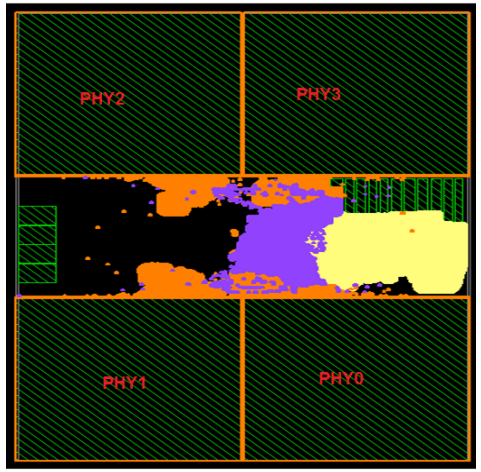
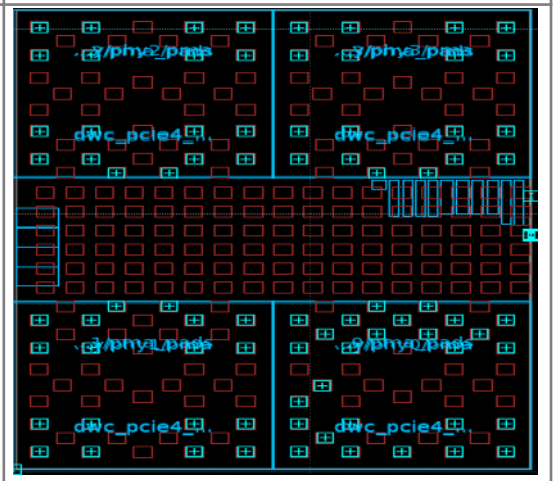
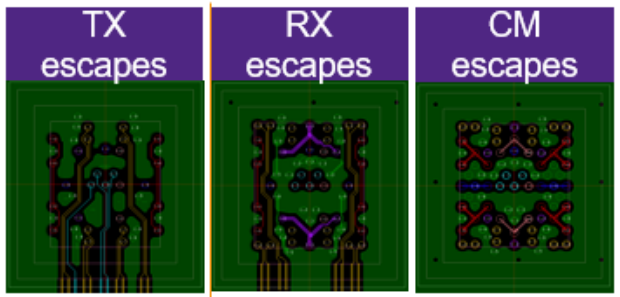
DesignWare 56G PHY Integration

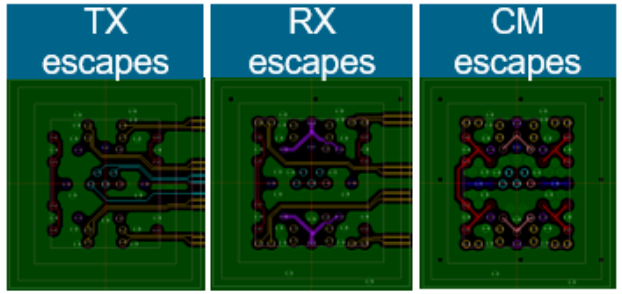
	Placement	Floor Plan	Hierarchy	Bumps
North-South (N/S)				
East-West (E/W)				

DesignWare 56G PHY Package Study

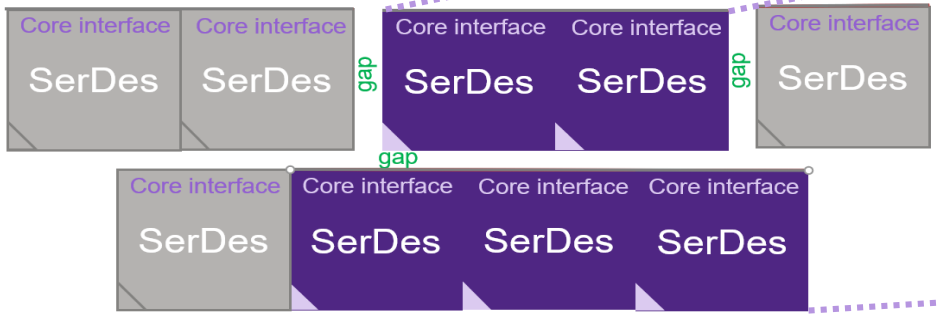
Escape Route & Substrate Routing

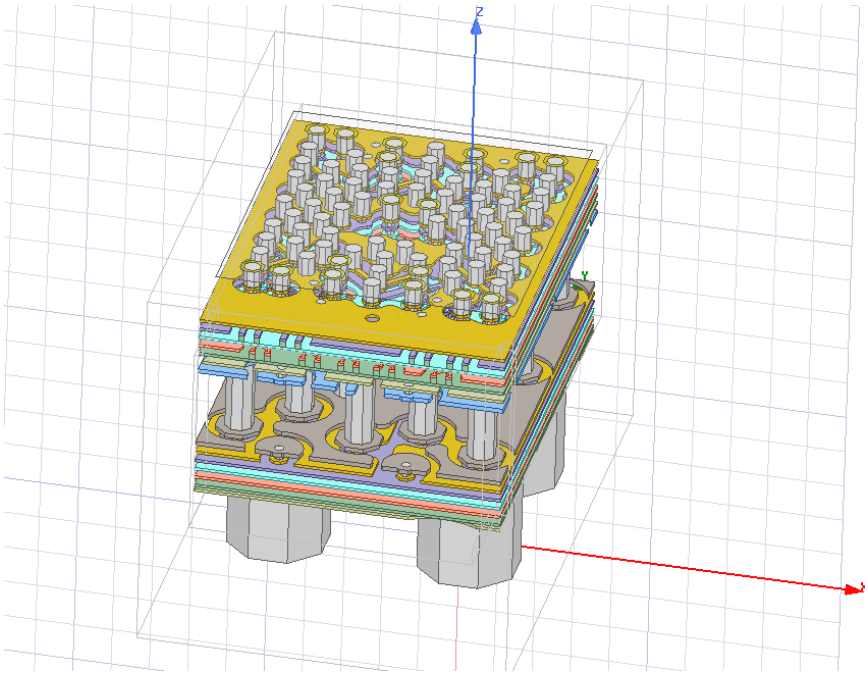


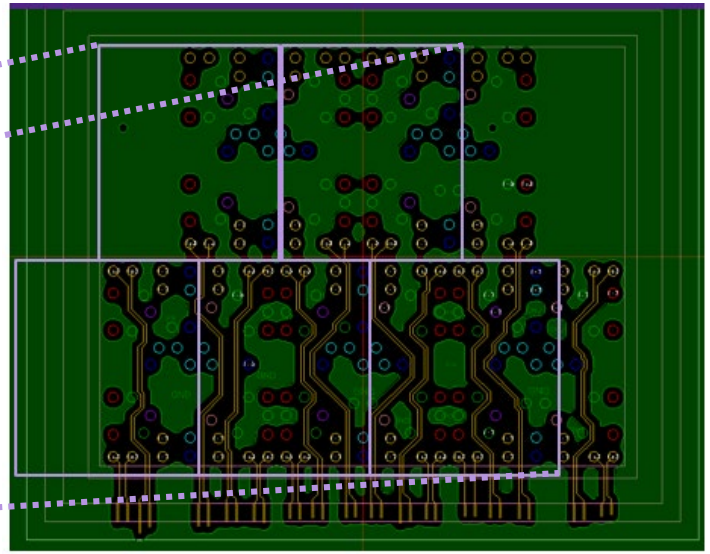
N/S Package Escape



E/W Package Escape



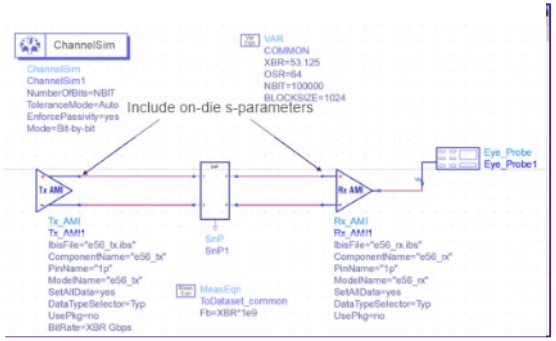


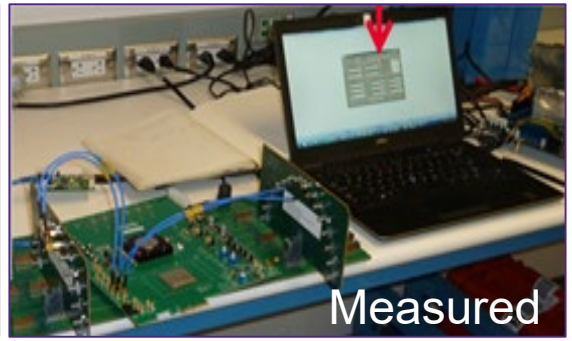


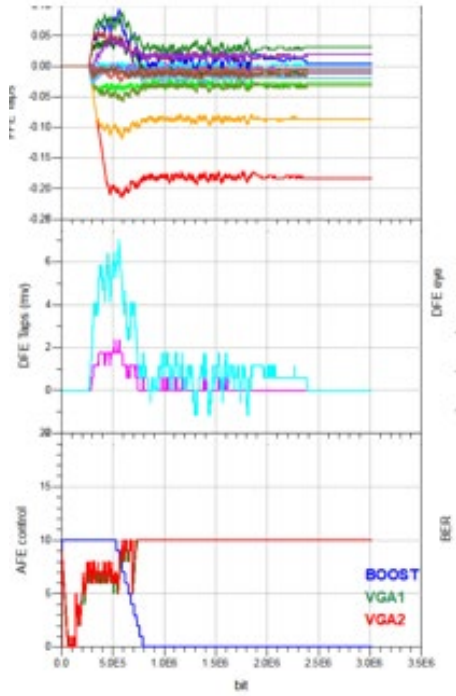
DesignWare 56G PHY IBIS-AMI Models

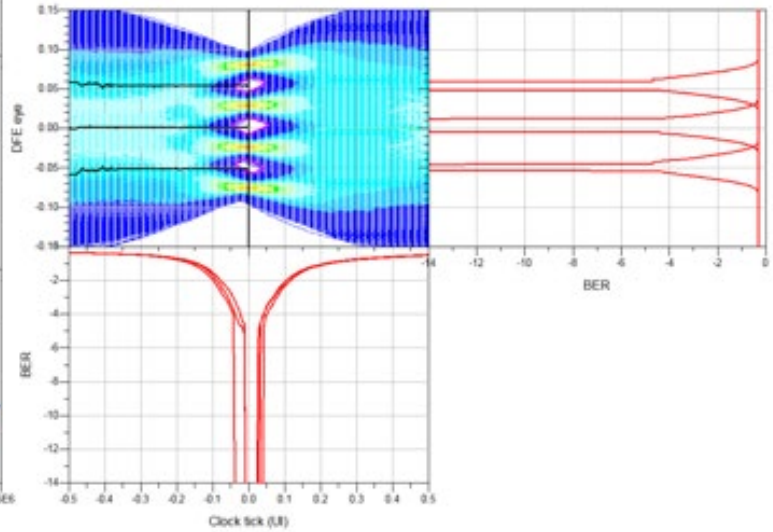
Silicon Correlated Models for Accurate SI Analysis

- Model elements to match architecture & implementation (including adaptation algorithms)
- Model tuned with information from hardware characterization data
- Correlated with silicon characterization for accurate analysis
- Verify models with different AMI simulators - Keysight-ADS, SiSoft-QCD and HSPICE





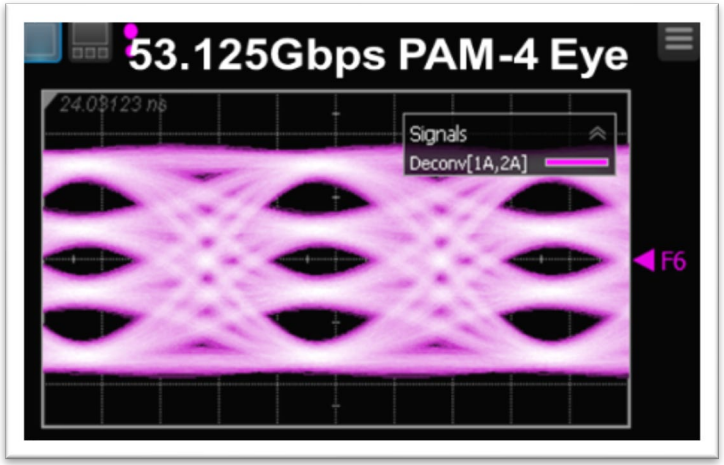




DesignWare 56G Ethernet PHY IP

For Next-Generation 400G Hyperscale Data Centers

- Available in advanced process technologies (16-nm to 7-nm FinFET)
- Supports all OIF & IEEE 802.3 Ethernet-based channel types
  - Backplane, copper cables (DAC) and optical links
  - Backward compatible with NRZ data rates
- Delivers high performance, >35dB @ 14GHz PAM-4 Nyquist
- Digital (AFE + ADC + DSP) based receiver with power-performance knobs
- Robust performance over Voltage & Temperature (VT) corners
- Scalable architecture to 112 Gbps



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