Enabling 400G Networking with 56G Ethernet PHY IP

D&R IP SoC Days

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April 9, 2019
Agenda

• Next-Generation Data Centers
• Multi-Level Modulation
• 56G Ethernet PHY
• High-Speed Ethernet PHY Integration
Enterprise Growth

Flexible & cost effective Scalability

• Horizontal Scaling (a.k.a. scaling out)
  - Additional processing & storage
  - Larger housing area
  - Increased IT management & cooling cost

• Vertical Scaling (a.k.a. scaling up)
  - Upgraded hardware
  - Potential availability constraints
  - More expensive equipment
  - Ease of control

Data Center

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Facebook Hyperscale Data Center

1.5 Million Square Feet on a 325 Acres (Virginia, US)
Hyperscale Data Center 100GE Interconnects
Intra-Rack, Inter-Rack, Co-Location & Regional

- 100G Regional
- 50G / 100G Colocation
- 25G / 50G / 100G Inter-rack
- 25G Intra-rack

Leaf Switch

Spine Switch

Building 1 DC1

DC2

DC3

DC4

DC5

DC6

Leaf Switches
Hyperscale Data Center 400GE Interconnects
Intra-Rack, Inter-Rack, Co-Location & Regional

- 400G Regional
- 200G / 400G Colocation
- 100G / 200G / 400G Inter-rack
- 50G Intra-rack
Agenda

- Next-Generation Data Centers
- Multi-Level Modulation
- 56G Ethernet PHY
- High-Speed Ethernet PHY Integration
Multi-Level Signaling vs. Binary Modulation

PAM-4 (4-Level Pulse Amplitude Modulation) vs. NRZ (Non Return to Zero)

- **PAM-4**
  - 00=0 (01=1)
  - 10=3
  - 11=2

- **NRZ**
  - **#1**
    - 0 0
    - 1 1 0
  - **#2**
    - 0
    - 1 1 0 0

Amplitude Levels

- 00=0
- 01=1
- 10=3
- 11=2

Symbol
Channel Impairment Impact

PAM-4 vs. NRZ

• Additional voltage levels reduce the eye height by a factor of 3 in PAM-4
  – Signal-to-noise ratio (SNR) degrades

• TX output eye width $\Rightarrow 1/2$ to $2/3$ of NRZ
  – Middle eye is the most symmetrical
  – Top and bottom eyes do not match the middle eye

• Impairments impact each eye differently

• Nonlinearity can significantly impact bit error rate

• Crosstalk and reflection have greater signal degradation impact
Shift From NRZ To PAM-4

50GBASE-KR Channel Insertion loss

56G PAM-4
- 33.35dB @ 14.0GHz

56G NRZ
- 62dB @ 28.0GHz
Data Center Interconnects @ 100GE ➔ 400GE

As speeds go up, technology requirements migrate down, and channels shrink.

### Connection Area

<table>
<thead>
<tr>
<th>Regions (Data center-to-data center)</th>
<th>Medium Type</th>
<th>100GE (25G / 50G / 100G)</th>
<th>400GE (50 G / 10G / 200G / 400G)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Colocation (Building-to-building)</td>
<td>Optical</td>
<td>40km SMF</td>
<td>10km SMF</td>
</tr>
<tr>
<td>Room-to-room</td>
<td></td>
<td>10km SMF</td>
<td>2km SMF</td>
</tr>
<tr>
<td>Intra-rack (Rack-to-rack)</td>
<td></td>
<td>100m MMF</td>
<td>500m SMF</td>
</tr>
<tr>
<td>Inter-rack (within the rack)</td>
<td>Copper -- cable</td>
<td>5m DAC, Twin-axial</td>
<td>3m DAC, Twin-axial</td>
</tr>
<tr>
<td>Intra-server</td>
<td>Copper PCB/mezzanine/backplanes</td>
<td>35dB @12.89GHz</td>
<td>30dB @13.28125GHz</td>
</tr>
</tbody>
</table>

**Single Mode Fiber (SMF), Multi Mode Fiber (MMF), Active Optical Cable (AOC), Direct Attached Cable (DAC)**
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Major Types of PAM-4 Designs

Analog vs. Digital Receiver Architecture

### Analog Receiver
- CTLE+VGA
- Analog FFE
- DFE

#### Analog Receiver Details
- Similar to NRZ receiver design
- PVT variation concern
- Technology scalability
- DFE taps (area + power)
- Ideal for short channels
- Power advantage

### Digital Receiver
- CTLE+VGA
- Analog FFE
- ADC
- DSP (FFE+DFE)

#### Digital Receiver Details
- Complex architecture
- Flexibility in process scaling
- More capable signal processing techniques
- Ideal for broad range of channels
- Power disadvantage
### IEEE802.3 Standards for Single & Multiple Channel

802.3bs (200G & 400G) & 802.3cd (50G, 100G, 200G, 400G) @ 53.125 Gbps

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Description</th>
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<tr>
<td>50GAUI-1</td>
<td>Chip-to-chip &amp; Chip-to-module</td>
</tr>
<tr>
<td>100GAUI-2</td>
<td>Chip</td>
</tr>
<tr>
<td>200GAUI-4</td>
<td>Chip</td>
</tr>
<tr>
<td>400GAUI-8</td>
<td>Module</td>
</tr>
<tr>
<td>50GBASE-CR</td>
<td>1-, 2- or 4-lane shielded balanced Twinaxial copper cabling (CR), 2 m &amp; 3 m</td>
</tr>
<tr>
<td>100GBASE-CR2</td>
<td>Chip</td>
</tr>
<tr>
<td>200GBASE-CR4</td>
<td>Chip</td>
</tr>
<tr>
<td>50GBASE-KR</td>
<td>1-, 2- or 4-lane Electrical backplane (KR)</td>
</tr>
<tr>
<td>100GBASE-KR2</td>
<td>Chip</td>
</tr>
<tr>
<td>200GBASE-KR4</td>
<td>Chip</td>
</tr>
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</table>

Single & aggregated link rates of up to 400 Gbps
DesignWare 56G Ethernet PHY IP
For Next-Generation 400G Hyperscale Data Centers

Tx Test Set-up
DUT

Rx Backplane Set-up
ISI Channel
DUT

Rx C2M & C2C Set-up
SFP28 MCB
DUT

Copper (DAC)

PAM-4 Eye
@ 53.125 Gbps

NRZ Eye
@ 10.3125 Gbps

IEEE 802.3cd Electrical Compliance

PASS
Agenda

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## DesignWare 56G PHY Integration

<table>
<thead>
<tr>
<th></th>
<th>Placement</th>
<th>Floor Plan</th>
<th>Hierarchy</th>
<th>Bumps</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>North-South (N/S)</strong></td>
<td><img src="image1" alt="North-South Placement" /></td>
<td><img src="image2" alt="North-South Floor Plan" /></td>
<td><img src="image3" alt="North-South Hierarchy" /></td>
<td><img src="image4" alt="North-South Bumps" /></td>
</tr>
<tr>
<td>SOC</td>
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<tr>
<td><strong>East-West (E/W)</strong></td>
<td><img src="image5" alt="East-West Placement" /></td>
<td><img src="image6" alt="East-West Floor Plan" /></td>
<td><img src="image7" alt="East-West Hierarchy" /></td>
<td><img src="image8" alt="East-West Bumps" /></td>
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DesignWare 56G PHY Package Study
Escape Route & Substrate Routing

N/S Package Escape
E/W Package Escape

die edge
DesignWare 56G PHY IBIS-AMI Models

Silicon Correlated Models for Accurate SI Analysis

- Model elements to match architecture & implementation (including adaptation algorithms)
- Model tuned with information from hardware characterization data
- Correlated with silicon characterization for accurate analysis
- Verify models with different AMI simulators - Keysight-ADS, SiSoft-QCD and HSPICE
DesignWare 56G Ethernet PHY IP

For Next-Generation 400G Hyperscale Data Centers

- Available in advanced process technologies (16-nm to 7-nm FinFET)
- Supports all OIF & IEEE 802.3 Ethernet-based channel types
  - Backplane, copper cables (DAC) and optical links
  - Backward compatible with NRZ data rates
- Delivers high performance, >35dB @ 14GHz PAM-4 Nyquist
- Digital (AFE + ADC + DSP) based receiver with power-performance knobs
- Robust performance over Voltage & Temperature (VT) corners
- Scalable architecture to 112 Gbps
Thank You

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