Sowmyan Rajagopalan, Founder & CTO
Thalia Design Automation

Is efficient Analog IP reuse a Myth?
An Innovative Approach to make Analog IP reuse a reality

April, 2019
Analog IP Reuse – Why is it difficult?

• Analog circuit design is impacted by a number of factors
  • Device performance,
  • Technology characteristics,
  • Functional requirements,
  • Design methodology

• Migrating an Analog circuit into a new technology is almost a redesign of an existing IP – custom requirements
  • Even a bandgap requires design redo !!!

• Limited solutions in the market and a shortage of analog designers exacerbates the problem

• Is efficient Analog IP reuse a dream?
Thalia at a glance

2011
Thalia is founded

2014
Amalia™ Suite Initial release

2015
Solutions Offering launched targeting Analog Reuse
• Experienced Delivery Team
  Established – Avg. 20 years of experience

2016
Several customer designs delivered
• RF Front end, Baseband applications

2017
Thalia established in India

2017
Amalia™ expanded to address several flavors of TSMC, GF, UMC, In-house technologies of Tier1 design companies

2018
Thalia expanded to Germany
Thalia’s target solutions

Through a combination of
Methodology
High Value Design Services
Innovative Technology

Development of Test Methodology
Generation of Test Benches & States

Design Enabler
Performance Improvement

IP Portfolio Generation
Creating flavors of functionality
to address different market requirements

Technology Migration
Migrating Design across technologies

IP On-Demand
Assisting in generation of IPs
Why are we different?

Thalia Unique Approach
- Speed
- Efficiency
- Cost

Thalia Toolsets
- Schematic + Design + Layout
- AI and Algorithms

Thalia Resources
- > 20 Years experience

Thalia Methodology
- Targeted automation

Smart Toolsets
Smart Methodology
Smart Resources
Toolsets Amalia™ Capability

Design Enabling Capability

- Circuit Analyzer
- IP Portfolio Generator
- Circuit Improvement
- Schematic Porting
- AMALIA Suite
- Layout Automation

17 April 2019
Thalia’s Analog Porting Flow

**Origin Design**
- Test Bench
- Schematic
- Layout

**Ported Design**
- AMALIA Automated Schematic Porting
- Ported Test Bench
- Ported Schematic
- Initial Ported Layout
- New layers and PCELLs

**Target PDK**
- Symbols, Models, Libraries
- Design Analysis and Centering - Nominal and PVT
- AMALIA + Design Expertise
- Optimised Device Sizes
- Updated device sizes
- Ported Layout

**Experienced Designers & Automation**

Thalia Design Automation Ltd
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Design Example – PLL Application in Wi-Fi Migration

Top Level Specifications
1. Ref Frequency=40MHz
2. VCO Out Freq=3.2G -4GHz
3. Reference spur <-50dBc
4. Programmable divider
5. Power consumption: 3mA

Others: PD & MMD = -9dB => -12dB each
@160 MHz: -12 dB => -40-12-31 = -83dBc
<table>
<thead>
<tr>
<th>VCO (LC based)</th>
<th>Programmable Feedback divider</th>
<th>Phase Frequency Detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centre frequency</td>
<td>3.86GHz</td>
<td>Operating frequency</td>
</tr>
<tr>
<td>Current consumption</td>
<td>1.5mA</td>
<td>Current consumption</td>
</tr>
<tr>
<td>Tuning range with band selection</td>
<td>3GHz-4GHz</td>
<td>Output swing</td>
</tr>
<tr>
<td>Phase noise</td>
<td>-120dBc/Hz @1MHz offset</td>
<td>Charge Pump</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Schedule

Loop stability, Parasitics etc

Topology

Technology Differences
Design Example: Clk PLL – Thalia’s Solution

- Targeted automation to provide incremental time and cost savings – full automation doesn’t work in Analog
Design Example: CLK PLL – Migration Results
## Business Value: Analog Migration

- **Ref Frequency=40MHz**
- **Clock output : 2.88GHz**
- **VCO phase noise =-121dBc/Hz @1MHZ.**
- **Programmable loop filter AND Programmable divider.**
- **EVM for Integrated PHASE NOISE @160MHZ should be better than -42dB.**
- **Ref spur =-90dB**
- **TSMC to GF 28nm**
- **Migrated, Design changes and layout in < 6-7 weeks**

### Functional Requirements
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Verified Specification</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL comparison frequency</td>
<td>Same as the XO frequency</td>
<td>40</td>
<td>40</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Output frequencies to the LB and HB PLL’s (low noise)</td>
<td>To frequency counter</td>
<td>160</td>
<td>160</td>
<td></td>
<td>MHz</td>
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<tr>
<td>Other output frequencies</td>
<td>To frequency counter</td>
<td>160</td>
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<td>?</td>
<td>-42.9</td>
<td>-43.6</td>
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### Design

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Solutions delivered by Thalia

Unique combination of Experienced Resources and Innovative Technologies

<table>
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<tr>
<th>Application</th>
<th>Technologies</th>
<th>Nodes</th>
</tr>
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<tbody>
<tr>
<td>Dual Band WIFI</td>
<td>TSMC, GF, Samsung</td>
<td>22nm, 28nm, 40nm, 28nm FDSOI</td>
</tr>
<tr>
<td>Bluetooth IP</td>
<td>TSMC, GF, Samsung</td>
<td>28nm, 40nm 28nm FDSOI</td>
</tr>
<tr>
<td>ADCs, PLLs, LNAs, PAs</td>
<td>TSMC, GF, Tier 1 In-house technologies, SMIC</td>
<td>16FF to 130nm</td>
</tr>
<tr>
<td>PMIC Derivatives</td>
<td>TSMC, GF, UMC, AMS</td>
<td>16FF to 350nm</td>
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Wide range of Technologies and nodes from 350nm down to 16FF nm
Proven Track Record delivering designs in cutting edge applications and in newest technologies
# Rapid Analog Porting - Reuse Customer Examples

<table>
<thead>
<tr>
<th>Classification</th>
<th>Examples</th>
<th>Redesign Cycle Time*</th>
<th>Thalia’s Cycle Time*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Analog IP</td>
<td>DAC, ADC, PLL</td>
<td>12-16 weeks [2-3 FTE]**</td>
<td>4-8 weeks [2 FTE]**</td>
</tr>
<tr>
<td>Application Analog IP</td>
<td>Bluetooth, GPS/GLONASS</td>
<td>&gt;40-50 weeks [~ 6-8 FTE]**</td>
<td>18-22 weeks [~ 6-7 FTE]**</td>
</tr>
<tr>
<td>Application Analog IP</td>
<td>Dual Band WLAN</td>
<td>&gt;50 weeks [~ 6-8 FTE]**</td>
<td>22-28 weeks [~ 6-7 FTE]**</td>
</tr>
</tbody>
</table>

(*) Elapsed calendar time to Specification Compliant Design
(**) FTE : Full Time Equivalent
Timescales will be impacted by Circuit complexity and process node differences
Customer Testimonial

Kave Kianush, Catena Vice President and Chief Technology Officer

“We’re taking a new approach, which represents a fundamental shift in the way analog IP is created and delivered.

Our relationship with Thalia helps us to deliver exactly the right feature and performance combination for our customers, against ever more demanding time-to-market and cost requirements.

Thalia’s combination of novel design automation technology and analog design expertise is unique in the market.

We’ve already seen a positive impact on our ability to deliver against tight customer deadlines.”

Summary: Re-inventing Analog Reuse

- Unique combination of toolsets, methodology and design experience
- Proven track record – 16 FF to 350nm; TSMC, UMC, GF, Tower, SMIC, AMS, Tier 1 Technologies
- Direct application in migrating IPs – Off the shelf IPs

- Contact us sales@thalia-da.com