Sowmyan Rajagopalan, Founder & CTO
Thalia Design Automation

Is efficient Analog IP reuse a Myth ?
An Innovative Approach to make Analog IP reuse a reality

April, 2019

Thalia Design Automation

Analog IP Reuse – Why is it difficult ?

- Analog circuit design is impacted by a number of factors
  - Device performance,
  - Technology characteristics,
  - Functional requirements,
  - Design methodology
- Migrating an Analog circuit into a new technology is almost a redesign of an existing IP – custom requirements
  - Even a bandgap requires design redo !!!
- Limited solutions in the market and a shortage of analog designers exacerbates the problem

- Is efficient Analog IP reuse a dream?

Thalia at a glance

2011

Thalia is founded

2014

Amalia™ Suite Initial release

2015

Solutions Offering launched targeting Analog Reuse

- Experienced Delivery Team Established – Avg. 20 years of experience

2016

Several customer designs delivered

- RF Front end, Baseband applications

2017

Thalia established in India

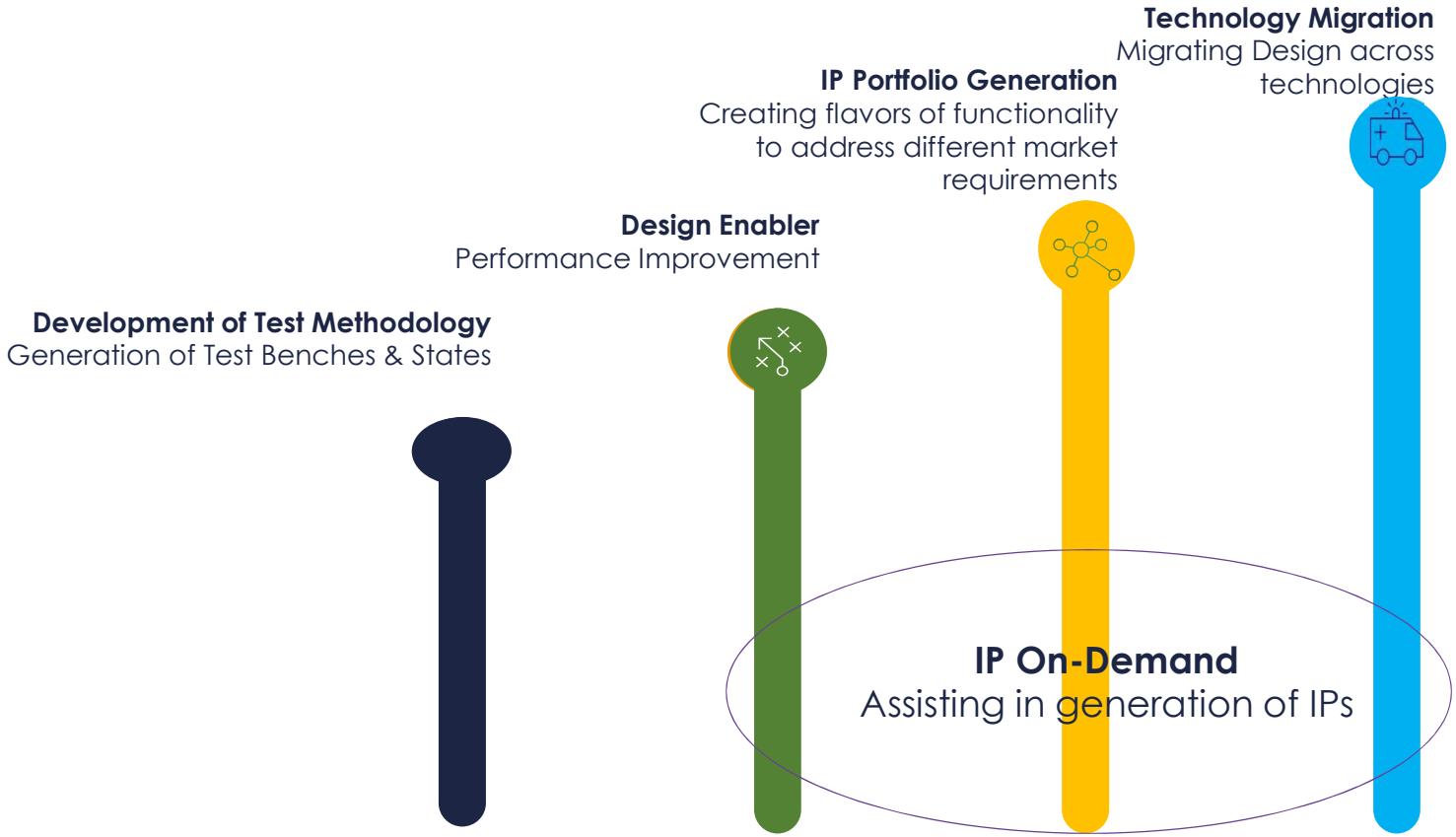
2017

Amalia™ expanded to address several flavors of TSMC, GF, UMC, In-house technologies of Tier1 design companies

2018

Thalia expanded to Germany

Thalia's target solutions



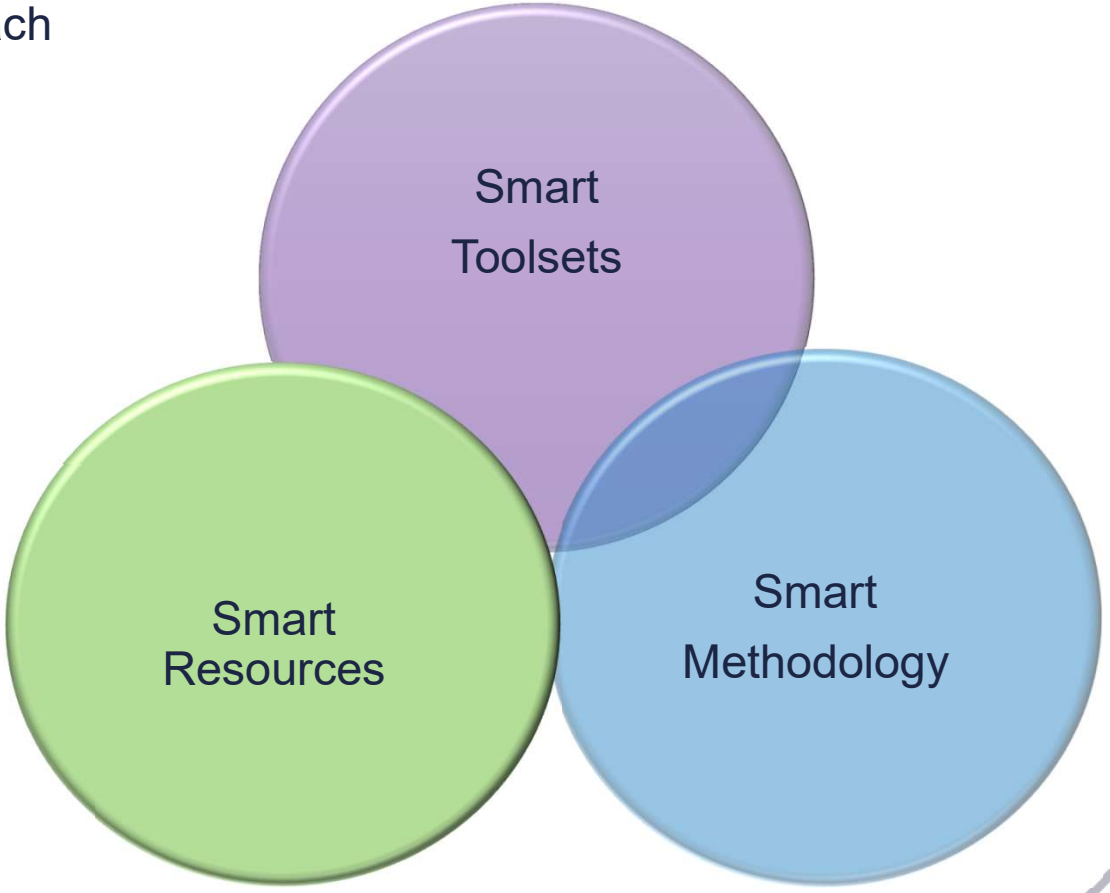
Through a combination of

Methodology
High Value Design Services
Innovative Technology

Why are we different?

Thalia Unique Approach

- **Speed**
- **Efficiency**
- **Cost**



Thalia Toolsets

- **Schematic + Design + Layout**
- **AI and Algorithms**

Thalia Resources

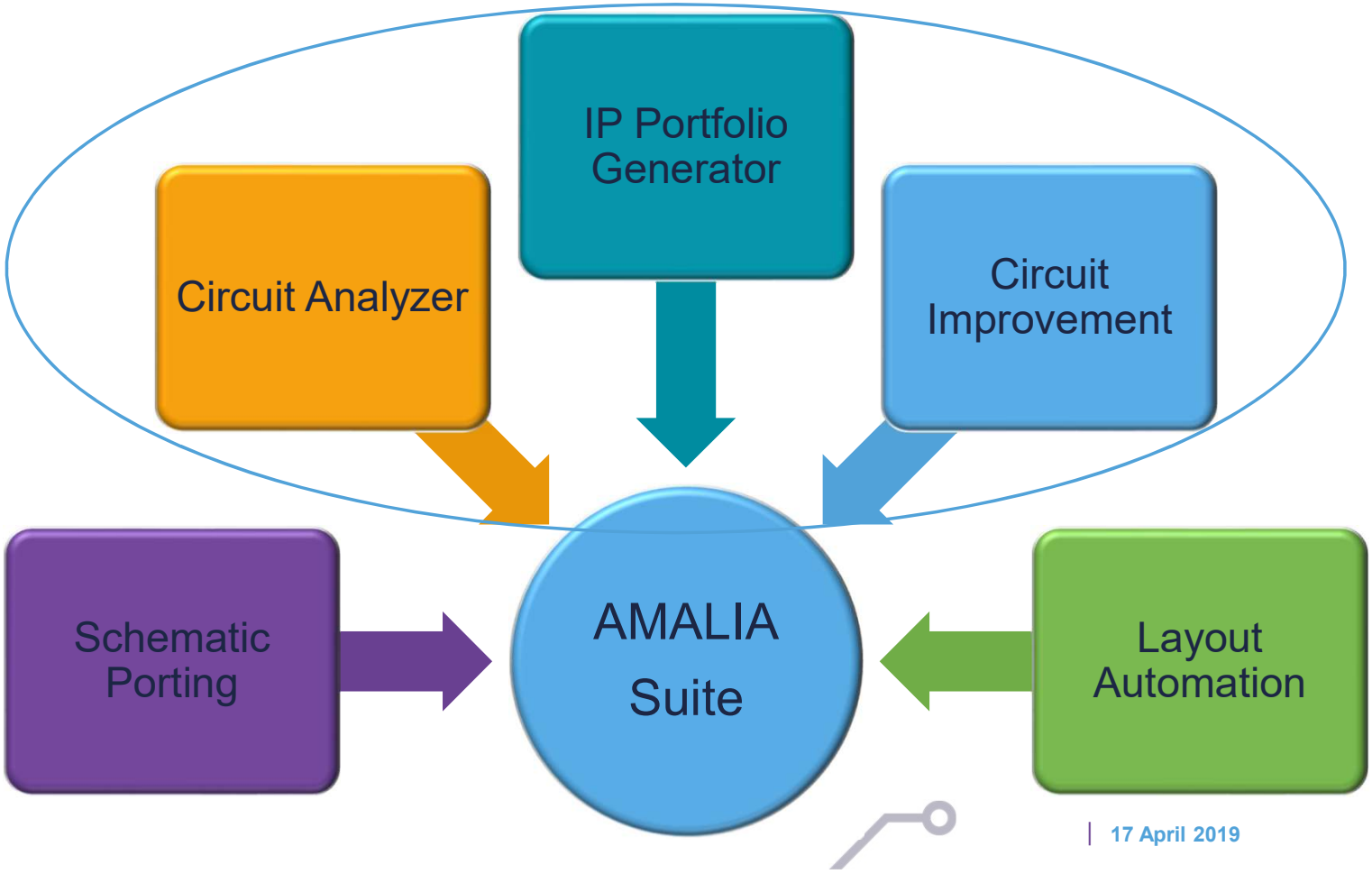
- **> 20 Years experience**

Thalia Methodology

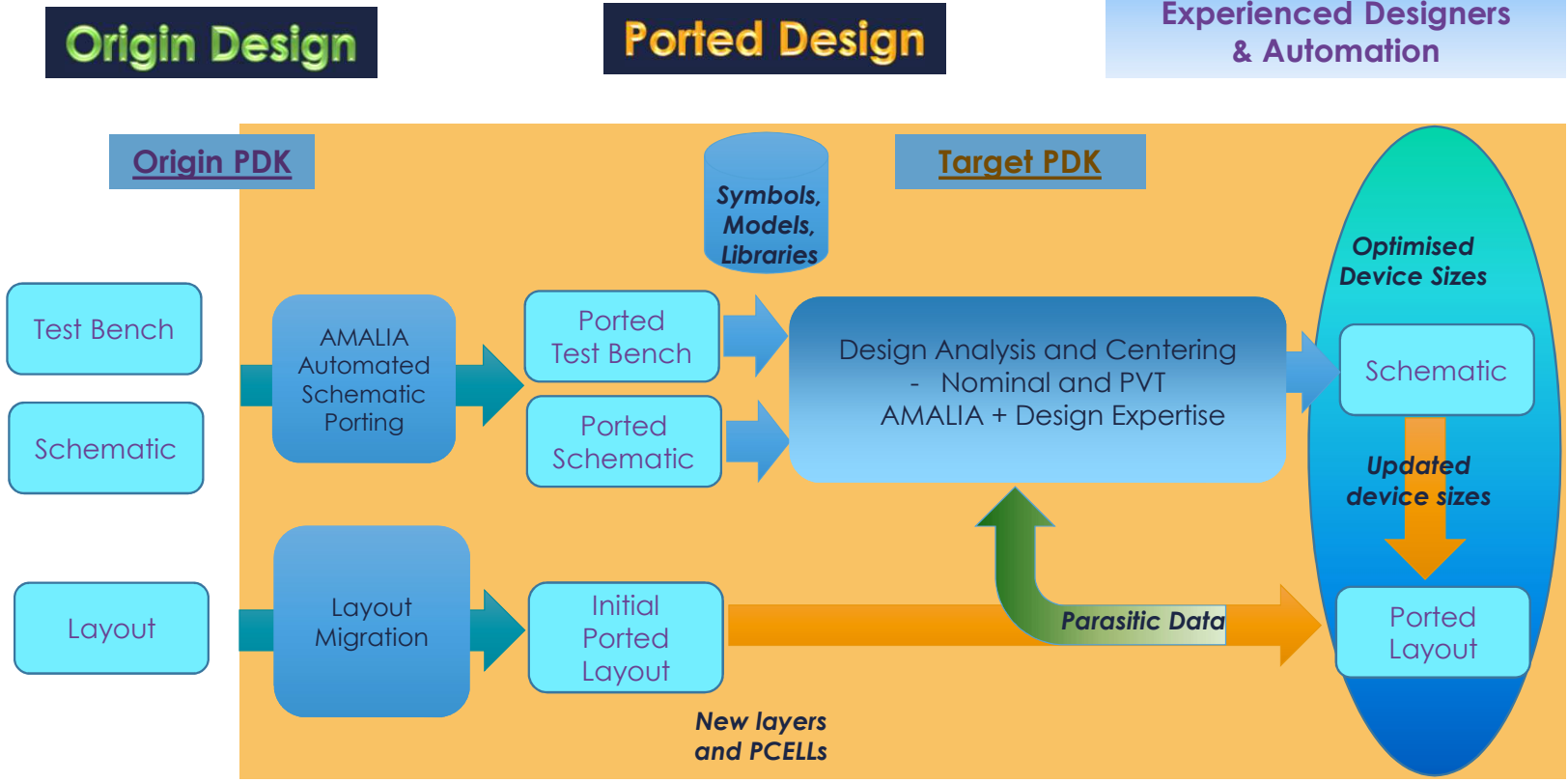
- **Targeted automation**

Toolsets Amalia™ Capability

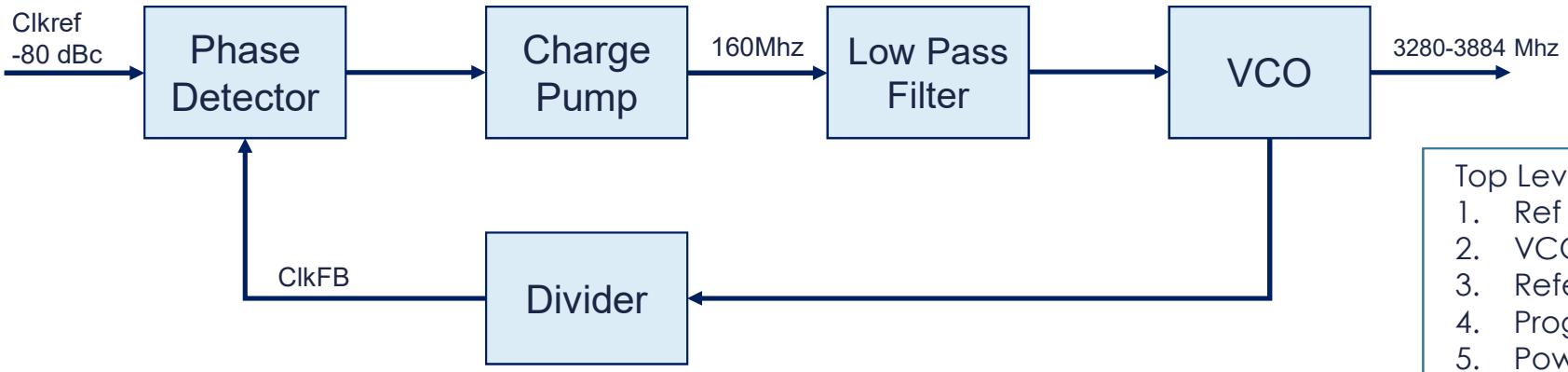
Design Enabling Capability



Thalia's Analog Porting Flow



Design Example – PLL Application in Wi-Fi Migration



Others: PD & MMD = -9dB => -12dB each
@160 MHz: -12 dB => -40-12-31 = -83dBc

Top Level Specifications
1. Ref Frequency=40MHz
2. VCO Out Freq=3.2G -4GHz
3. Reference spur <-50dBc
4. Programmable divider
5. Power consumption: 3mA

The Design Conundrum

VCO(LC based)	
Centre frequency	3.86GHz
Current consumption	1.5mA
Tuning range with band selection	3GHz-4GH
Phase noise	-120dBc/Hz @1MHz offset

Programmable Feedback divider	
Opera… freque…	6.4GHz
Current consumption	1.0mA
Output swing	Rail to

Phase Frequency Detector	
Operating frequency	Up to 160MHz

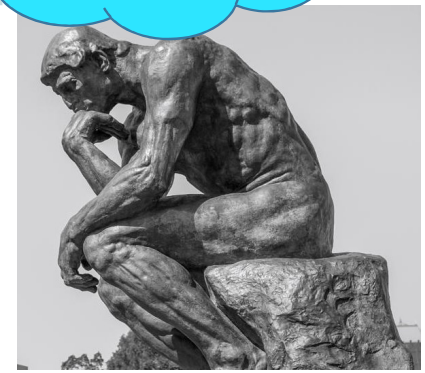
Charge Pump	
Full differential design with 3bits programmability	40uA-200uA

Schedule

Loop stability, Parasitics etc

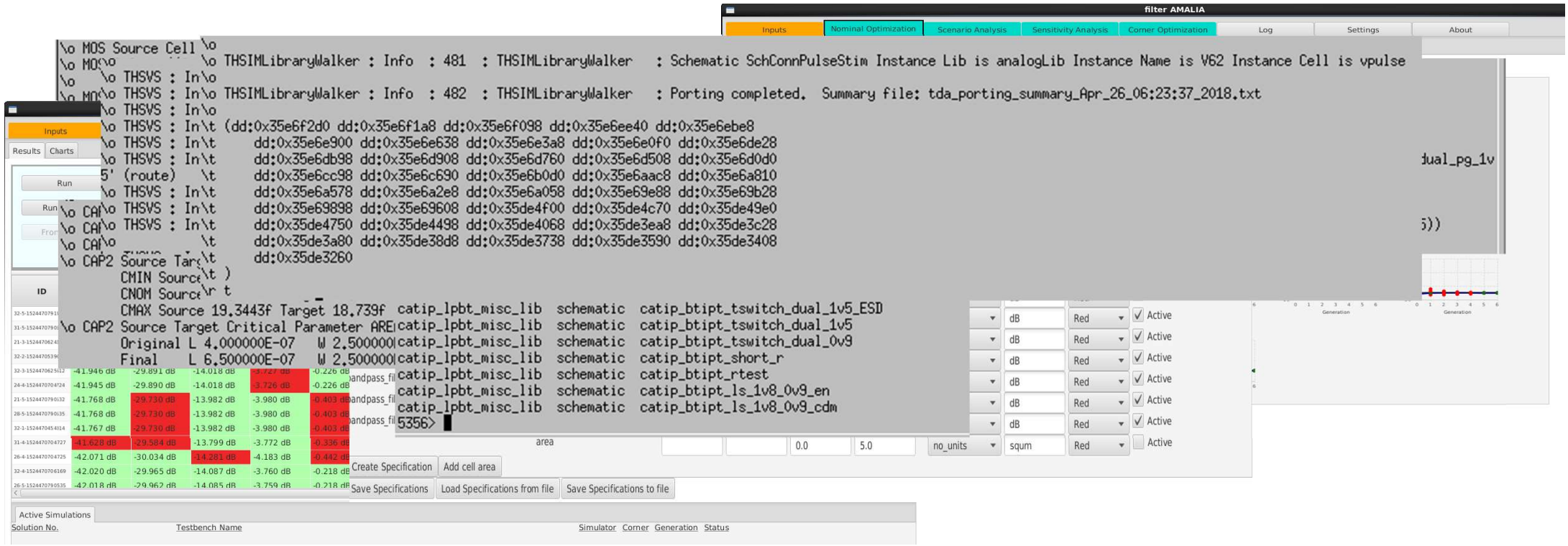
Topology

Technology Differences

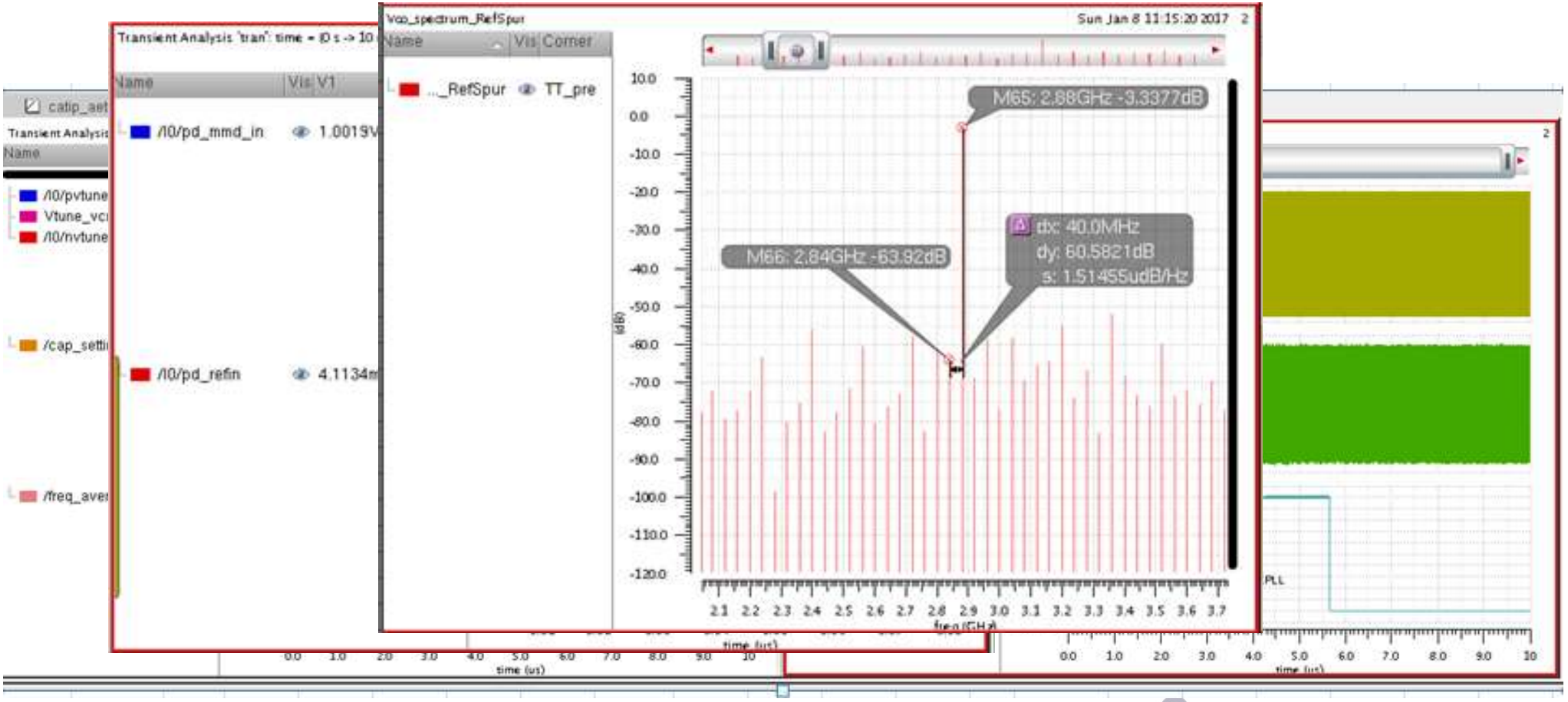


Design Example: Clk PLL – Thalia's Solution

- Targeted automation to provide incremental time and cost savings – full automation doesn't work in Analog



Design Example: CLK PLL – Migration Results



Business Value: Analog Migration

Design	Parameter		Verified Specification			Min	Typ	Max	Units
	Conditions		min	nom	max				
	Functional requirements								
CLK-PLL	PLL comparison frequency	Same as the XO frequency		40			40		MHz
	Output frequencies to the LB and HB PLL:s (low noise)			160			160		MHz
	Other output frequencies	To frequency counter		40			40		MHz
				960			960		MHz
		Test-output		40			40		MHz
		To ADC/DAC		160			160		MHz
	Parametric requirements								
	EVM from Integrated phase noise at the 160MHz output	Integrated from 10kHz to 2MHz and referred to 5.9GHz	?	-42.9			-43.6		dB

- Ref Frequency=40MHz
- Clock output : 2.88GHz
- VCO phase noise =-121dBc/Hz @1MHZ.
- Programmable loop filter AND Programmable divider.
- EVM for Integrated PHASE NOISE @160MHZ should be better than -42dB.
- Ref spur =-90dB
- TSMC to GF 28nm
- Migrated, Design changes and layout in < 6-7 weeks

Thalia
Design Automation

Solutions delivered by Thalia

Unique combination of Experienced Resources and Innovative Technologies

Application	Technologies	Nodes
Dual Band WIFI	TSMC, GF, Samsung	22nm, 28nm, 40nm, 28nm FDSOI
Bluetooth IP	TSMC, GF, Samsung	28nm, 40nm 28nm FDSOI
ADCs, PLLs, LNAs, PAs	TSMC, GF, Tier 1 In-house technologies, SMIC	16FF to 130nm
PMIC Derivatives	TSMC, GF, UMC, AMS	16FF to 350nm

Wide range of Technologies and nodes from 350nm down to 16FF nm
Proven Track Record delivering designs in cutting edge applications and in newest technologies

Thalia Design Automation

Rapid Analog Porting - Reuse Customer Examples

Classification	Examples	Redesign Cycle Time*	Thalia's Cycle Time*
Standard Analog IP	DAC, ADC, PLL	12-16 weeks [2-3 FTE]**	4-8 weeks [2 FTE]**
Application Analog IP	Bluetooth, GPS/GLONASS	>40-50 weeks [~ 6-8 FTE]**	18-22 weeks [~ 6-7 FTE]**
Application Analog IP	Dual Band WLAN	>50 weeks [~ 6-8 FTE]**	22-28 weeks [~ 6-7 FTE]**

(*) Elasped calendar time to Specification Compliant Design
(**) FTE : Full Time Equivalent
Timescales will be impacted by Circuit complexity and process node differences

Customer Testimonial

Kave Kianush, Catena Vice President and Chief Technology Officer

"We're taking a new approach, which represents a fundamental shift in the way analog IP is created and delivered.

Our relationship with Thalia helps us to deliver exactly the right feature and performance combination for our customers, against ever more demanding time-to-market and cost requirements.

Thalia's combination of novel design automation technology and analog design expertise is unique in the market.

We've already seen a positive impact on our ability to deliver against tight customer deadlines."

https://www.thalia-da.com/catena-selects-thalia-da-to-facilitate-analog-ip-re-use/

Summary: Re-inventing Analog Reuse

- Unique combination of toolsets, methodology and design experience
- Proven track record – 16 FF to 350nm; TSMC, UMC, GF, Tower, SMIC, AMS, Tier 1 Technologies
- Direct application in migrating IPs – Off the shelf IPs

- Contact us sales@thalia-da.com