General Description

Analog Bits' PVT Sensor is a highly integrated macro for monitoring process, voltage, and temperature variation on-chip, allowing very high precision even in untrimmed usage. It consumes very little power even in operational mode, and leakage power only when temperature measurement is complete. An additional voltage sample mode is included allowing for supply voltage monitoring, and process monitor mode to assess transistor performance. The block includes a simple-to-use digital interface that works with standard core and IO level power supplies. The macro uses core and thick-oxide devices.

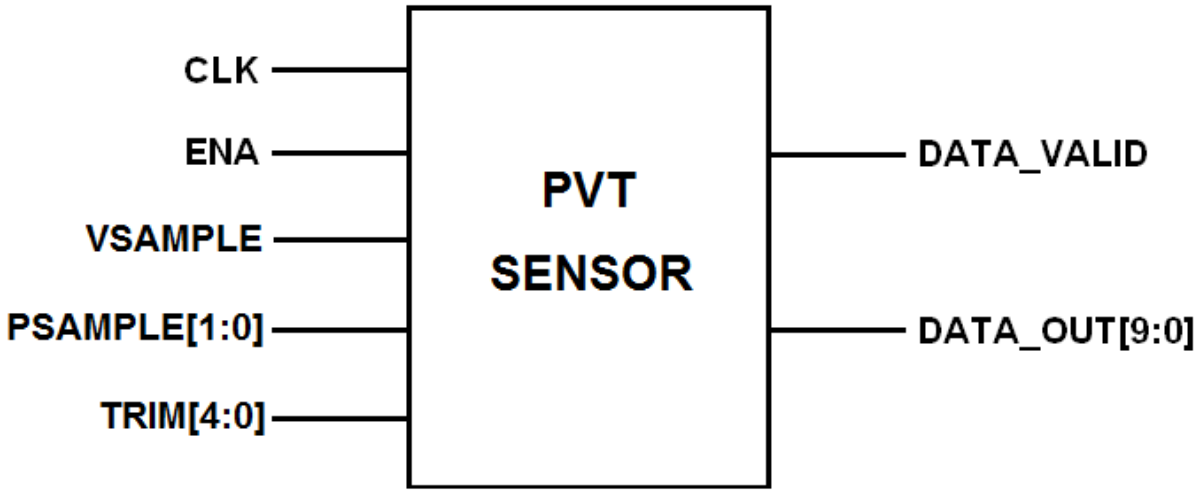
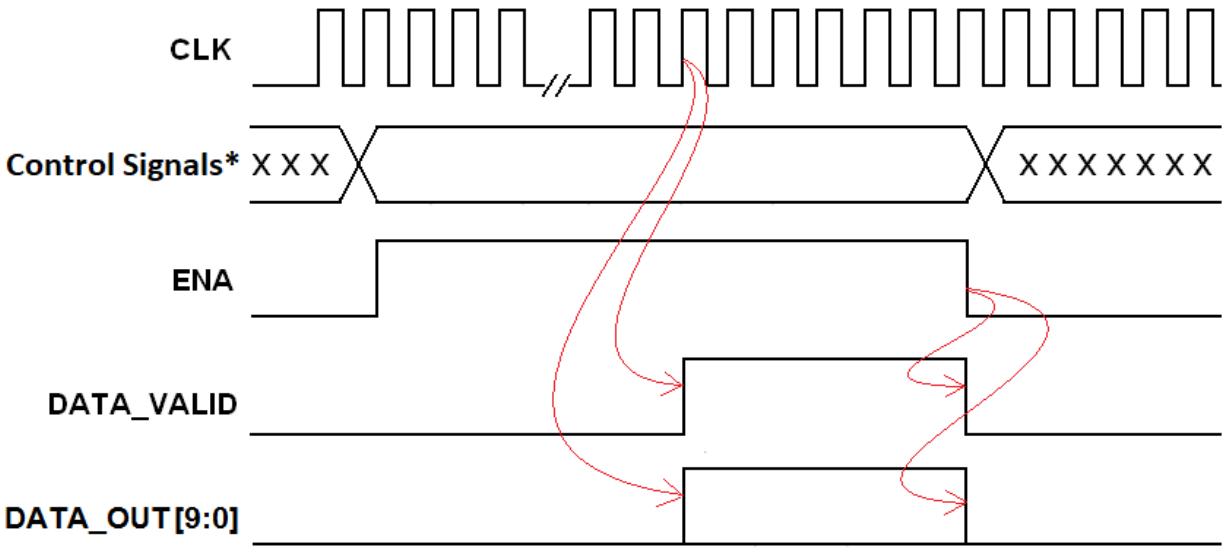


Figure 1: PVT Sensor Block Diagram

Specifications

Description	Units	Min	Typ	Max
Temperature Accuracy (post-trim)	^{o}C		±1	
Temperature Accuracy (untrimmed)	^{o}C		±5	
Voltage Accuracy (±3 σ)	%			±3
Clock Frequency	MHz	1.15		1.25
Sample Rate	Samples/sec			5000
Area	sq.mm		0.05	
Dynamic Power	µA		478	
Operating Voltage (Digital)	V_{DIG}	0.81	0.9	0.99
Operating Voltage (Analog)	V_{ANA}	1.62	1.8	1.98
Operational Temperature	^{o}C	-40	25	125

Table 1: PVT Sensor Specifications



*Control Signals: VSAMPLE, PSAMPLE[1:0], and TRIM[4:0]

Figure 2: Timing Diagram

Pin Description

Pin	Type	Function
CLK	Input	A logic clock to run the digital portion of the temperature sensor. The actual speed is not very critical, and may be divided off of any convenient logic clock.
ENA	Input	A control signal commanding the temperature sensor to re-evaluate the local die temperature (active HIGH)
PSAMPLE[1:0]	Input	Select for Process Sample mode (select between SVT, HVT and LVT devices)
VSAMPLE	Input	Select for Voltage Sample mode (active High)
TRIM[4:0]	Input	Optional programmable inputs which may be used to improve the absolute accuracy of the temperature sensor. The optimal values may be ascertained during test, or at any other time.
DATA_VALID	Output	An output signaling when the temperature sensing is complete, and when the sensor is available to re-assess the temperature.
DATA_OUT[9:0]	Output	A 10-bit bus representing the sensed temperature
Note: All input port pins have antenna diodes		

Table 2: Pin Description

Deliverables and EDA Design Views

Front-end Design Views (with NDA)	Back-end Design Views (with License Agreement)
Verilog Model	GDSII stream file
Synopsys (LIB)	CDL/Spice netlist
Footprint (LEF) format	Application Notes inclusive of design integration guidelines (PDF)
Datasheet (PDF)	

Table 3: List of Deliverables