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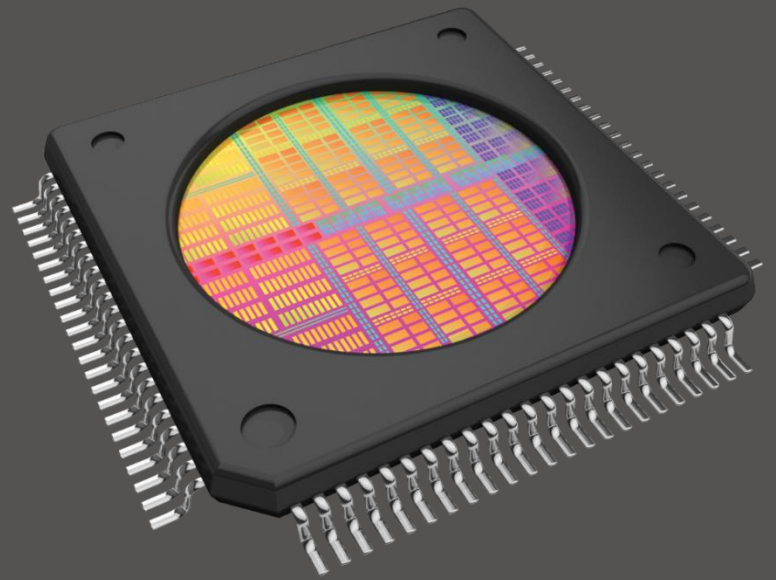
Moortec
Global In-chip Monitoring



Design & Reuse, IP SoC Day
Shanghai 2nd September 2016
Shortform Presentation

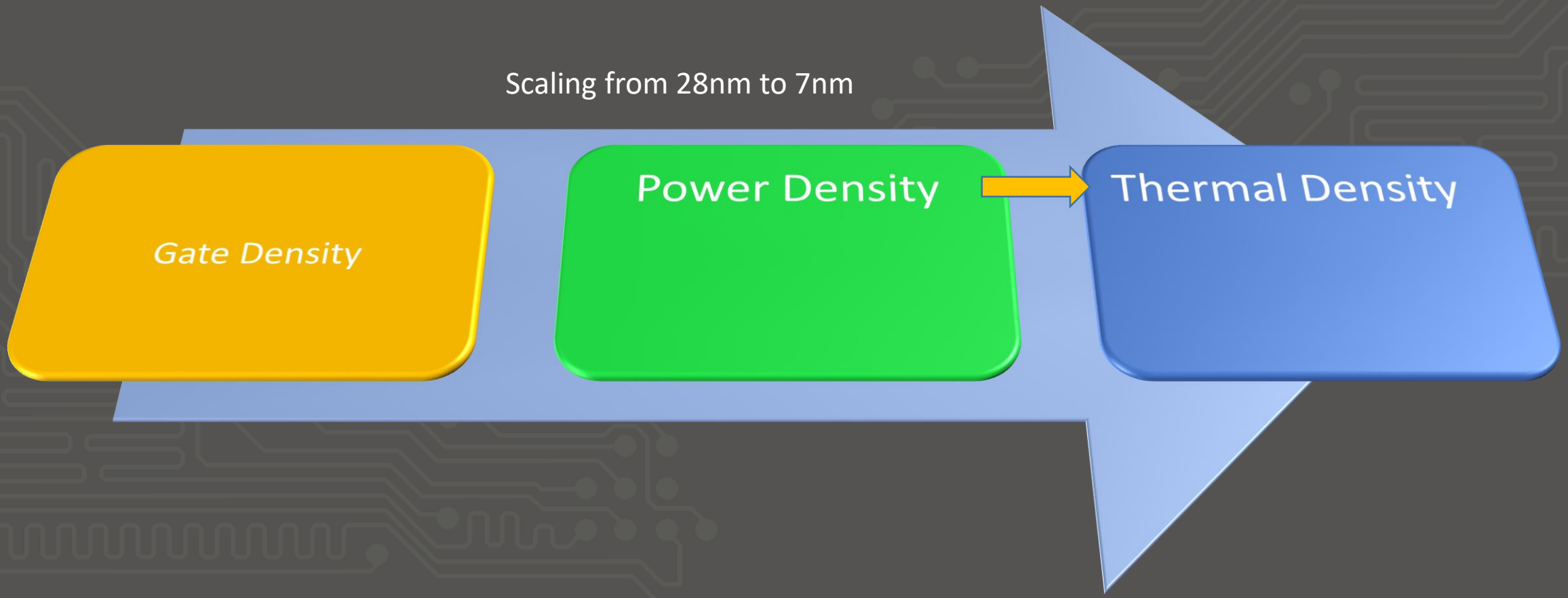
The Challenges Posed by In-Chip Conditions to Reaching Working Silicon

(Presenter: Stephen Crosher)

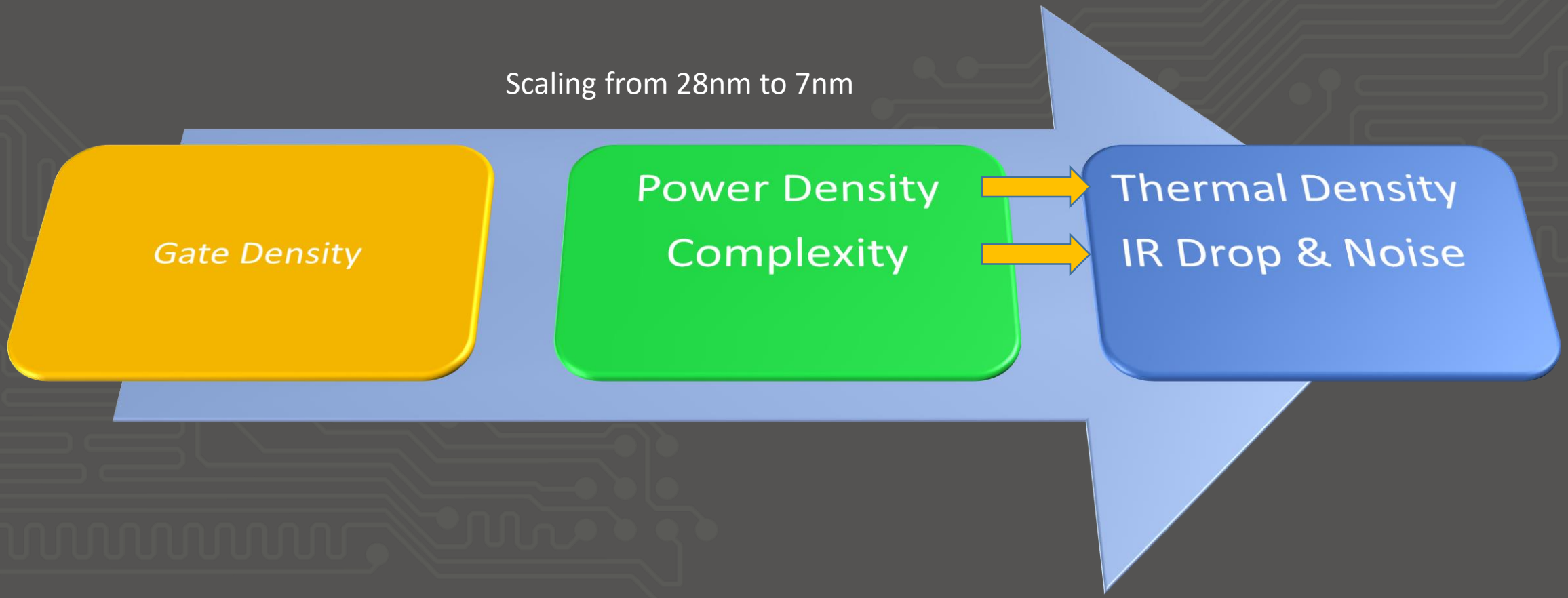
Contact: **+44 1752 875130** Web: **www.moortec.com** Email: **info@moortec.com**

20 mins
11.25am

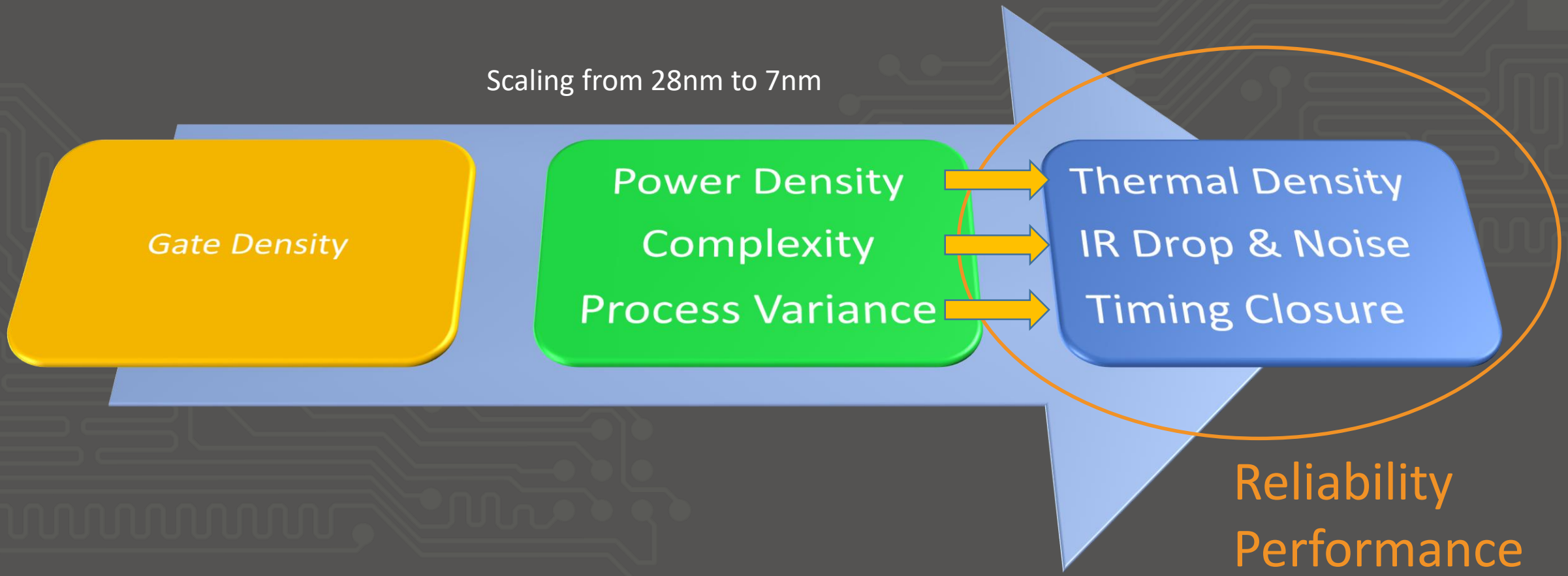
Advanced Node Design



Advanced Node Design



Advanced Node Design

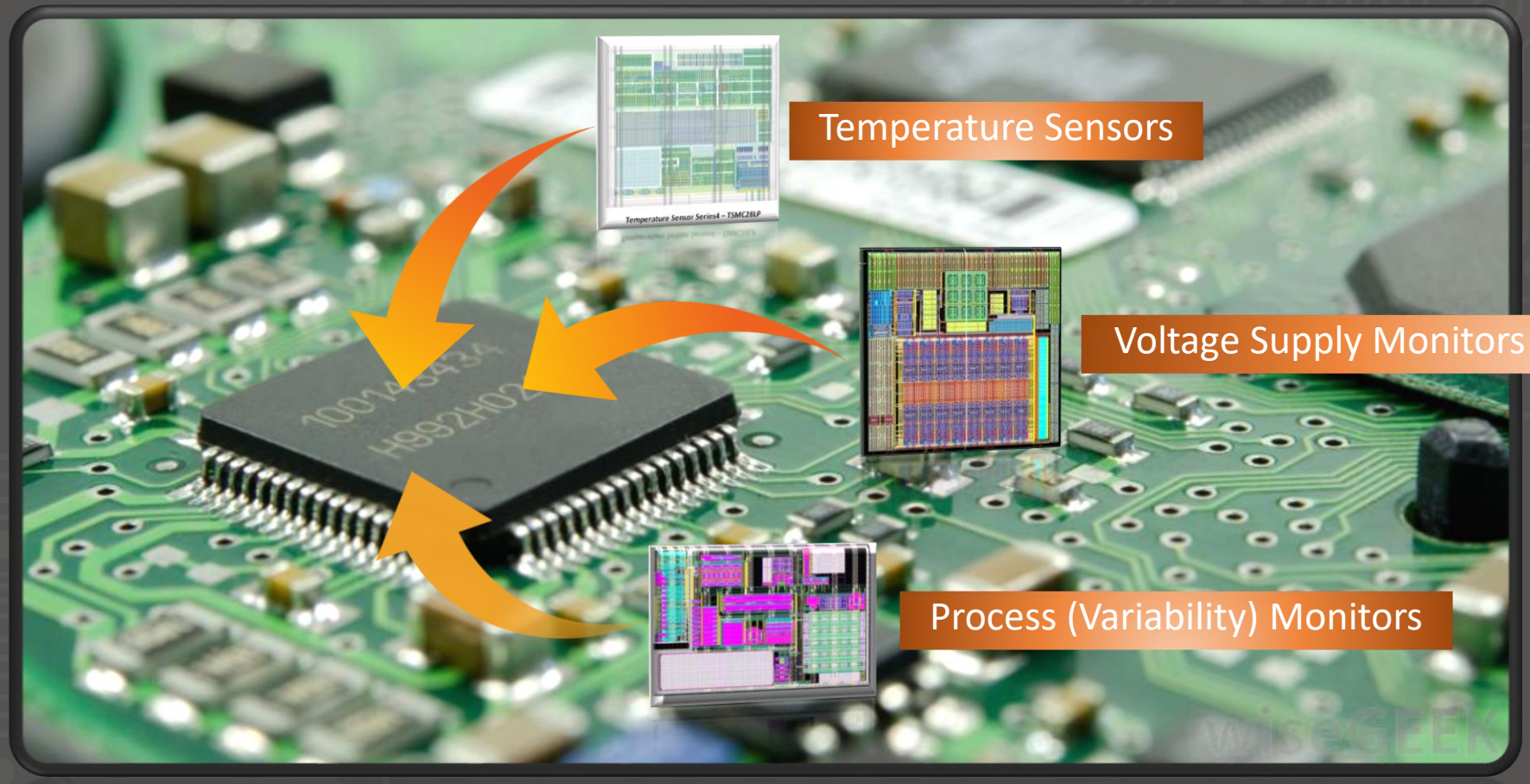


In-Chip Monitoring

Measure

Monitor

Optimise



GLOBAL IN-CHIP MONITORING

Challenges

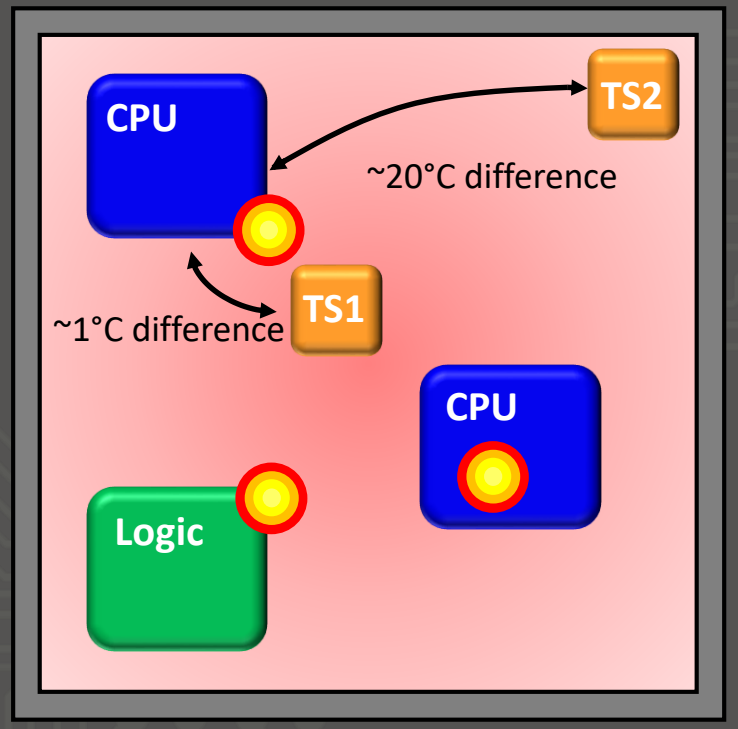
- In-Chip Conditions
  - Process – Static condition
  - Voltage & Temperature - Dynamic
- Design Challenges
  - Working silicon & Performing Silicon
  - Optimisation & Design Trade offs
  - Monitoring – speed & accuracy
  - Trust in your IP
- What is the ideal solution?

Thermal Challenges

What is happening on chip?

- Hot spots
- Thin tracks (thermal coupling)
- Electro Migration
- Power (thermal runaway)

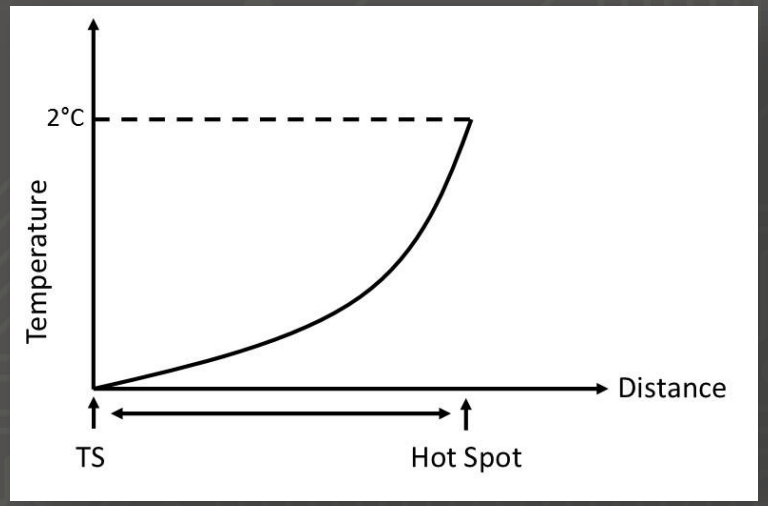
Power

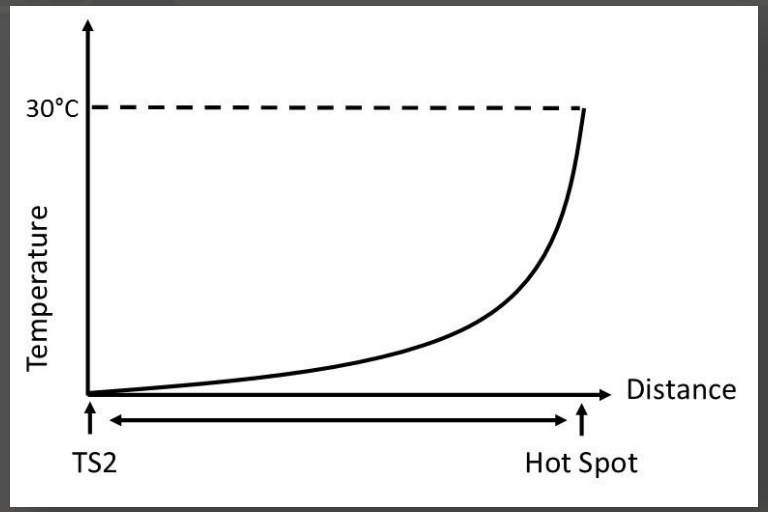


Static & Dynamic Heating

Design challenge

- Where to monitor?
- How to use monitor information?

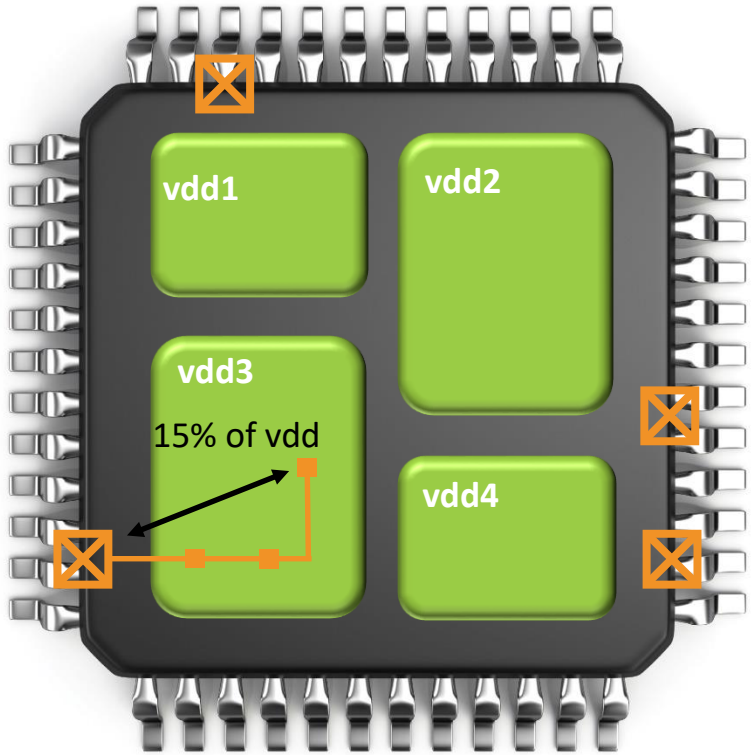




Supply Challenges

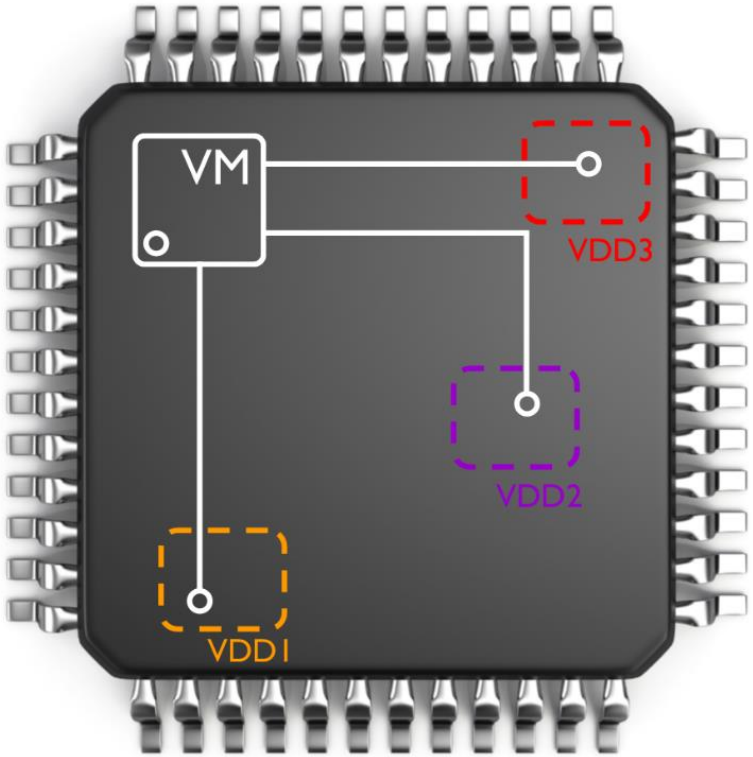
What is happening on-chip?

- IR Drops
- Vt is relatively static yet headroom as reduced.
  - Eg. Finfet with extremely low vdd
- Interconnect & via resistances increasing
- Lose state, crossing Vt esp if transient events.
- Vdd conditions may violate timing



Supply Challenges

- Dynamic power
  - Planar is leakage dominated
  - FinFET is activity dominated (bouncy supplies!)
- Therefore accurate measurement, tight control, quick regulator response.
- Maintain headroom if possible



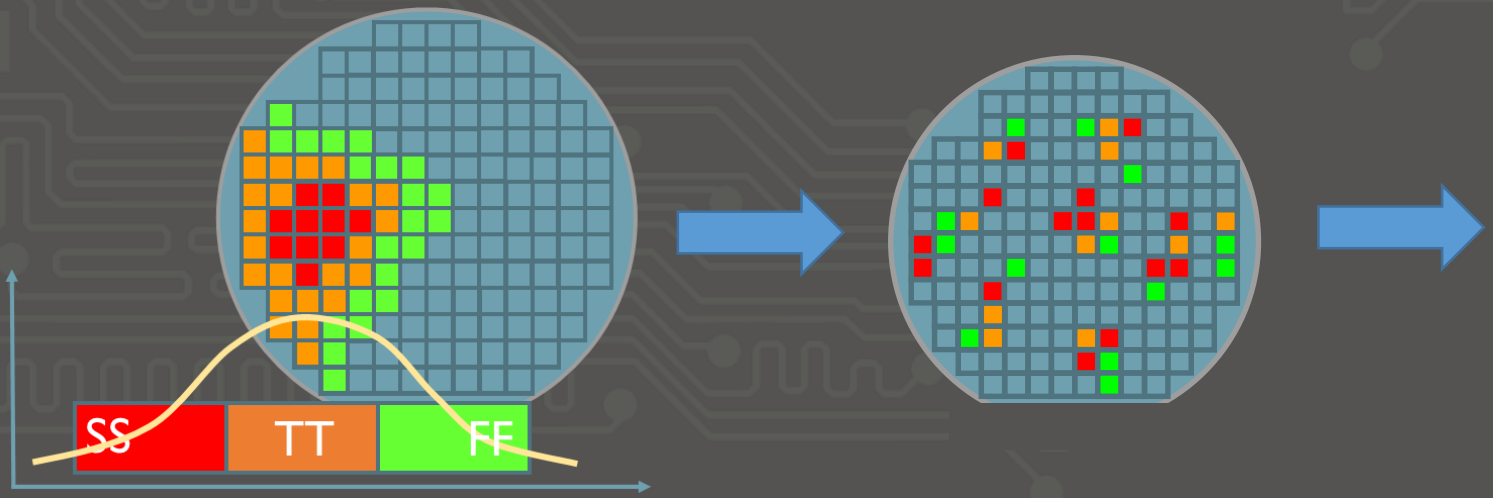
Process Challenges

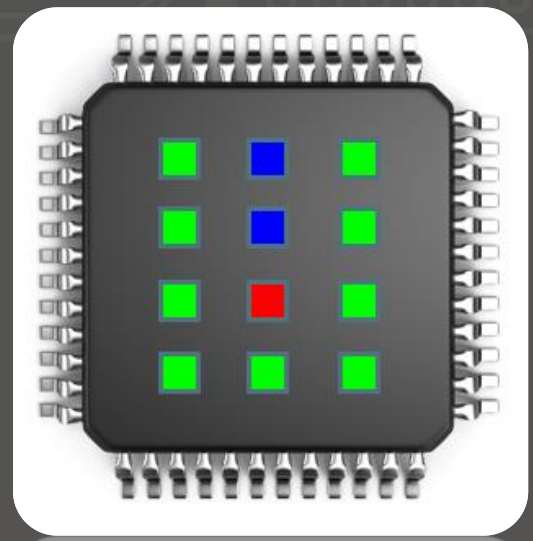
What's happening on chip?

- Increased Process Variability:
  - Multi patterning
  - Metal resistance variability increasing
  - Via resistance
  - Interconnect track lengths increasing

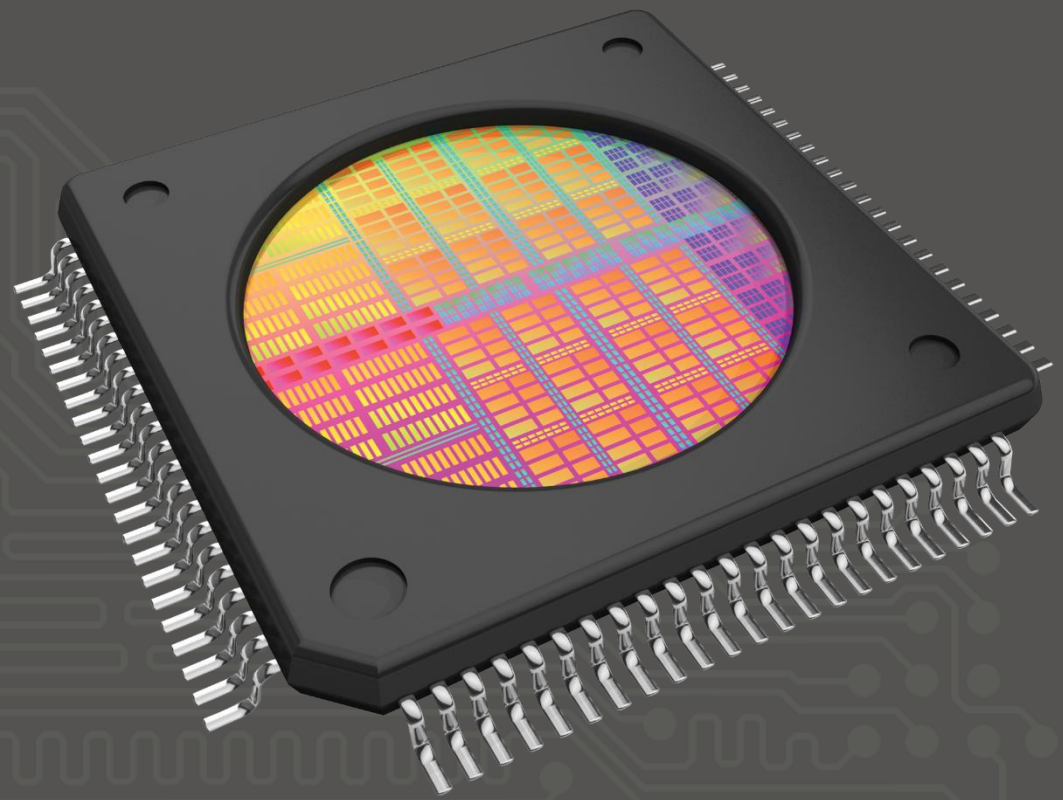
- Sensitivities to VT variation
- Aging: Gm degradation and Vt shift with aging
- Bias Temperature Instability, BTI (Vt increasing)

- Hence, greater gate delay variability



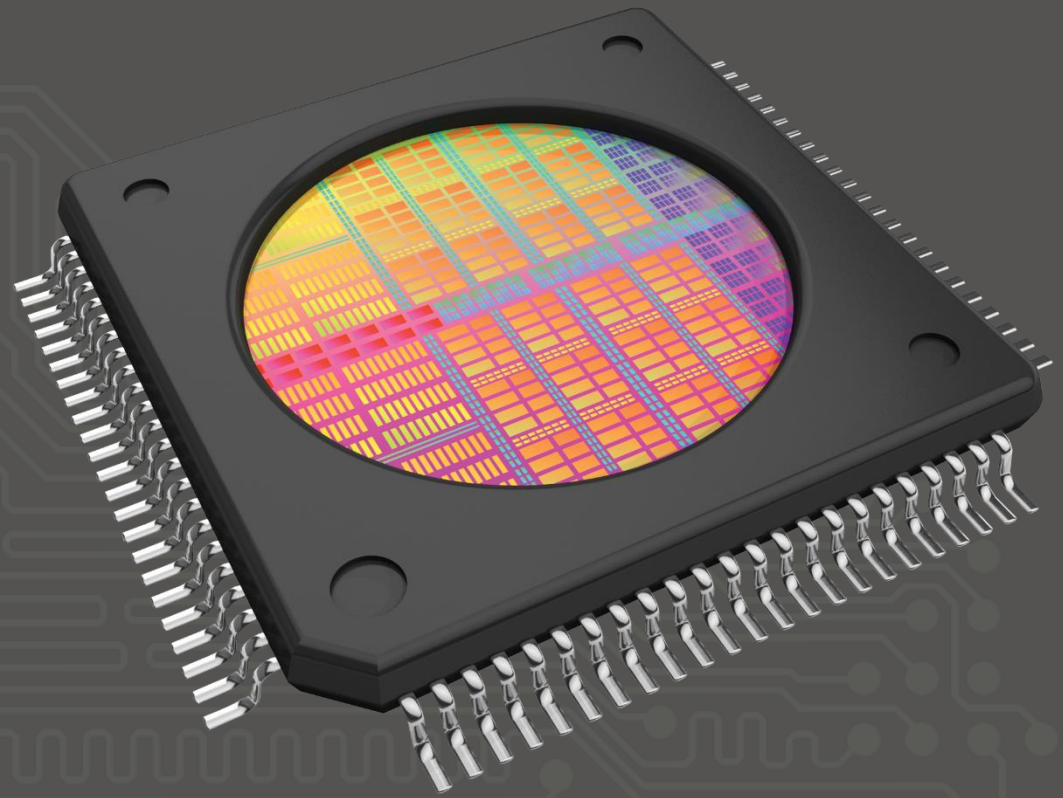


Summary



- Key Challenges:
  - Timing Closure Issue
  - Reliability
  - Thermal dissipation vs Moore’s Law
- New Design Methodologies
  - Design for *Thermal* (DFT)
  - Holistic Thermal analysis of Package & Die
  - Data!
- Opportunities
  - Optimisation
  - Accurate, trusted monitoring

Thank you



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