Compute Express Link (CXL)

Next Generation Interconnect
for
High Performance Heterogeneous Computing

IPSoC, April 9, 2020
Mobiveil - Introduction

Vision
Provide Technology, Platform and value-added services to accelerate electronic product development
- Strong portfolio of high-speed controller IPs for ASIC/FPGAs
- FPGA-based Application Platforms for SSD, IoT
- Consulting/Engineering Services

Leadership
Management with 30+ years experience in Semiconductor/Silicon IP/Product Engineering Services
Team working together developing Silicon IP & Engineering Services for 15+ years
- Silicon valley “Fast 50” in 2018
- 2018 Inc. 5000 “Fastest Growing Private Companies in America”
- 10 Most Promising Solution Providers in Storage by CIO Magazine
- 4 Patents in Storage and Flash Reliability

Location
Headquarters in Milpitas, Engineering Centers in Chennai, Bangalore and Hyderabad. Total headcount ~275
Mobiveil Vision for Application Platforms

• What are platforms
  • Bundle of highly configurable Silicon IP blocks, Pre-integrated
  • Pre-Validated FPGA platform
  • Operating Firmware
  • Pre-verified hooks to 3rd party IPs like Verification IP, PHYs
  • Pre-verified environment for the design flow like the Emulation

• Benefits of Platform
  • True acceleration of product development as much of the integration and verification is already completed
  • Reduction in cost and schedule, Product development risk minimized

• SSD Platform Example for customers developing SSD Controllers
• RISC V SOC Platform for customer developing AI and IoT SOCs
Mobiveil Platform Focus Domain

Flash Storage
- Enterprise
- Data Centers
- Laptop/Consumer
- Mobile

AI/ML/IoT
- Edge /Cloud Computing
- Smart Cities
- IOT Gateways
- Industrial IOT

Communications
- Base Stations
- HPC
- Industrial
- Aerospace
- Automotive
# IP Portfolio (1 of 2)

<table>
<thead>
<tr>
<th>Product</th>
<th>Platinum (Proven in Silicon)</th>
<th>Gold (Proven in FPGA)</th>
<th>Market</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express Gen4/3/2/1</td>
<td>Y</td>
<td>Y</td>
<td>Storage/Server/Data Center/AI/Networking</td>
</tr>
<tr>
<td>PCI Express to AXI Bridge</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>PCI Express Switch</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>PCI Express PCS</td>
<td>Y</td>
<td>Y</td>
<td></td>
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<tr>
<td>RapidIO Gen4 (25G)</td>
<td>Y</td>
<td>Y</td>
<td>Wireless Networking, Aerospace, Industrial</td>
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<tr>
<td>RapidIO to AXI Bridge</td>
<td>Y</td>
<td>Y</td>
<td></td>
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<tr>
<td>RapidIO 4/3/2/1</td>
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<td>Y</td>
<td></td>
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<tr>
<td>NVM Express Controller</td>
<td>Y</td>
<td>Y</td>
<td>Storage</td>
</tr>
<tr>
<td>Flash Reliability – LDPC Compiler (Encoder/Decoder)</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>DDR4/3</td>
<td>Y</td>
<td>Y</td>
<td>All</td>
</tr>
<tr>
<td>ONFI/TOGGLE</td>
<td>Y</td>
<td>Y</td>
<td>Storage</td>
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# IP Portfolio (2 of 2)

<table>
<thead>
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<th>Product</th>
<th>Platinum (Proven In Silicon)</th>
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<tr>
<td>RISC-V Frame Work</td>
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<td>Y</td>
</tr>
<tr>
<td>AXI Interconnect Matrix</td>
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<td>Y</td>
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<tr>
<td>PSRAM Controller</td>
<td>Y</td>
<td>Y</td>
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<tr>
<td>Hyperbus Controller</td>
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<td>Y</td>
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<td>PCI Express Gen5</td>
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<td>Q3,2019</td>
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<tr>
<td>CXL</td>
<td>Under Development</td>
<td>TBD</td>
</tr>
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</table>

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NVMStor-Ultra Configurable NVMe SSDC Platform

ARM/RISCV Core

GPIO

Device FW

PCIe Controller

NVMe Controller

MCC

DDR4 controller

ONFI/Toggle PHY

Flash

DDR PHY

Configuration & Status Registers (CSR)

WR REQ Queue

RD REQ Queue

WR DATA BUF

RD DATA BUF

Port Queue

WRITE DATA PATH

READ DATA PATH

Bank CTRL

WRITE DATA PATH

READ DATA PATH

Bank CTRL

Bank CTRL

Device FW

On Chip Control Path

On Chip Data Path
Mobiveil Configurable NVMe SSDC Platform
Unique Subsystem Development Solution

• Provides Full NVMe Based Reference Design Using Mobiveil’s Controllers
  • PCIe Gen4.0 PCIe Controller (GPEX)
  • Multiport NVMe (UNEX)
  • Flash Reliability – (LDPC)
  • Enterprise Flash Controller (EFC)
  • UMMC
    • Media Control Cluster
  • Reference Firmware is also provided. Runs on ARM or RISCV.
  • Allows various Flash parts to be used
  • Customer can add their custom value add in SW or HW
Generic Transparent PCIe Switch

9 Port Switch Example

US port-0 (Gen4, x16, 512b DP)

Switch Fabric

DS port-1 (Gen4, x2, 64b DP)
DS port-2 (Gen4, x2, 64b DP)
DS port-3 (Gen4, x2, 64b DP)
DS port-4 (Gen4, x2, 64b DP)
DS port-5 (Gen4, x2, 64b DP)
DS port-6 (Gen4, x2, 64b DP)
DS port-7 (Gen4, x2, 64b DP)
DS port-8 (Gen4, x2, 64b DP)

PIPE

US port – Upstream port
DS port – Downstream port
Compute Express Link (CXL)

- New open industry standard for high bandwidth, low latency interconnect

- Promoted by Alibaba, CISCO, Dell, EMC, Facebook, Google, HP, Huawei, Intel, Microsoft

- 1.1 Spec is now available. 2.0 spec development in progress

- Connectivity between host processor and accelerators/Memory devices/Smart NIC

- Addresses high performance computational workloads across AI, ML, HPC and communication segments
  - Heterogeneous processing: Scalar, Vector, Matrix, Architecture spanning CPU, GPU, FPGA
  - Memory device connectivity

- Based on PCIe 5.0 PHY Infrastructure
  - Leverages channel, Retimers, PHY, logical Protocols
  - CXL.io- I/O semantics
  - CXL.cache- Caching semantics
  - CXL.memory-Memory Semantics
WHY A NEW CLASS OF INTERCONNECT?

MOVE PAST THE PCIe LIMITERS ON HETEROGENEOUS COMPUTING AND SERVER DISAGGREGATION USAGES

- PCIe creates isolated memory pools with an inefficient mish-mash of access mechanisms.
- Moving operands and results back and forth between accelerators and devices is painful and inefficient.
- Resource sharing is all but disallowed.
- Latencies are an order of magnitude off of what is needed to enable disaggregated memory.
Broad Industry Support for CXL

- Alibaba.com
- CISCO
- DELL EMC
- Facebook
- Google
- Hewlett Packard Enterprise
- Huawei
- Intel
- Microsoft
All 3 representative usages have latency critical elements:
- CXL.cache
- CXL.memory

CXL cache and memory stack is optimized for latency:
- Separate transaction and link layer from IO
- Fixed message framing

CXL io flows pass through a stack that is largely identical a standard PCIe stack:
- Dynamic framing
- Higher resultant latency
REPRESENTATIVE CXL USAGES

CACHING DEVICES / ACCELERATORS
Usages:
- PGAS NIC
- NIC atomics
Protocols:
- CXL.io
- CXL.cache

ACCELERATORS WITH MEMORY
Usages:
- GPU
- Dense Computation
Protocols:
- CXL.io
- CXL.cache
- CXL.memory

MEMORY BUFFERS
Usages:
- Memory BW expansion
- Memory capacity expansion
- ZLM
Protocols:
- CXL.io
- CXL.mem
CXL SUMMARY

CXL HAS THE RIGHT FEATURES AND ARCHITECTURE TO ENABLE A BROAD, OPEN ECO-SYSTEM FOR HETEROGENEOUS COMPUTING AND SERVER DISAGGREGATION

- PCIe foundation and asymmetric architecture for broad adoption and interoperability across segments and developers (on both ends of the wire)

- A cache coherency scheme, “Coherence Bias”, designed for the heterogeneous device driven computing paradigm, not homogeneous multi-socket processor coherency

- Low latency for memory driven application models

- Three mix-and-match protocols for a wide variety of usages
Mobiveil CXL Controller (COMPEX)
COMPEX Controller

- Type 1/2/3 Device Mode
- Host Mode
- Dual Mode
- Version 2.0 Compliant
- Backward Compatible With 1.1
COMPEX Features

- Compliant to CXL Specification 2.0
- Backward Compatible with version 1.1
- Supports CXL.IO, CXL.mem and CXL.Cache protocols
- Supports Type1, Type2 and Type3 CXL Device and Host mode
- Supports Dual Mode (Device & Host)
- Supports x16 Devices
- Low Latency Design
- Packet Based User Interface
- Supports PCIe Native mode
- Uses PCISIG Certified Controller (GPEX) for CXL.io Channel
Further Engagement with Mobiveil

• Contact us at ip@Mobiveil.com