1. About Chipus
2. IoT Edge Devices: Challenges & Opportunities
3. Chipus methodology
4. Typical IoT chip at the “edge"
5. Technical case study: Battery charger
6. Success cases
7. Conclusion
Chipus Mission

“Develop chips that enable innovative and power efficient products”

Chipus has been delivering tailormade ASICs, ultra low power analog IP, efficient power management circuits and for more than 10 years.
Chipus facts

- Founded in 2009
- Successfully delivered projects to customers in:
  - North America
  - Europe
  - Asia
- ISO 9001 certified since 2017
- Global presence
  - Office in Santa Clara
  - Business development in the USA and Europe
  - Headquarters and Design Center in Brazil

Link to Design & Reuse about ISO 9001 certification
Chipus is a one-stop shop for semiconductor design

**Design services**
Develop custom circuits and retarget Chipus’ IPs using best-in-class support in order to help you develop a successful product.

**ASIC**
Taking advantage of the in house experience, Chipus is enabled to build turn-key ASIC solutions with proven success cases.

**Analog IP**
Based on a wide proven IP portfolio built over 10 years in the market, Chipus can provide you the ultra low power, analog and mixed signal IP block you are looking for.
IoT Edge Devices: Challenges & Opportunities

Famous IoT architecture
- Cloud services demand big data centers
- Gateways and aggregators will have a standard specifications
- Things are closer to people

IoT Edge devices are close to people
- **Huge** number of “things”
- Diverse applications
- Diverse requirements
IoT Edge Devices: Market Segments

Precision agriculture
- Long time in the field
- Low requirements for bandwidth
- Low requirements on uC
- No access to maintenance
- Custom sensor AFE

Modern wearable device
- Frequently charged
- High requirements for bandwidth
- High requirements on uP
- Quick access to maintenance
- Custom sensor AFE
Precision agriculture

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Both solutions demand custom chips
**IoT Edge Devices: System Architectures**

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### IoT Edge Devices: System Architectures

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**Are they really the same?**

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<th>DAC</th>
<th>POR</th>
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![Digital Block Diagram](image_url)
IoT Edge Devices: System Architectures

Understanding trade-offs and building specifications is part of Chipus’ know-how
Chipus counts on structured mixed-signal methodology to achieve first-working silicon

Based on checklists, design reviews and supported by ISO procedures
Our IP porting methodology takes advantage of validated testbenches of proven IPs

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<th>Specification Capture Phase</th>
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<th>Physical Implementation Phase</th>
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<td>Chipus will work with customer to mature a set of specifications that fit the product and its manufacturing, while enabling the design team to work efficiently.</td>
<td>Chipus’ design team will reuse existing IP to speed up the development of the ASIC. Thorough verification will be made to check every specification in all operating condition. Customer is invited to participate in joint design reviews specifically in ATE for manufacturing</td>
<td>Building on top of the documentation from the design team, physical implementation takes all best practices in account to achieve performance and robustness. Layout reuse is also used to speed up the development.</td>
<td>Deep checks are made in the sign-off phase such as top level DRC, LVS, DFM, functional verification and appropriate requirements for ATE development. The design team also runs final checks on the functionality of the ASIC for tape-out.</td>
<td>Chipus supports the customer in the development of system prototypes, end products and full release-to-production manufacturing</td>
</tr>
</tbody>
</table>
### Digital Design Capabilities

#### Design/Functional Verification
- **Modeling**
  - SystemVerilog
  - SystemC
  - Python
- **RTL design**
  - Verilog
  - VHDL
- **Testbench**
  - Verilog
  - SystemVerilog
- **Methodology**
  - UVM

#### Logic Synthesis/ATPG
- **Logic synthesis**
- **Insertion of DFT structures**
- **ATPG**

#### Structural Verification
- **Logic Equivalence Check (LEC)**
- **Static Timing Analysis (STA)**
- **Power Analysis (EM/IR)**
- **Physical Verification (DRC/LVS)**

#### Design Implementation
- **Floorplan**
- **Power Plan**
- **Placement**
- **CTS**
- **Routing**
- **Signal Integrity**
- **Timing closure**

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Digital flow implemented with Cadence, Synopsys and Mentor tools
Typical IoT chip at the “edge”

Device at the “edge”

- Acquire from sensors
- Convert data
- Process and store
- Manage power efficiently
- Send data and receive commands
Typical IoT chip at the “edge”

- Analog Front-ends
- Data Converters
- Integrated sensors
- Power Management
- RF Front-ends
- Digital Circuits
Typical IoT chip at the “edge”

Technical example

Analog Front-ends
Data Converters
Integrated sensors
Power Management
RF Front-ends
Digital Circuits
Battery charger is a mixed signal IP that requires care in the design in several levels:

- **Analog variations and mismatches**
  - References
  - Buffers
  - Isolation from substrate noise

- **High power sections**
  - Current handling
  - Proper bulk biasing

- **Digital Section**
  - Correct functionality
  - Register mapping
  - Communication interface

- **Integration**
  - Several voltage domains
  - Thermal issues
  - Noise issues
Case Study: Battery Charger

Analog checks include:

- Several power up conditions
- Several operating conditions
- Verification of operation modes
- Verification of configurable performances
- Trimming

These checks must take into account:

- Validation across corners
  - Process
  - Voltage
  - Temperature (-40°C to 125°C)
- Monte Carlo checks
Case Study: Battery Charger

Mixed signal simulations (AMS) are used since the beginning of the project to avoid bugs in late phases.

- Flags
- Registers
- Protections
- Trimming
- Communication
- ...

Constant current mode

Battery fully charged

Trickle current mode

Constant voltage mode
In the overall functionality this type of curve is what we are looking for in silicon measurement.

Simulation results
The IPs implement the following charging modes for best battery management:

1. **Trickle**: IP applies low current until battery voltage is in safe range
2. **Fast**: full charging current (configurable)
3. **Constant voltage**: IP keeps constant voltage until battery is completely full

*This is obtained after thorough verification in both design and layout phases*
### Power Management ASIC

#### Some Information

- 3 DC-DCs (2 bucks and 1 boost) up to 500mA
- Battery Charger up to **1.1 A**
- LED Drivers (4x) up to 300mA
- Load switches up to 100mA
- Ultra-Low-Power LDOs/References/Osc/POR
- USB interface for battery charging
- Ultra-low-power (**350 nA**) in idle mode
- Node: 0.18µm BCD

#### Main Challenges:

1. **Big power transistors** (total load up to 1.8A) while having a stand-by mode of only 350nA. Leakage optimization at device level required;

2. **Cannot use duty-cycle to reduce consumption** (Power Management is the only chip that needs to be "on" in the system even in sleep mode).
Magnetic Sensor ASIC

Some Information

- Integrated Magnetic Sensor
- Integrated Sensor
- Ultra-low power (250 nA)
- Specs to Production in 18 months
- Node: 0.13µm CMOS
- Status: In Production since Q4/2016

Main Challenges:

1. Wake up, measure, send data, sleep in the shortest time possible using duty-cycle techniques to optimize consumption
2. Innovative sensor technology (custom analog front-end design)
Chipus counts on more than 200 silicon-proven mixed-signal IPs to speed up ASIC development.

- **Power management**
  - High voltage
  - High current
  - Low power
  - High efficiency

- **Data converters**
  - ADCs and DACs

- **Integrated sensors**
  - Temperature
  - Capacitive touch
  - Magnetic

- **Optical**
  - Analog Equalizers (<28Gbps)
  - TIAs, PAs

- **RF**
  - RFID front-ends
  - RF Transceivers

- **Processes**
  - CMOS
  - BCD
  - SOI
  - SiGe

- **Nodes**
  - 0.18um
  - 0.13um
  - ...
  - 40nm
  - 22nm
  - 7nm

- **Applications**
  - Consumer
  - Industrial
  - Automotive
  - Optical communications
  - Medical
  - Wearables
● IoT at the “edge” demands custom chips due to specific requirements
● Interesting opportunity for ASIC companies
● Chipus is ready to provide effective solutions based on:
  ○ proven expertise over the years
  ○ extensive analog and digital IP portfolio
  ○ Porting of proven IPs to reduce time to market
  ○ Strong Analog and Digital knowledge
● Project methodology transforms specifications into parts
  ○ Based on ISO procedures
  ○ Checklists
  ○ Design reviews with customer
  ○ Flexibility to adapt to customer
● Our customer’s success is also our success as shown in all of our ASIC engagements
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Thank you