IP Provider the Seed of Innovation in Electronic Industry. Can IP Innovation be Measured?

Gabrièle Saucier
Design And Reuse

IP SoC Day Silicon Valley 2020
IP Concept: Why? Who? Which IP?

- **Why?**
  - Time to market pressure; Engineering (Knowledge) shortage
  - Talented engineering available? Globalization?
- **IP Concept born:** Resource & Knowledge sharing/Reuse
- **IP Business.** NRE, Licensing fee, Maintenance, Royalty

**Star IP**
ARM, Amba Ecosystem

**Standard Centric**
Interface IP

**Design Skill Centric**
Analog, Embedded memory

**Knowledge Centric**
AI, Automotive, Video, Security

![EDA vendor]

Alliance program
IP as Enablers

![Foundry]

Fabless IC Vendor
Asic in Electronic Systems
AI, IoT, medical, mobile, network …

![Design & Reuse]
Outline

• Introduction: D&R community

• D&R partners hold patents? – Who and How many?

• Any correlation between IP attraction and patent holding?

• D&R initiative a patent panel
D&R Ecosystem: 42.000 Registered members

D&R founded in 97 as a privately hold company:

Be the catalyst of IP Dissemination & IP business providing support to IP providers & IP consumers:

IP Search or scouting....

• Hold Premier IP SoC Market Place www.design-reuse.com
  – displaying exhaustive list of resources available as Silicon IP and SoC (System on Chip) solutions
  – Facilitating the contact between provider and consumer
• Extended to www.dr-embedded.com (2012)
  – Dedicated to Application specific solutions (Automotive, AI, IoT, Security, ...)
• Extended to www.design-reuse-china.com (2016)
  – Dedicated to Chinese audience

Provides next generation Technology and Services based on IP Management Platform - IPMS™

• Web e-Catalog
• IP Management Enterprise Platform For IP providers and IP consumers
• Vendor tool Management
D&R Community

- 42,000 Registered Users

- End product
When was the company created?

- Early at the IP concept launching (before 2000)
- A peak between 2000 and 2009: the IP concept was mature
- Innovation does not stop...
D&R Partner Company Size

- Whole Spectrum of design forces in Electronic industry represented
  - Small innovators/design centres
  - 44% of Partners are medium sized design centres (11-50 employees)
  - Large and extra large companies participate (IP as enablers)

The number of IP providers who are partners of D&R is "stable"
The number of acquired companies compensate by the number of newly created companies
Provider as innovation seed of Electronic Industry?

Are patent a proof of innovation?

- Who holds patent?
  - Those who can afford? Time and money?
  - Venture support
  - Proof of innovation needed

- Do patent holders attract more traffic on our website

Analysis targeting the IP providers partner of D&R

**Important Note**

D&R performed a manual Google search for finding patents hold by our partners
No guarantee of completeness
Providers to contact us for correction
Who holds patents?

- 63% of D&R partners hold patents - 37% do not hold any patent
- No patent
  - No time and money to do so
  - 78% are small companies (2-10 employees) and medium (11-50) companies
Distribution according to number of patents

63% of D&R partners hold patents

- How many?
  - Innovators will perform few “key” patents deposit to prove their innovation
  - When becoming established innovation consolidated by a “patent portfolio”
  - Large companies have a specialized departments to do so
  - Extra large companies may deploy a “patent war” (not only IP)
Category 1: Extra small number of patents (1,2)

- Small companies, start up
- Design center with analog IP
- Adding IP business from an existing activity (EDA, system design)
Small Number of patents (up to 10)

Innovation centric

- Consolidated Technology innovation (Kandy Bus, Silicon library)
- Video/image (Allegro, Intopix)
- AI (Brainchip)
- Processor, GPU (Minima, Silicon Arts)
- Avionics (Accord software)
“Established “ IP provider highly specialized

- Technology innovation supported by larger companies (NSCore, Sofics, Floadia)
- Proven Design center (Dolphin technology, Dolphin design, Brite Semi, CSEM)
- Application centric
  - Video (Chip& Media), DSP (Ceva)

Other characteristics

- New area (AI) & Venture supported (Gyrfalcon)
- Encouraged by Asian “patent” culture: Chinese young or established players (M31, Andes technology, Verisilicon, attopsemi, Acct)
Providers with large number of patents

Chip/Custom chip provider (not just IP provider). Difficult to filter IP centric patent

- Sunplus, Delta systems, SST (microchip subsidiary)

Foundry related design center
- Faraday, eMemory

Finally 3 “star IP” providers with a big number patents
- Rambus, Imagination, Arm

Note
EDA vendors (Mentor, Synopsys, Cadence, Silvaco)
& Foundries (TSMC)
are not listed.

- Non IP centric patents
- Large portfolio
Correlation between patent and web attraction?

Analysis per category

- Most of the traffic (but not all) goes to IP from providers holding patent
  - Analog design
  - Especially when going to complex IP
<table>
<thead>
<tr>
<th>Subcategory</th>
<th>IP Name</th>
<th>Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>AI Processor</td>
<td>DPU for Convolutional Neural Network</td>
<td>Xilinx, Inc.</td>
</tr>
<tr>
<td></td>
<td>Machine Learning Processor</td>
<td>Arm Ltd.</td>
</tr>
<tr>
<td></td>
<td>Neuromorphic IP</td>
<td>BrainChip Inc.</td>
</tr>
<tr>
<td>IoT Processor</td>
<td>Convolutional Accelerator for Convolutional Neural Networks (CNN)</td>
<td>iBex Logic</td>
</tr>
<tr>
<td></td>
<td>Full eNB-IoT Release 14 IP solution with multi-constellation GNSS support for IoT devices</td>
<td>CEVA, Inc.</td>
</tr>
<tr>
<td></td>
<td>IEEE 802.11ax MAC/PHY for STA</td>
<td>Comsis</td>
</tr>
<tr>
<td>Processor Cores</td>
<td>RISC-V Processor - 32 bit, 3-stage</td>
<td>Codasip Ltd.</td>
</tr>
<tr>
<td></td>
<td>Smallest, Lowest Power ARM Multicore Applications Processor</td>
<td>Arm Ltd.</td>
</tr>
<tr>
<td>Audio Processor</td>
<td>Neural network-based speech recognition technology for voice assistants and IoT devices</td>
<td>CEVA, Inc.</td>
</tr>
<tr>
<td></td>
<td>Multipurpose Hybrid DSP and Controller Architecture Family</td>
<td>CEVA, Inc.</td>
</tr>
<tr>
<td></td>
<td>Tensilica HiFi 5 DSP for AI Speech and Audio Processing</td>
<td>Cadence Design Systems, Inc.</td>
</tr>
<tr>
<td>CPU</td>
<td>RISC-V SOC Platform</td>
<td>Mobiveil Inc.</td>
</tr>
<tr>
<td></td>
<td>Ultra Compact 32-bit RISC-V CPU Core</td>
<td>Andes Technology Corp.</td>
</tr>
<tr>
<td></td>
<td>Arm Cortex-a77</td>
<td>Arm Ltd.</td>
</tr>
<tr>
<td>DSP Core</td>
<td>Full eNB-IoT Release 14 IP solution with multi-constellation GNSS support for IoT devices</td>
<td>CEVA, Inc.</td>
</tr>
<tr>
<td></td>
<td>Multipurpose Hybrid DSP and Controller Architecture Family</td>
<td>CEVA, Inc.</td>
</tr>
<tr>
<td></td>
<td>Software-Compatible DSPs For Radar, Lidar and 5G Applications</td>
<td>Cadence Design Systems, Inc.</td>
</tr>
<tr>
<td>Microcontroller</td>
<td>Super-Fast 8051 Microcontroller Core with Configurable Features and Peripherals</td>
<td>CAST, Inc.</td>
</tr>
<tr>
<td></td>
<td>Floating Point Processor for Embedded Systems</td>
<td>Cortus, Inc.</td>
</tr>
<tr>
<td>Security Processor</td>
<td>Near-threshold voltage and ultra-wide dynamic voltage and frequency scaling (UW-DVFS)</td>
<td>Minima Processor</td>
</tr>
<tr>
<td></td>
<td>Very Low gate Count, Hardware level, Software Data Isolation and Master level Data protection engine.</td>
<td>Green IP Core</td>
</tr>
<tr>
<td></td>
<td>Transaction-aware embedded cybersecurity solution that can detect, block and record attacks, &amp; prevent propagation</td>
<td>UltraSoC Technologies Ltd.</td>
</tr>
</tbody>
</table>
Most Popular IP

All IP

• 40% of the most popular IP are not covered by patent
  • Innovative IP from small company have their chance
• 60% of the most popular IP are provided by patent holders

D&R web sites serves both
• small innovators
• established major providers
### D&R initiative: Patent Panel

**Goal**

- Making available promptly information about patent status of D&R partners
- IP scouting: a selection choice? Some IP consumers may be interested in knowing promptly the patent portfolio of a provider

<table>
<thead>
<tr>
<th>Assignee</th>
<th>Nb of Patents</th>
<th>Company Size</th>
<th>View More</th>
<th>Patent Application Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arteris IP</td>
<td>1</td>
<td>51-200</td>
<td></td>
<td>GB2534992B</td>
<td>Configurable snoop filters for cache coherent system</td>
</tr>
<tr>
<td>Creonic</td>
<td>1</td>
<td>2-10</td>
<td></td>
<td>EP3086474B1</td>
<td>Method for controlling a check node of a nb-lpgc</td>
</tr>
<tr>
<td>EnSilica Limited</td>
<td>1</td>
<td>51-200</td>
<td></td>
<td>US9917688B2</td>
<td>Two point polar modulator</td>
</tr>
<tr>
<td>Mixel, Inc.</td>
<td>1</td>
<td>11-50</td>
<td></td>
<td>US10289511B2</td>
<td>Differential physical layer device with testing capability</td>
</tr>
<tr>
<td>Mobile Semiconductor Corporation</td>
<td>1</td>
<td>11-50</td>
<td></td>
<td>EP2122473B1</td>
<td>ADAPTIVE MEMORY SYSTEM FOR ENHANCING THE P</td>
</tr>
<tr>
<td>ORTHOGONE TECHNOLOGIES INC.</td>
<td>1</td>
<td>51-200</td>
<td></td>
<td>US10447463B2</td>
<td>Device and method for ultra-low latency communication</td>
</tr>
<tr>
<td>PACIFIC MICROCHIP CORP.</td>
<td>1</td>
<td>2-10</td>
<td></td>
<td>US96282635B2</td>
<td>Signal digitizer and cross-correlation application scramble</td>
</tr>
<tr>
<td>SEAMLESS MICROSYS, INC.</td>
<td>1</td>
<td>2-20</td>
<td></td>
<td>US10075313B2</td>
<td>Systems and methods for ring-oscillator based operation</td>
</tr>
<tr>
<td>Silicon Creations</td>
<td>1</td>
<td>51-200</td>
<td></td>
<td>US9354441B2</td>
<td>Receiver optical assemblies (ROAs) having photo-detectors</td>
</tr>
<tr>
<td>Tamba Networks, Inc.</td>
<td>1</td>
<td>2-10</td>
<td></td>
<td>US6832613B1</td>
<td>Tunable design of an interlaced region of an integr</td>
</tr>
<tr>
<td>Thalga Design Automation</td>
<td>1</td>
<td>11-50</td>
<td></td>
<td>US10055527B2</td>
<td>Yield process for analog circuit design optimization</td>
</tr>
<tr>
<td>Zhuhai Chuangfexin Technology</td>
<td>1</td>
<td>11-50</td>
<td></td>
<td>US10128148B2</td>
<td>Antifuse structure in via hole in interlayer dielectric metering</td>
</tr>
<tr>
<td>Analog Bits, Inc.</td>
<td>2</td>
<td>11-50</td>
<td></td>
<td>US8866556B2</td>
<td>PHASE SHIFT PHASE LOCKED LOOP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>US8742957B2</td>
<td>MULTI-VARIABLE MULTI-WIRE INTERCONNECT</td>
</tr>
</tbody>
</table>
Conclusion

- IP visibility or attraction goes
  - to innovators even who have no time and money to deposit patents
  - to established providers who hold patent
    - Equally distributed about few patents and large portfolio

Electronic world need both
- resources and design skill
- Point innovation

- D&R web sites serves both