Broadest Portfolio of Low Power Differentiated IP
Corporate Background

Heritage
- Focused on differentiated low power mixed-signal IP
  - Founded in 1995, based in the Silicon Valley
  - Independent with no external funding

Track Record
- World-class mixed signal CMOS engineering staff
  - Extensive experience in advanced SoC designs
  - IP in billions of silicon from 0.25\(\mu\)m to 5nm FF

Core Values
- Premier IP partner from architecture to silicon
  - Customer-centric business engagement
  - Engineering-centric support

Client Base
- Global customer base: 50% US, 50% international
  - 500+ Customers in 70+ Processes
Advanced Technology Leadership in FinFet Processes
16/12/14nm IP Shipping in Production & Numerous 7nm Production Tape-outs

- Multiple products on 16nm/14nm in Mass Production for Smart Phones using PLL’s, Sensors and IO’s
- Lowest power 4.3pj/bit 1-15G SERDES on AI SoC on 16FF+
- 16FFC/14LPP Production Silicon - PLL and Sensor, IO, Serdes
- 16FFC Automotive-grade PLL, Sensor and Xtal OSC available
- 16FFC 1-25G Enterprise Class SERDES shipping
- 16FFC and 12FFC 1-10G Ultra low power SERDES shipping
- GF 12LP Taped-out with PLL, Sensor, POR and IO’s – Q4-19
- Numerous production FinFet tape-outs at TSMC, Samsung, GF
- 7FF Automotive-grade PLL, Sensor and IO’s Working Silicon
- N6 Test-Chip Tape-out with PLL, Sensors, IO Taped Out
- Enterprise class 1-32G PCI Gen5 SERDES Taped Out in 8nm
- Ultra Low Power 1-16G Low Power SERDES Taped Out in 7nm
- Ultra Short Reach and Die to Die SERDES in development
- N5P Test-Chip Tape-out with PLL, Sensors, IO – Q1-2020
- N6 Test-chip with HP PLL, IO’s – Q2-2020

Confidential Information

Unparalleled Power Performance
### Merchant Fabs

**Process Names, (Red in Production, Black pre-production)**

<table>
<thead>
<tr>
<th>Process Names</th>
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</thead>
</table>

### IDM Fabs

<table>
<thead>
<tr>
<th>Process Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>45LP, 32LP, 28LP, 28FDSOI, 14LPP, 8LPP, 7LPP, 5LPE</td>
</tr>
</tbody>
</table>

### Low Cost Fabs

<table>
<thead>
<tr>
<th>Process Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.13u, CH90G, CH90LP, CH65G, CH65LP, CH65LPE, CH45LP, 40LP, 32LP, 28SLP, 22FDX, 14LPP, 12LP, 12LP+</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Process Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>L250, L180 HS, L150 HS, L130E HS, L130 SP, L130 LL, L90SP, L90G, 65SP, 65LL, 40LP, 28HPL, 22ULL</td>
</tr>
</tbody>
</table>

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**Confidential Information**
Analog Bits - Clocking and Sensor IP Portfolio

**Clocking**
- Wide-range, low power PLL- Integer, FracN/SSCG
- Ultra low jitter sub-picosecond LC PLL
- PCIe Clock PHY IP – eliminates Clock Chip, saves BOM
- High performance C2C PLL (20GHz)
- Digital Core Power PLL
- Ultra low power sub-micro watt IOT class PLL
- High reliability radiation tolerant PLL

**Sensors**
- Integrated On-Die PVT Sensor
- Power on Reset with Burn-Out Detection
- On-Die Power Supply Glitch Detector
- Digital Core Power Sensor
- Bandgap Generator
- System Power Detector

New Products introduced in 2019 and 2020
Differentiated IO for High Performance & Low Power/Cost IoT Markets

- Differential clock transmitter and receiver
  - LVDS, CML, etc
- PCI-Express - HCSL clock drivers
- C2C IO’s
- Low noise and low power crystal oscillators
- Lowest Power Crystal-less OSC pads for IoT
- Voltage tolerant IO buffers
- DDR IO’s

7nm Differential IO TX/RX
7nm CML Pads
## Portfolio of Analog Foundation IP Availability in FinFET

<table>
<thead>
<tr>
<th>Foundation Analog IP</th>
<th>TSMC N5P</th>
<th>TSMC N7//N6</th>
<th>TSMC 16FFC</th>
<th>TSMC 12FFC</th>
<th>Samsung 14LPP</th>
<th>GF 14LPP/12LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integer PLL</td>
<td>Apr-2020</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>FracN/SSCG PLL</td>
<td>May-2020</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>PCI Ref Clock PLL</td>
<td>Q2-2020</td>
<td>Q2-20</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td></td>
</tr>
<tr>
<td>20GHz C2C PLL</td>
<td>Apr-2020</td>
<td>Available</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sensor</td>
<td>Apr-2020</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>POR</td>
<td>Q2-2020</td>
<td>Q2-20</td>
<td>Available</td>
<td>Available</td>
<td></td>
<td>Available</td>
</tr>
<tr>
<td>Glitch Detector</td>
<td>Apr-2020</td>
<td>Available</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Power Sensor</td>
<td>Q2-2020</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandgap</td>
<td>Q2-2020</td>
<td>Available</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OSC Pads</td>
<td>Apr-2020</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Buffers</td>
<td>Apr-2020</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td></td>
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</tr>
</tbody>
</table>
Multi-rate, multi-protocol SERDES
- Lowest power & latency
- Smallest area
- Programmable for numerous channel environments

And enabling many SOC applications
PCIe Gen 4 and Gen5 Developments

- **Enterprise Class PCIe Gen5 SERDES**
  - 1-32G multiprotocol enterprise class PCIe Gen 4/5 SERDES
    - Area: 0.432mm²
    - Power: 7.5 pj/bit
    - Taped-out in October in Samsung 8nm
      - Expected Silicon in Q2
- **Low Power PCIe SERDES**
  - 1-16G multiprotocol low power PCIe Gen 4 SERDES
    - Area: 0.35mm²
    - Power: 6 pj/bit
  - 1-8G multiprotocol low power PCIe Gen 3 SERDES
    - Power: 4 pj/bit
    - Taped-out in December in Samsung 7nm
## SERDES IP Availability

**TSMC 16FFC, 12FFC, 7FF, Samsung 14LPP, 8FF, 7FF**

<table>
<thead>
<tr>
<th>Serdes IP</th>
<th>TSMC 16FFC</th>
<th>TSMC 12FFC</th>
<th>Samsung 14LPP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-25G PCIe3/4, SAS3/4, SATA3 (Multiprotocol enterprise class)</td>
<td>Production Silicon</td>
<td></td>
<td></td>
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<tr>
<td>Enterprise grade 1-16G PCIe3/4</td>
<td>Production Silicon</td>
<td></td>
<td>Production Silicon</td>
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<tr>
<td>1-8G Low power SERDES (PCIe 2/3 – consumer)</td>
<td>Production Silicon</td>
<td>Production Silicon</td>
<td>Production Silicon</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Serdes IP</th>
<th>Samsung 8FF</th>
<th>Samsung 7FF/5FF</th>
<th>TSMC N5P</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-32G PCIe3/4/5, SAS3/4, SATA3 (Multiprotocol enterprise class)</td>
<td>Available</td>
<td></td>
<td>Upon Customer Program Request</td>
</tr>
<tr>
<td>Enterprise grade 1-16G PCIe3/4</td>
<td>Available</td>
<td></td>
<td>Upon Customer Program Request</td>
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Why Analog Bits

**Differentiated IP** with broadest portfolio focused with best in class PPA

**Excellent Reputation** for best-in-class mixed signal designs in the Silicon Valley

**Global Customer Base** from 0.25µm to 5nm FinFET

**Volume Business Friendly** no royalty model