Automotive-Qualified IP for Evolving Integrated ADAS Domain Controller SoCs

D&R IP SoC Days Silicon Valley

Ron DiGiuseppe,
Automotive IP Segment Manager
April 2020
ADAS & Autonomous Driving SoCs

Goal: Reduce Accidents, Injuries & Fatalities

• 6.2 million automotive accidents and 35,000 deaths* in 2015 (in United States)
• About 94% of accidents caused by human error*
  – 2% environment, 2% mechanical, 2% margin error

• ADAS applications (vision-based)
  – Rear view camera
    – Park assist
  – Front camera
    – Pedestrian detection
    – AEB (Automatic Emergency Braking)
  – Surround view cameras
  – Interior camera
    – Drowsiness / gaze detection

Automotive Systems Transition to Centralized Compute Architecture

Architecture Trends shown by Continental

- Increasing requirements for compute performance lead to centralized architectures
- Separate hardware from Software
  - SW integration required
- Requires Multi-layered security and safety
  - Due to single point of failure & vulnerabilities

Source: Dr Elmar Degenhart, CEO, Continental CES 2018 Strategy Presentation
https://www.continental-corporation.com/resource/blob/118106/deafe75b7e11426dabc785c0e0316ab/2018-01-09-strategy-key-figures-data.pdf
Examples of ADAS Architectures

Delphi (Aptiv) Multi-Domain Controller (MDC)

- System & Component Integration
  - Higher computing, performance and density
  - Same trend as smartphones and servers in last 10 years
- Ongoing development in established suppliers and start-ups

Audi ZFAS Centralized ADAS Module

- System & Component Integration
  - Higher computing, performance and density
  - Same trend as smartphones and servers in last 10 years
- Ongoing development in established suppliers and start-ups
Centralized ADAS typical SoC Architecture

- **Interfaces**
  - LPDDR5/4/4X, Ethernet TSN, MIPI, HDMI, PCI Express, CXL, ADC

- **Processing with Accelerators**
  - Embedded Vision
  - DSP

- **Security**

- **SoC Safety Manager**

- **Sensor Fusion**

- **28-nm → to 16-/14-nm → 8-/7-nm**

- **Requires Functional Safety**
Designing Multi-Domain ADAS Processors for Safety Critical Operations
Automotive Functional Safety

ISO 26262 Standard Focuses on Safety-Critical Components

• “Safety-Critical” systems must minimize risk of catastrophic failures and respond to failures in a predictable manner

• ICs in these systems must meet ISO 26262 functional safety requirements

• Automotive Safety Integrity Level (ASIL) designates risk potential, from QM (lowest) to D (highest)

• Compliance certifications for SoCs granted by accredited providers
  – Product & process reviews
  – Product assessments, audits & certifications

Automotive Safety Integrity Levels (ASIL)

Evolving ASIL Requirements
Adapting SoC Development Flows to ISO 26262
Synopsys Automotive IP with ISO 26262 Functional Safety Features
Example Showing Safety Mechanisms Added to DesignWare LPDDR4 Controller & PHY

- Inline ECC – Data Path Protection
- On-chip Parity– end-to-end Data Path Protection
- Register Parity Protection on critical clocking
- Command and Address Path Protection: Parity, ECC and Redundancy
- Command and Address Path Protection: Parity and Redundancy
- Configuration and Status Registers Parity Protection

Certification for ISO 26262 Part 5 HW
Automotive Safety Features

DesignWare MIPI CSI-2 Device Controller IP

- ECC Protection on Packet Header stored in Memory
- ECC Protection on IDI/IPI Packet Header
- Parity Protection on IPI Data Path
- Parity Protection on Configuration Registers
- IPI/IIDI Overflow Protection
- CRC Protection on Packet data path
- IDI Header and payload Data checks
- Module Redundancy Protection for critical logic

Certification for ISO 26262 Part 5 HW
Automotive Reliability
Synopsys Has Defined Internal Reference Temp Profiles Based on Multiple Automotive Engagements

**Target Low PPM Automotive Reliability vs. Consumer**

- **Typical consumer component**
  - Limited DFM effort in design
  - Limited test coverage / DFT
- **Automotive component**
  - Safe launch
  - Corrective actions

**Temperature Mission Profile* Industry Example**

<table>
<thead>
<tr>
<th>Operation time* [h]</th>
<th>Duration (h)</th>
<th>Percentage (%)</th>
<th>Tj component (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>10</td>
<td>10</td>
<td>48</td>
</tr>
<tr>
<td>1600</td>
<td>16</td>
<td>16</td>
<td>71</td>
</tr>
<tr>
<td>6500</td>
<td>65</td>
<td>65</td>
<td>108</td>
</tr>
<tr>
<td>890</td>
<td>9</td>
<td>9</td>
<td>150</td>
</tr>
</tbody>
</table>

Synopsys Automotive Grade IP

Reduce Risk and Accelerate Qualification for Automotive SoCs

Functional Safety

Accelerate ISO 26262 functional safety assessments to help ensure designers reach target ASIL levels

Reliability

Reduce risk & development time for AEC-Q100 qualification of SoCs

Quality

Meet quality levels required for automotive applications
Synopsys SG: ISO 9001 Certified for Quality

Commitment to Quality Minimizes Integration Risk and Accelerates Time-to-Market

- Synopsys’ IP Business Unit or Solutions Group (SG) is committed to maintaining and continually improving its Quality Management System (QMS) modeled on ISO 9001:2015

- SG’s QMS is applicable to the development of Synopsys’ portfolio of DesignWare IP and tools at worldwide Synopsys sites

  - Helps ensure IP quality, minimizing integration risk
  - Increases confidence in IP development processes, eliminating the need for customers to perform 2nd party quality audits
  - Implements key clauses of IATF 16949 in our QMS, supporting additional automotive requirements

- SG’s QMS is ISO 9001:2015 certified by 3rd party: BSI
DesignWare IP Portfolio for Automotive Applications

**IP Portfolio**

- Ethernet AVB/TSN
- LPDDR5/4/4X
- MIPI CSI-2/DSI
- HDMI
- USB Host & Device
- Star Memory System
- ARC EM & HS Processors
- Security: Encryption & Decryption
- NVM

**Accelerates Qualification of Automotive SoCs**

**ASIL B/D Ready IP** with **AEC-Q100 Design & Testing** and **Automotive Quality Management** targeting ADAS, infotainment and MCU applications.
Synopsys Delivers Automotive-Grade IP in TSMC 7-nm Process for ADAS Designs

DesignWare IP in FinFET Processes Adopted by More Than a Dozen Companies

Press Releases

Synopsys Delivers Automotive-Grade IP in TSMC 7-nm Process for ADAS Designs

DesignWare IP in FinFET Processes Adopted by More Than a Dozen Companies Designing ADAS and Autonomous Driving SoCs

MOUNTAIN VIEW, Calif., Oct. 1, 2018 /PRNewswire/ --

Synopsys, Inc. (Nasdaq: SNPS) today announced delivery of DesignWare PHY IP for TSMC’s 7-nanometer (nm) FinFET processes, PCI Express® 4.0, and security IP. The delivery of automotive-grade IP in TSMC’s 7-nm process provides SoC designers with the tools to create production-quality systems, including ADAS systems, that meet the stringent reliability and operation requirements of the automobile industry.

Highlights:

• Broad portfolio of controller and PHY IP in the 7-nm process includes LPDDR4X, MIPI CSI-2 and D-PHY, PCI Express 4.0, and security IP
• IP solutions implement advanced automotive-grade design rules for TSMC 7-nm process to meet the reliability and 15-year automotive operation requirements
• ISO 26262 ASIL Ready IP with safety packages, FMEDA reports, and safety manuals accelerates SoC-level functional safety assessments

© 2020 Synopsys, Inc. 16
ASIL Ready DesignWare IP Accelerates Path to ISO 26262 Compliance*

<table>
<thead>
<tr>
<th>DesignWare IP</th>
<th>ASIL Functional Safety Level</th>
<th>Temperature Grade PHYs, Embedded Memories, NVM</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARC EM22FS Processors</td>
<td>ASIL B and ASIL D</td>
<td></td>
</tr>
<tr>
<td>ARC EV7xFS Vision Processors</td>
<td>ASIL B and ASIL D</td>
<td></td>
</tr>
<tr>
<td>ARC MetaWare Toolkits for Safety</td>
<td>ASIL D</td>
<td></td>
</tr>
<tr>
<td>Embedded Memories 16FFC</td>
<td>ASIL D</td>
<td>Grade 1 &amp; 2</td>
</tr>
<tr>
<td>Star Memory System (SMS)</td>
<td>ASIL D</td>
<td></td>
</tr>
<tr>
<td>Star Hierarchical System (SHS)</td>
<td>ASIL D</td>
<td></td>
</tr>
<tr>
<td>EEPROM and Trim NVM</td>
<td>ASIL D</td>
<td>Grade 1 &amp; 2</td>
</tr>
<tr>
<td>Ethernet QoS, Ethernet XPCS and 10GMAC</td>
<td>ASIL B</td>
<td></td>
</tr>
<tr>
<td>PCIe 4.0 Controller, PCIe 3.1 Controller &amp; 16FFC PHY</td>
<td>ASIL B</td>
<td>Grade 1 &amp; 2</td>
</tr>
<tr>
<td>USB 2.0 &amp; 3.0 Controller &amp; 16FFC PHY</td>
<td>ASIL B</td>
<td></td>
</tr>
<tr>
<td>LPDDR4 Controller &amp; 16FFC MultiPHY v2</td>
<td>ASIL B</td>
<td>Grade 1 &amp; 2</td>
</tr>
<tr>
<td>MIPI CSI-2 Controller &amp; 16FFC PHY</td>
<td>ASIL B</td>
<td>Grade 1 &amp; 2</td>
</tr>
</tbody>
</table>

*Certification for ISO 26262 Part 5 HW Development
Synopsys Differentiation

• **ADAS:** Fastest growing automotive application: 19% CAGR ‘14-23

• Synopsys provides ISO 26262 Safety Features integrated into Automotive IP portfolio
  - DDR, Ethernet, USB, MIPI CSI-2/DSI, PCIe IP
  - Memories, Logic Libraries and Test & Repair
  - Analog and Non-Volatile Memory
  - ARC EM & ARC Safety Island with Safety Enhancement Package
  - Sensor & Control IP Subsystem
  - VDKs, IP Prototyping Kits

• ISO 26262 ASIL Ready IP, AEC-Q100 Design, Verified & Testing, Automotive Quality Management accelerates qualification of automotive SoCs
Thank You