The environmental footprint of semiconductor manufacturing

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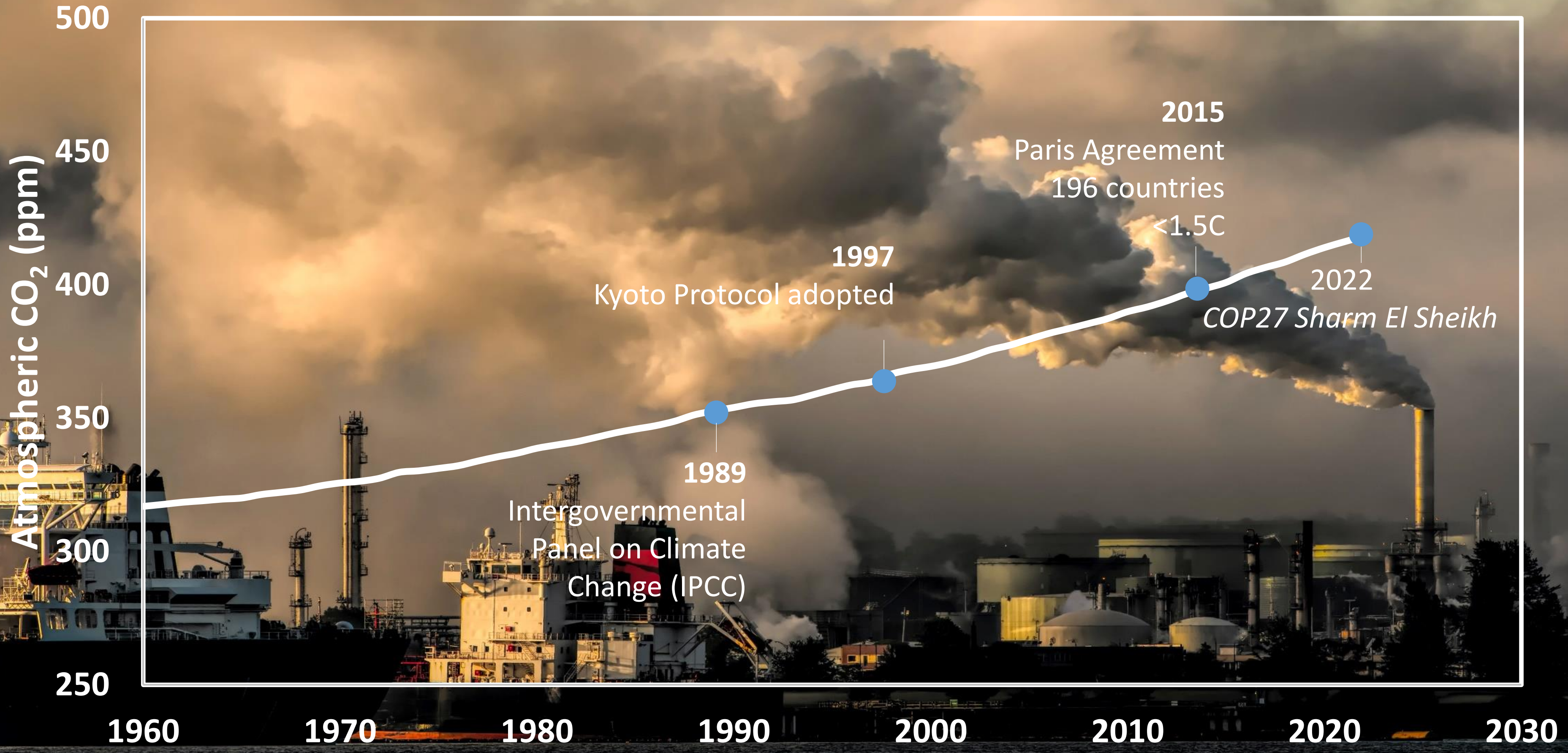
DATE conference, April 17, 2023, 14:40
Workshop 01: Eco-ES: Eco-design and
circular economy of Electronic Systems

CO_2 in the atmosphere increases despite global commitments

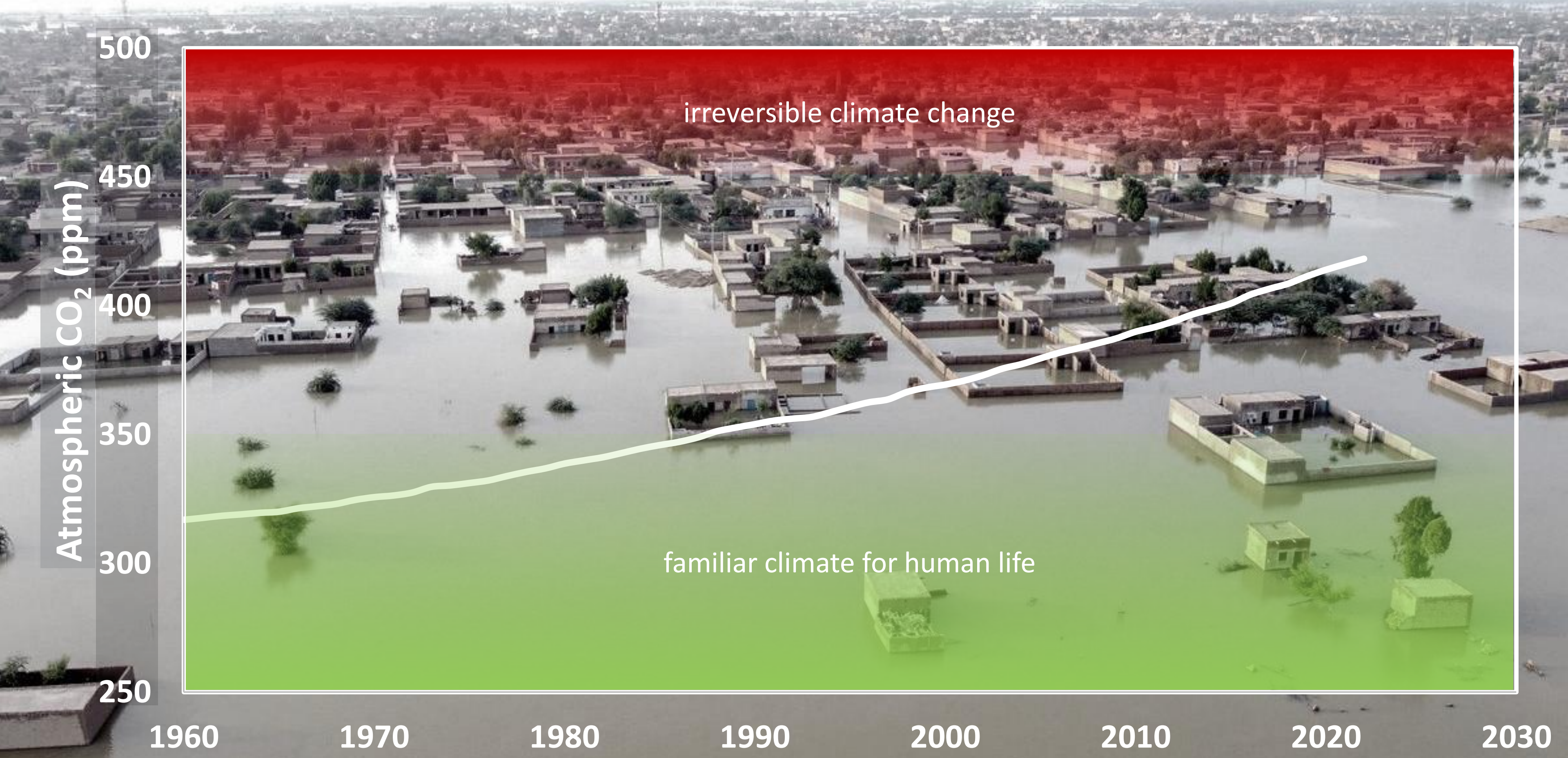


https://www.noaa.gov/news-release/carbon-dioxide-now-more-than-50-higher-than-pre-industrial-levels

Scripps CO2 Program, 2222

Photo by Chris LeBoutillier on Unsplash

Need to address emissions, not simply make commitments



Solomon et al., Irreversible climate change due to carbon dioxide emissions, PNAS 2009

Pakistan giant monsoon, Summer 2022
Photo by Fida Hussain/AFP

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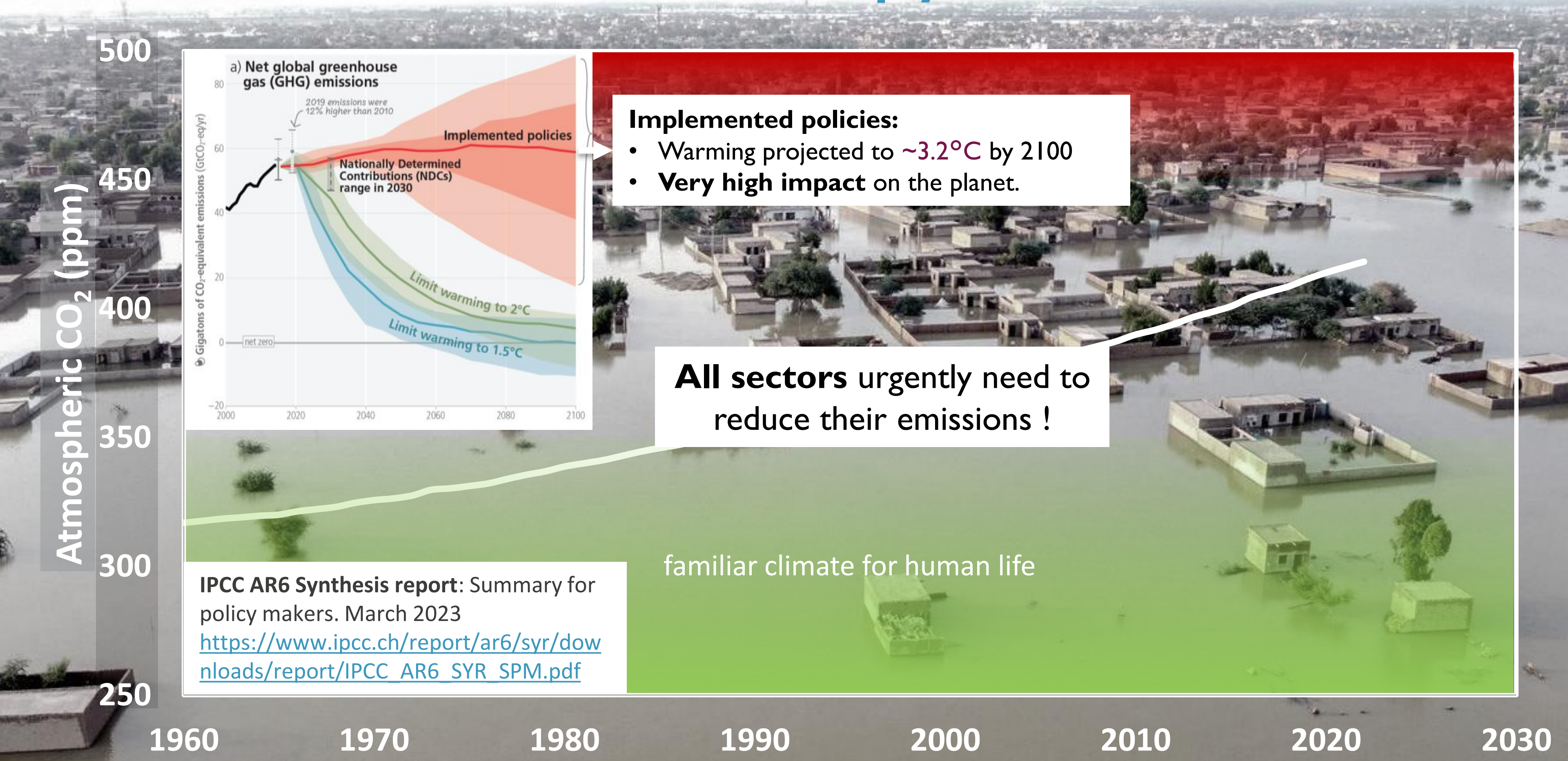

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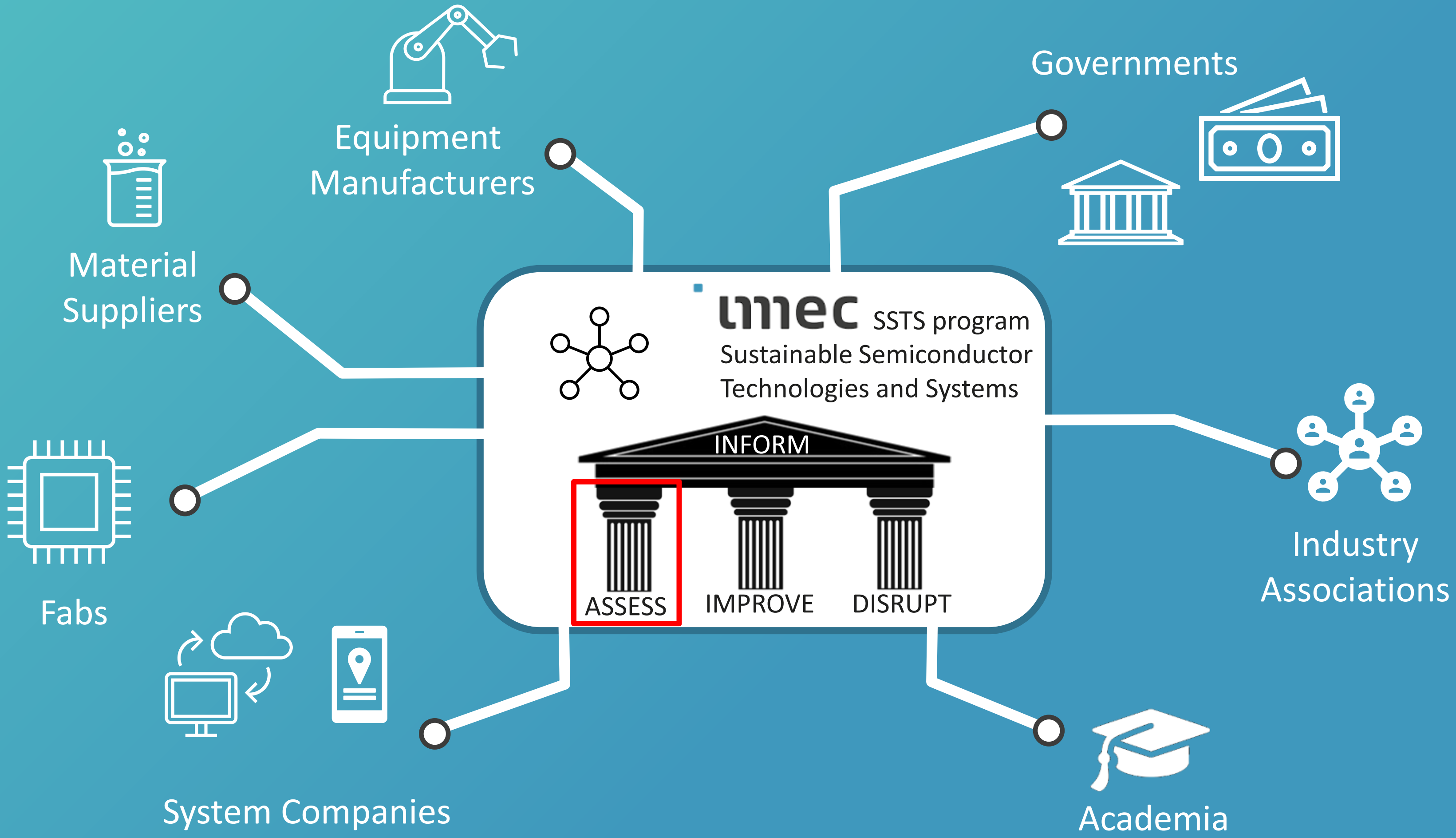
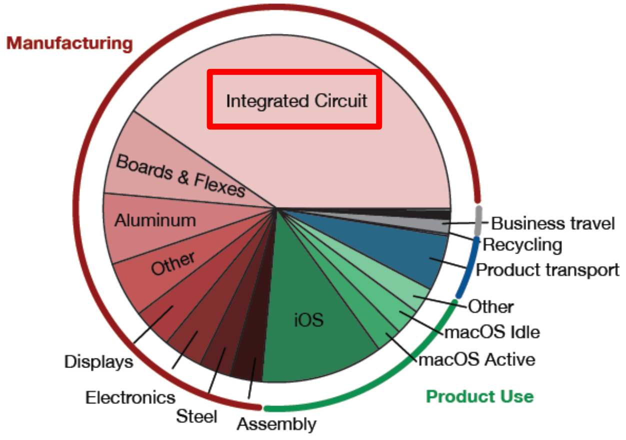
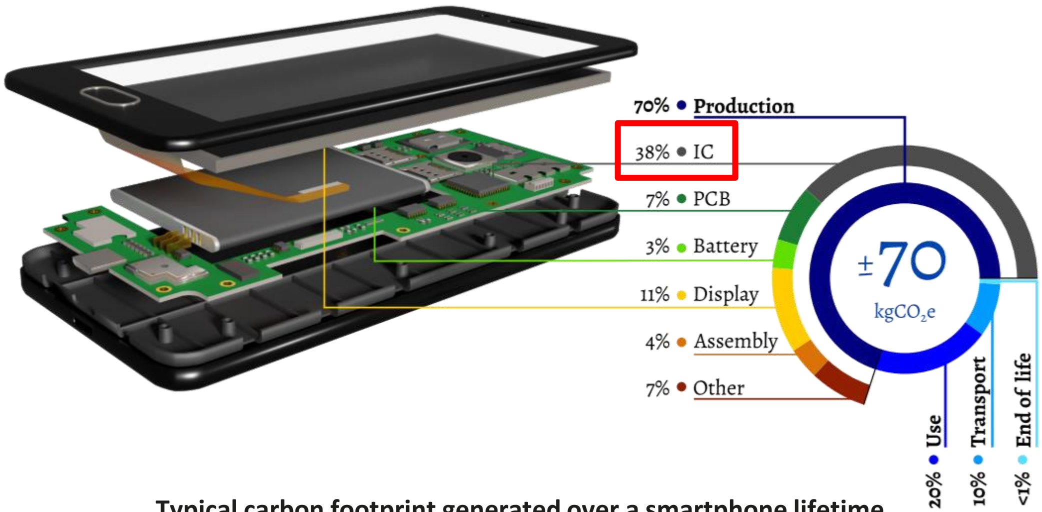


Our mission: Help the semiconductor industry achieve its targets in carbon footprint reduction

The climate impact of Consumer Electronics manufacturing



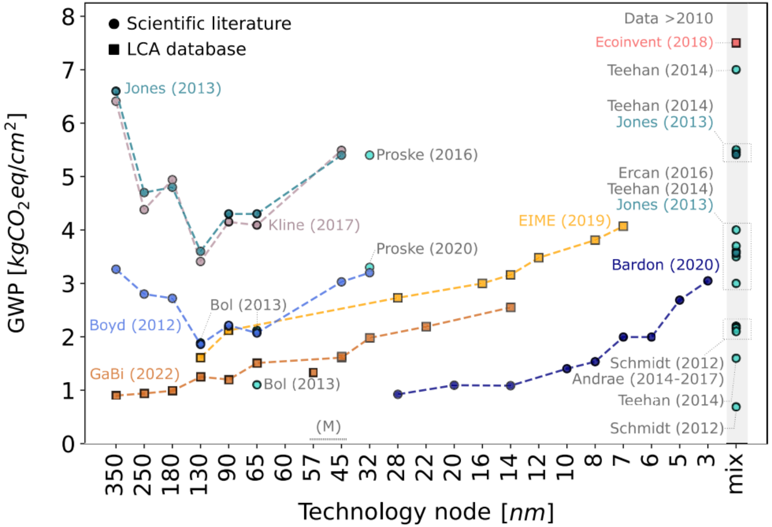
Apple's Carbon-Emission Breakdown
Source: Gupta et al., 2021 –The elusive environmental footprint of computing

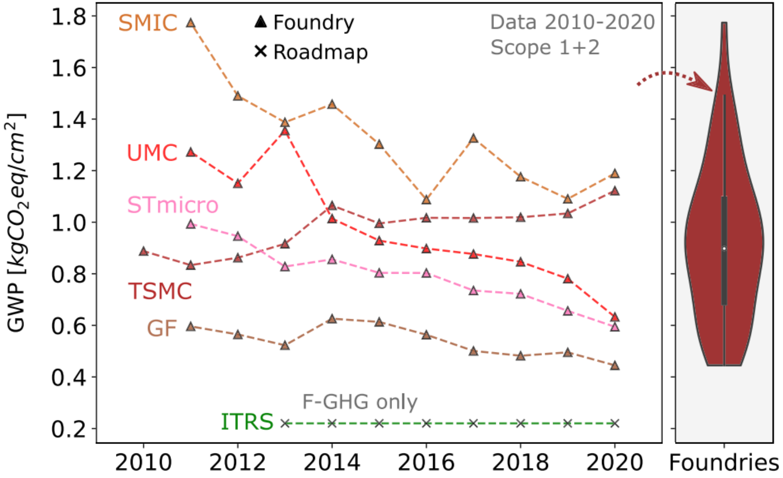


Typical carbon footprint generated over a smartphone lifetime
Source: Moreau et al., 2021 –Could Unsustainable Electronics Support Sustainability?

IC chip manufacturing accounts for the largest share of the climate impact, dominating over product use phase

Scattered data over IC chip manufacturing environmental impact





Literature and LCA database data:

- Variable Scope
- Variable sources (Primary vs. Secondary)
- Variable approaches (e.g. Bottom-up vs Top-down)
- Data gaps require “creative” plugging methods

Industry data from public CSR reports:

- Top-down, primary sourced data
- Aggregated over entire company operation, not “per chip” or “per-node”
- Limited scope
- Non-transparent methodology

Source: Pirson et al., 2023 – The Environmental Footprint of IC Production: Review, Analysis, and Lessons From Historical Trends

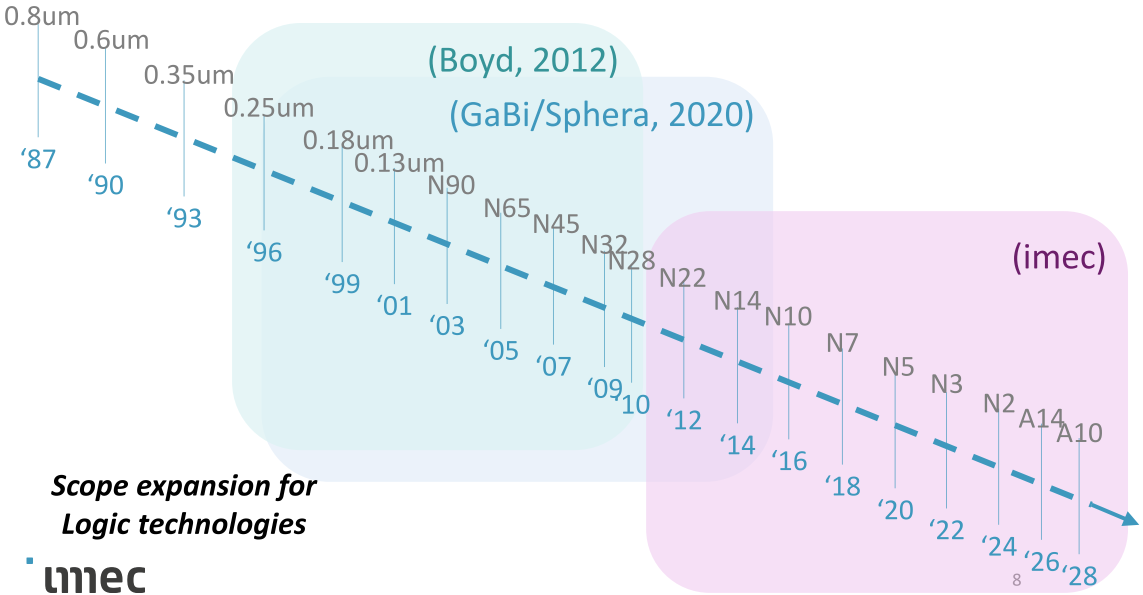
GWP: Global Warming Potential

Imec ambition for the SSTS Assess pillar

Close the data gap by providing **quality, transparent** data on environmental impact of IC chip fabrication in a **generic high volume manufacturing plant**

imec.netzero

a *Virtual Fab* model for environmental impact assessment



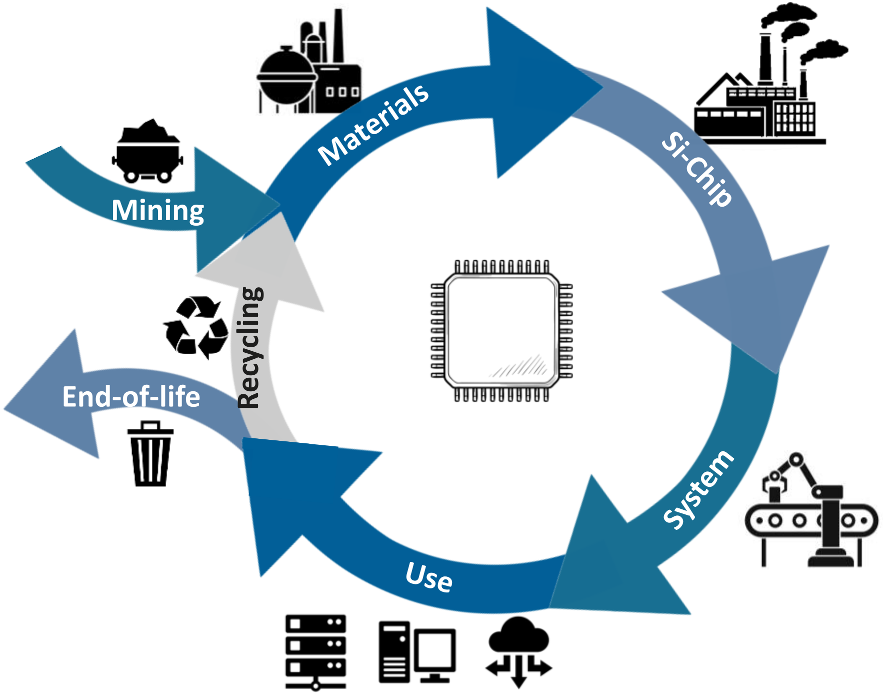
Scope expansion for Logic technologies

Expand the analysis to:

- Identify **high impact** problems to focus Improve efforts
- Project **the future impact of IC chip manufacturing**

The Life-Cycle of a Si-chip

Goal and scope of imec.netzero



- **Product system** – Si chips from HVM
  - Serving several applications (Logic, memory, etc.)
  - Multiple (future) technology nodes
- **Functional Unit**
  - For Manufacturing industry: *"per Wafer"*
  - For IC Chip users:
    - *"per functional die"*
    - *"per functional cm²"*
    - *"per transistor"*
- **Impact categories**
  - Current focus:
    - *Climate Change*
  - Under development:
    - *Abiotic resource depletion*
    - *Water scarcity*

The Life-Cycle of a Si-chip

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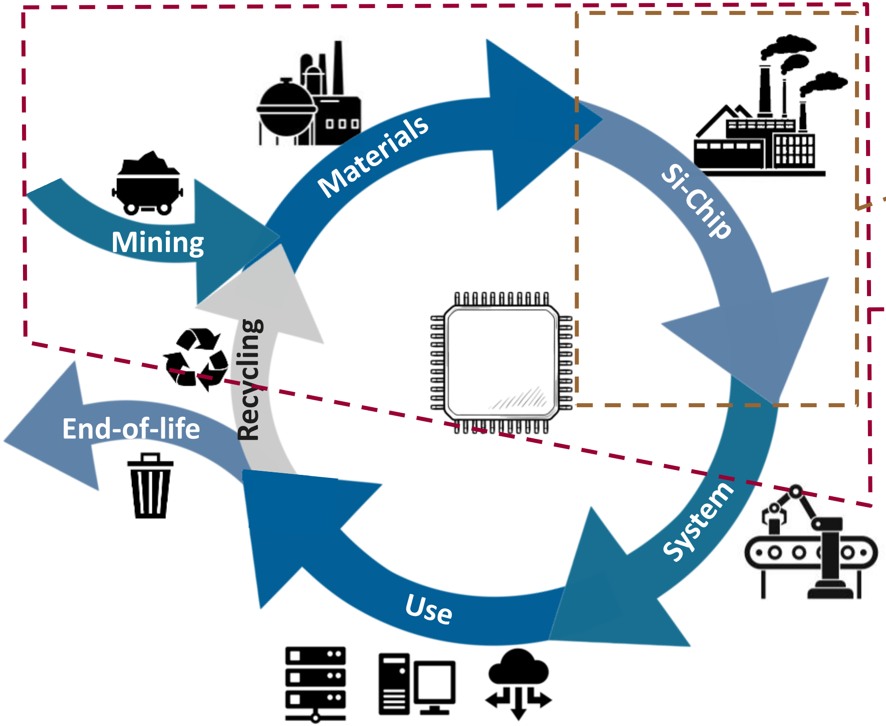
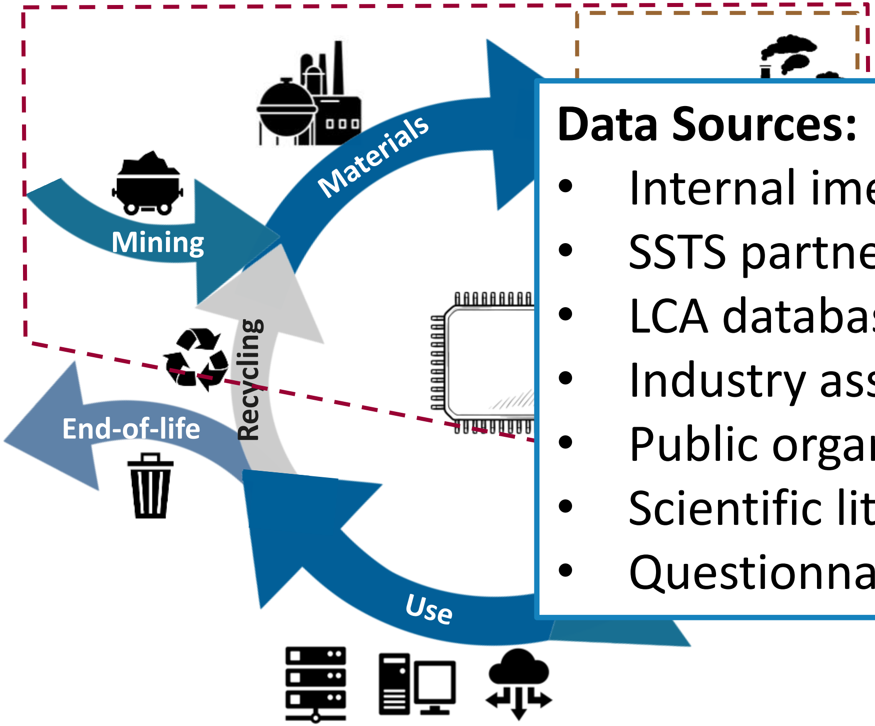


- **System boundaries** – Two sets :
  - Gate-to-Gate semiconductor Fab
    - Mainly PRIMARY data
    - Flow includes: **Process Equipment**, **Utilities** and **Infrastructure** operation
  - Cradle-to-Gate Si-chip manufacturing
    - Adding SECONDARY data
  - **Recycling** considered at Fab level
- **Not included in present analysis**
  - Equipment manufacturing
  - Infrastructure construction

The Life-Cycle of a Si-chip

Goal and scope of imec.netzero



Data Sources:

- Internal imec
- SSTS partners
- LCA databases
- Industry associations: SEMI, ...
- Public organizations: IPCC, IEA, ...
- Scientific literature
- Questionnaire to supply chain

- **System boundaries** – Two sets :

semiconductor Fab

IMARY data

ides: **Process Equipment**,

nd **Infrastructure** operation

e Si-chip manufacturing

CONDARY data

sidered at Fab level

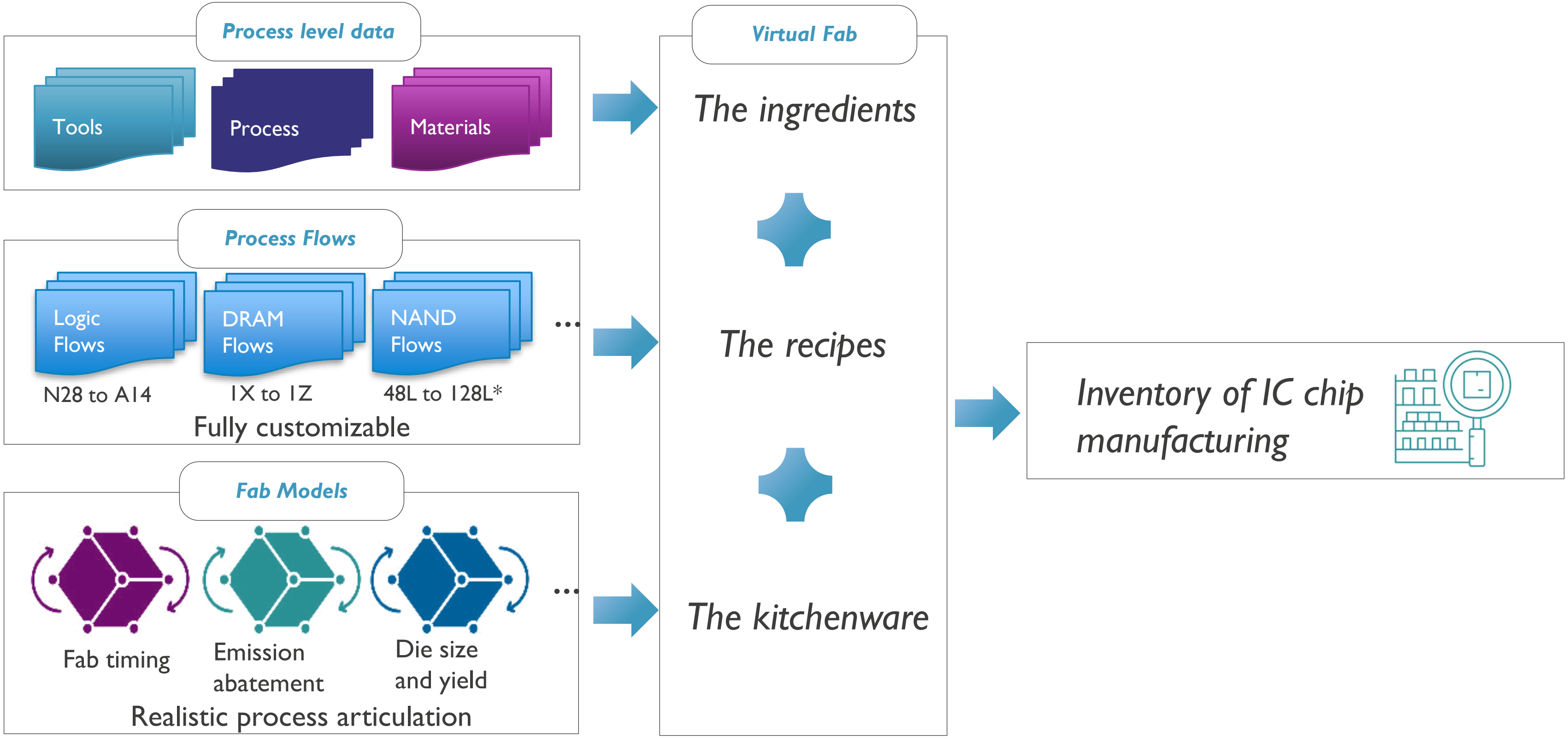
resent analysis

anufacturing

construction

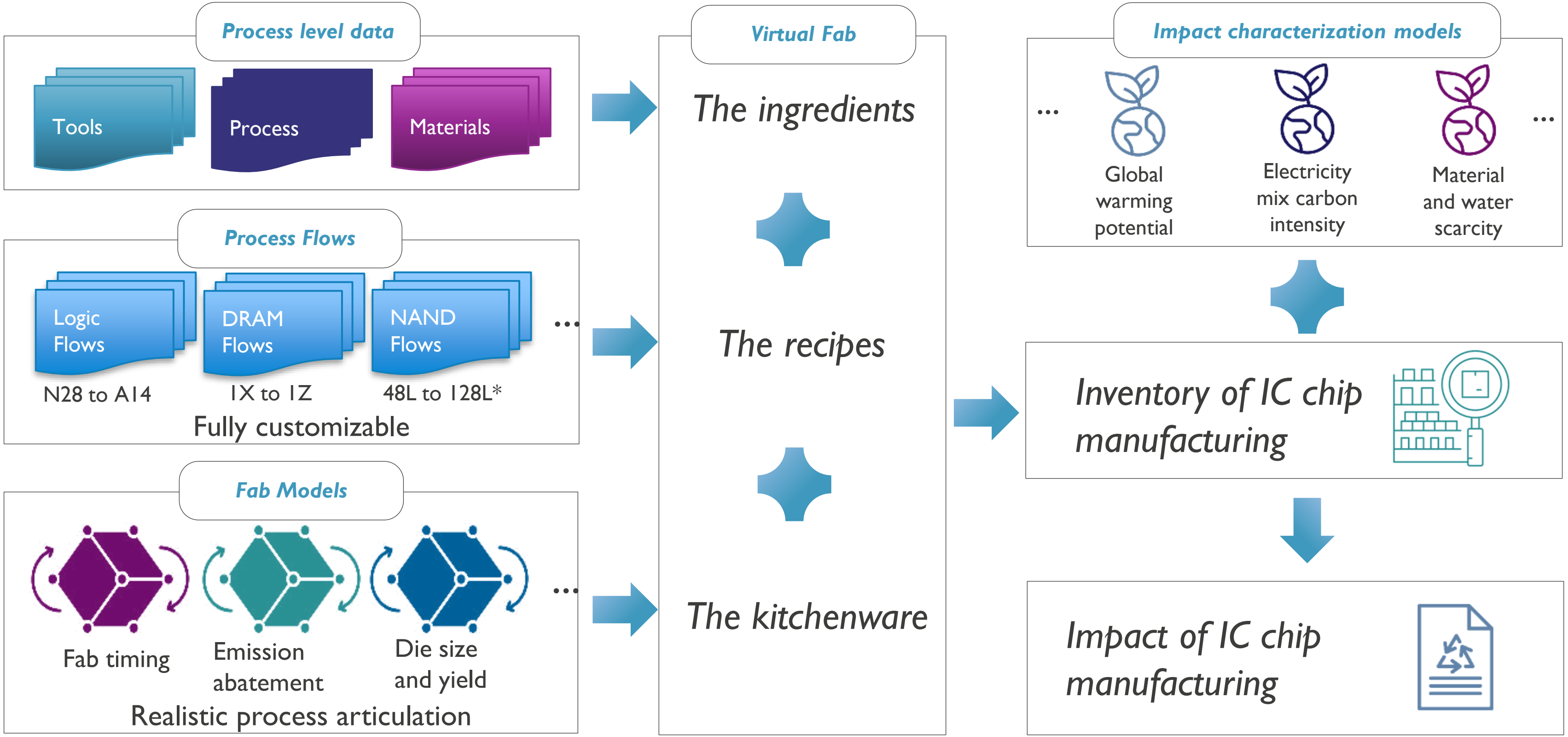
SSTS Assess - Virtual Fab Model

Quantify the footprint of a chip



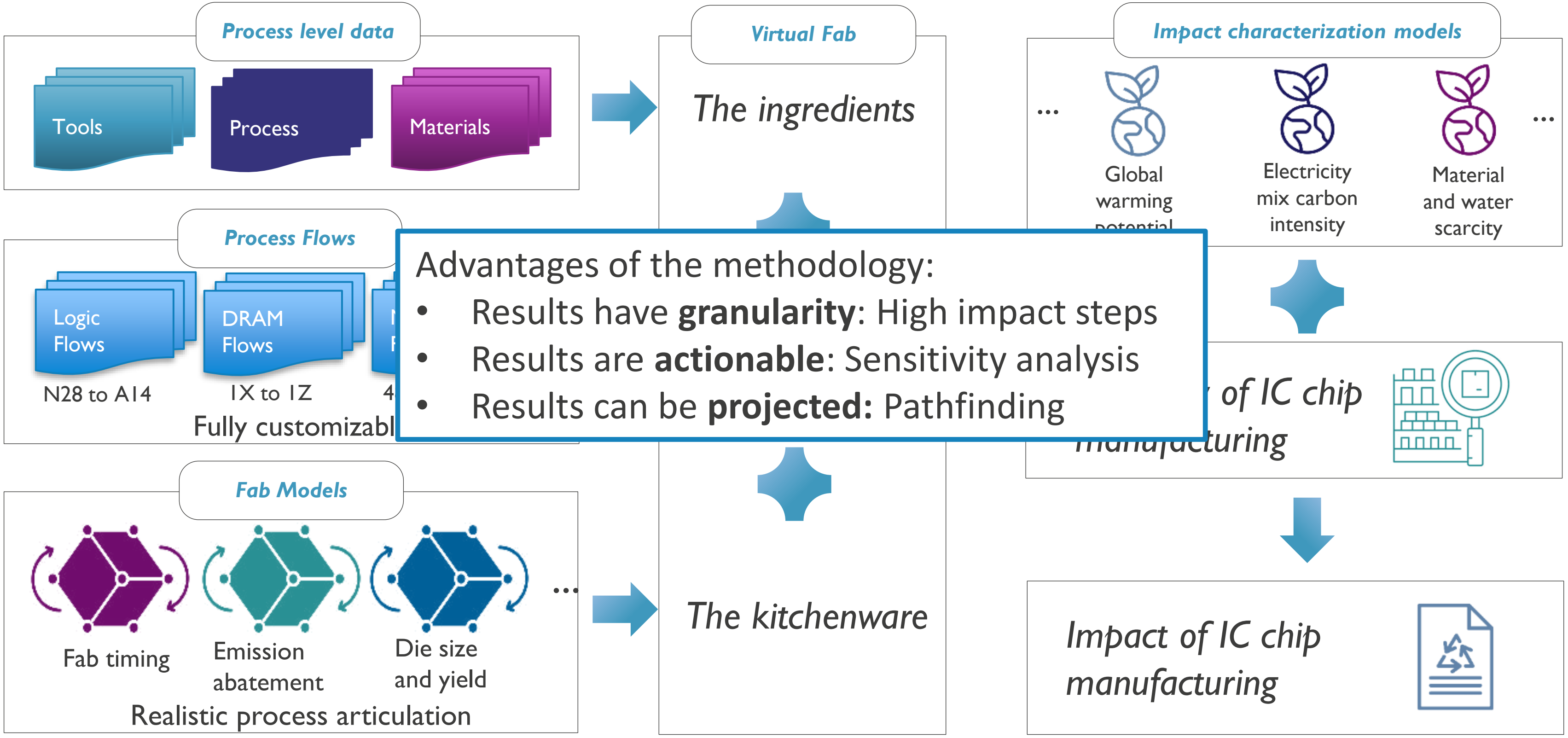
SSTS Assess - Virtual Fab Model

Quantify the footprint of a chip



SSTS Assess - Virtual Fab Model

Quantify the footprint of a chip

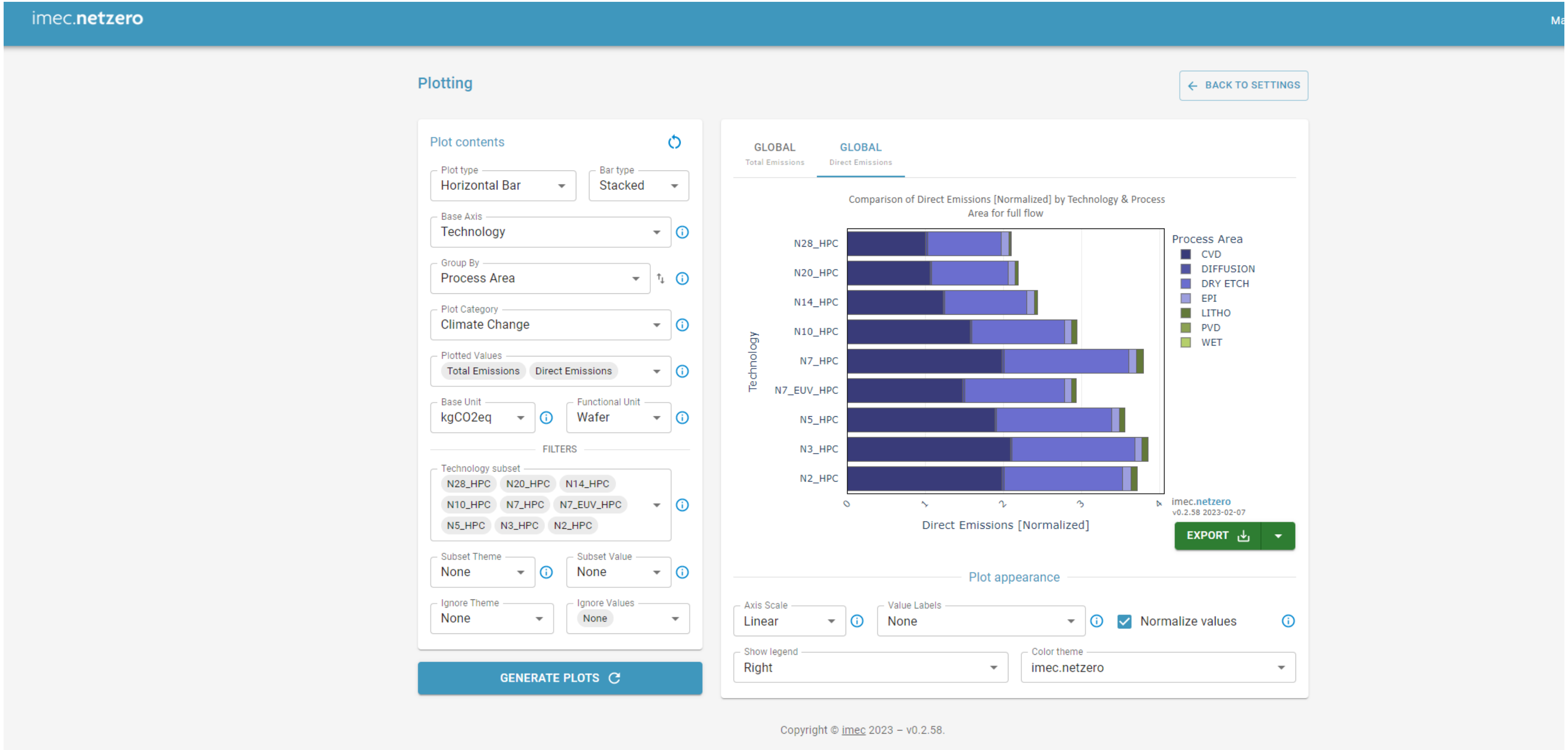


Advantages of the methodology:

- Results have **granularity**: High impact steps
- Results are **actionable**: Sensitivity analysis
- Results can be **projected:** Pathfinding

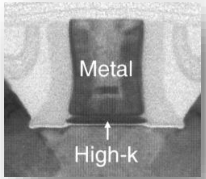
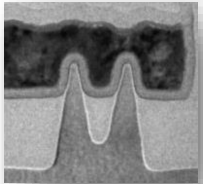
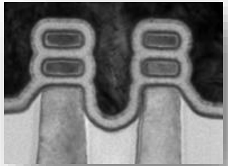
imec.netzero Web Application

Public version release: June 30



Studied Logic CMOS technologies and nodes

In production ← | → Future

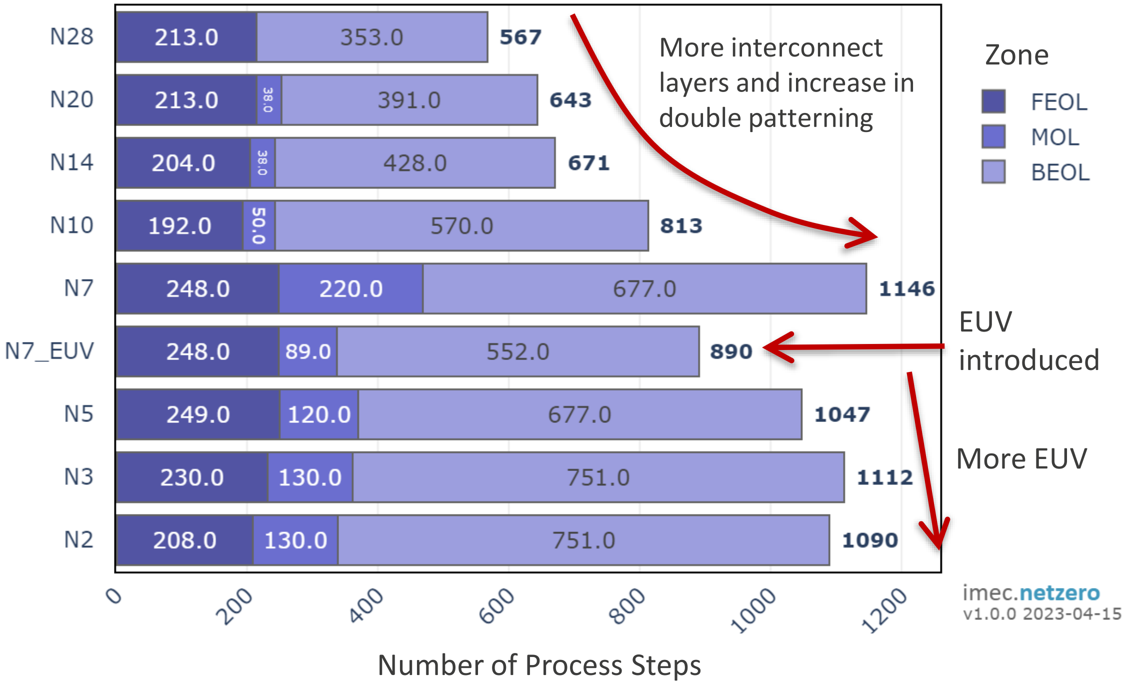
Technology Node	N28	N20	N14	N10	N7	N5	N3	N2	A14
Metal Pitch [nm]	90	64	64	48	40	28	22	21	18
Device structure	 Planar				 FinFETs			 Nanosheets	
Standard cells # tracks	9T	9T	9T	7.5T	6.5T	6T	6T	5T	5T
Scaling boosters					Self Aligned Gate Contact		Metal Gate Cut	Backside power delivery	
Lithography	Immersion (ArFi)								EUV

Nodes based on imec process flow are generic but representative of foundry nodes.

Complexity Increase of a Mobile SoC

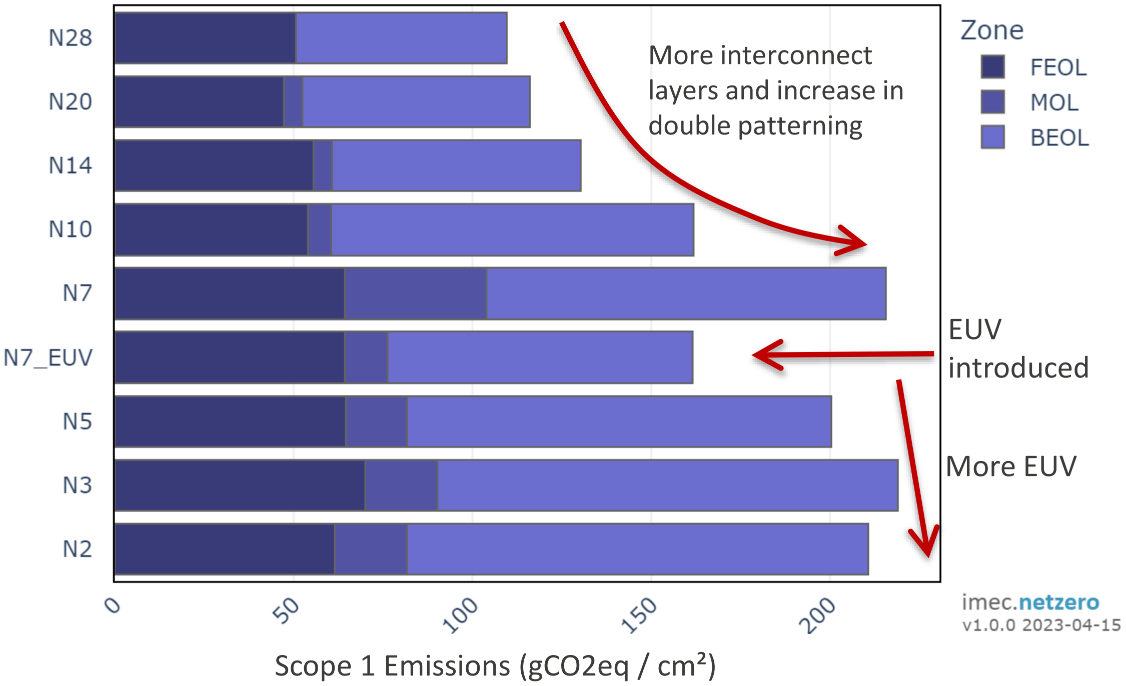
Number of process step evolution per node

- Increase in Complexity node to node where BEOL interconnects dominate
- Introduction of **EUV slows down the increase in complexity**:
  - Less multi-patterning DUV immersion steps
  - Less deposition, Dry-Etch, Wet-Clean, Metrology steps



Direct Emissions (Scope 1)

- Process gases are potent Greenhouse gases => **Deposition and Etch** contribute strongly to direct emissions
- Multi patterning use many repeats of deposition and etch ⇔ **By reducing complexity, EUV keeps direct emissions under check**

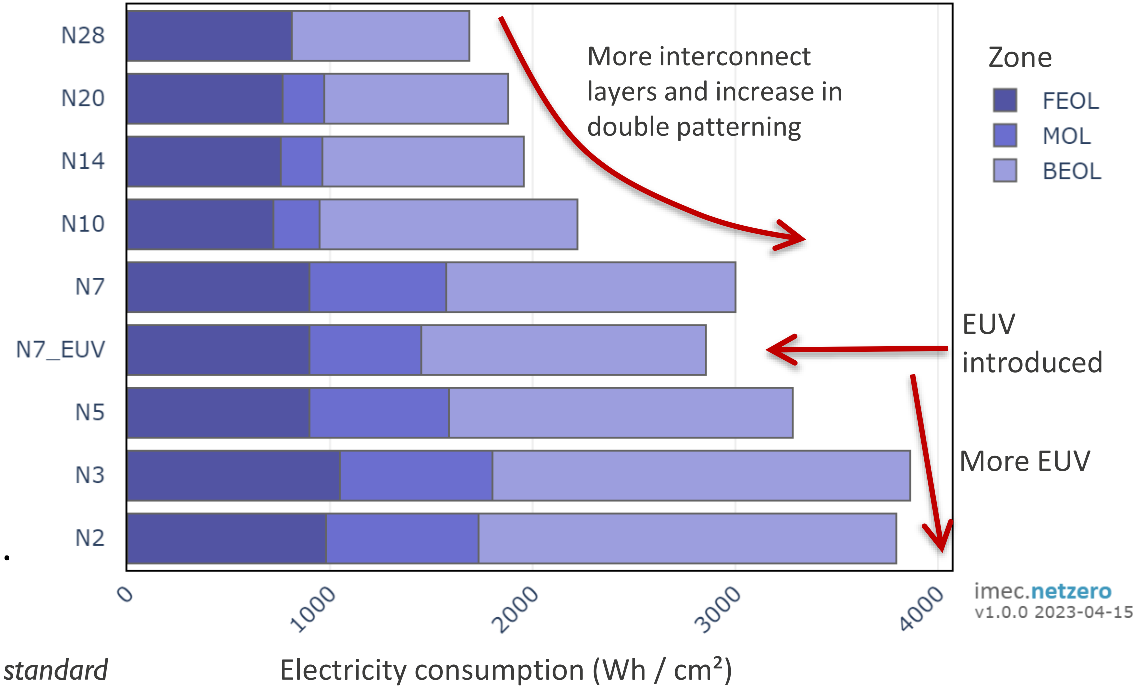


- *10x10mm² die, Murphy yield with 0,15 defect/cm²*
- *Tier 2C Abatement model (2019 Refinement to the 2006 IPCC Guidelines for National Greenhouse Gas Inventories)*
- *GHG global warming potential from IPCC AR6*

Electricity consumption

- Increase in process complexity directly leads to **increased electricity consumption**
- Introduction of EUV leads to:
  - **Reduce in process complexity**
  - **Increased electricity consumption** of the litho process area

These two effect counteract each other leading to a continued increase.



- *10x10mm² die, Murphy yield with 0,15 defect/cm²*
- *Utility electricity consumption modelled using SEMI S23 standard*
- *Tool Utilization assumed using SEMI S23 standard*

Carbon Emissions for Semiconductor Manufacturing are Increasing

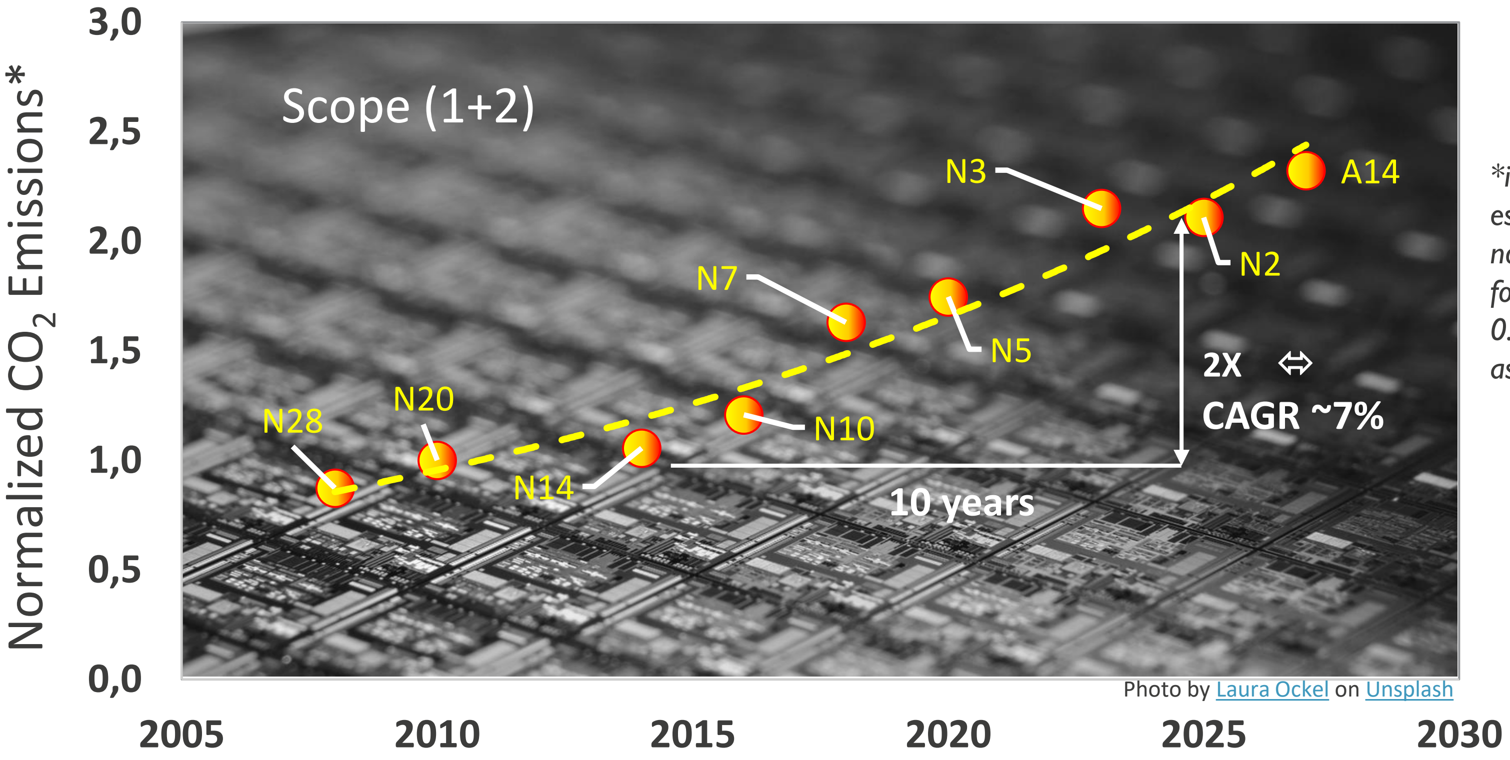
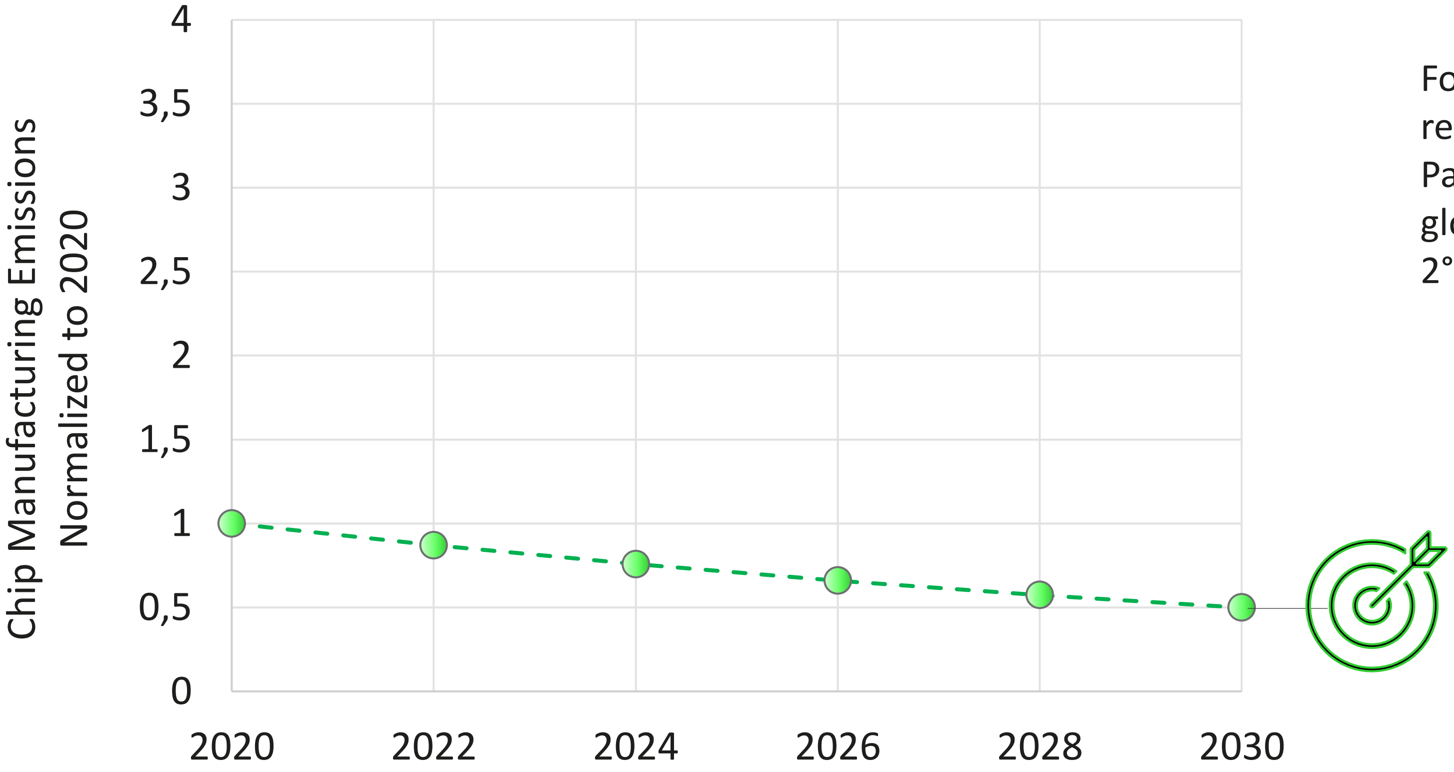


Photo by Laura Ockel on Unsplash

**imec.netzero: emissions estimate of imec process nodes representative of foundry nodes. $0.49 kgCO_2eq/kWh$ assumption for electricity*

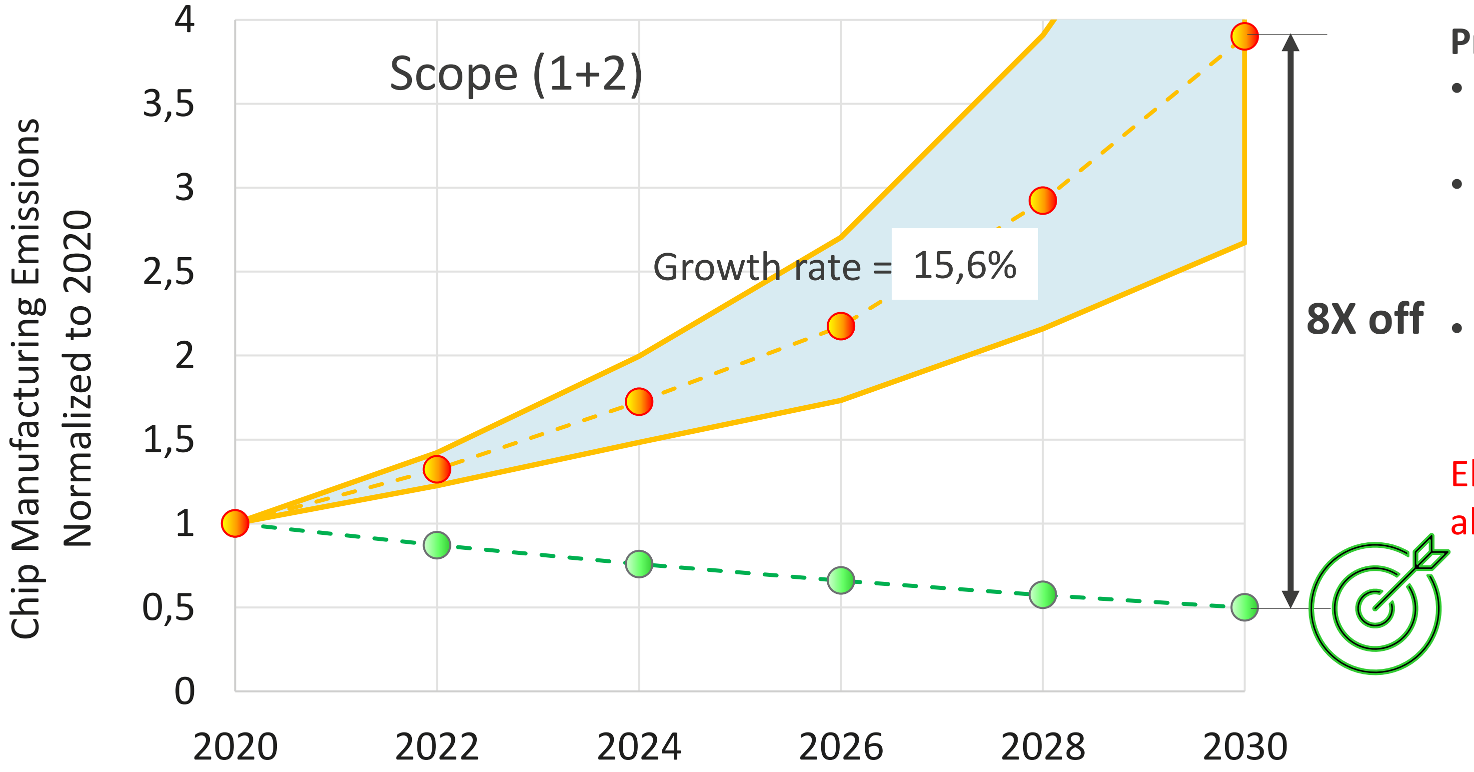
CAGR = Compound Annual Growth

Ideal climate impact scenario for Semiconductor Manufacturing



Following the path recommended by the Paris Agreement to keep global warming under 2°C

“Do Nothing” Scenario for Semiconductor Manufacturing



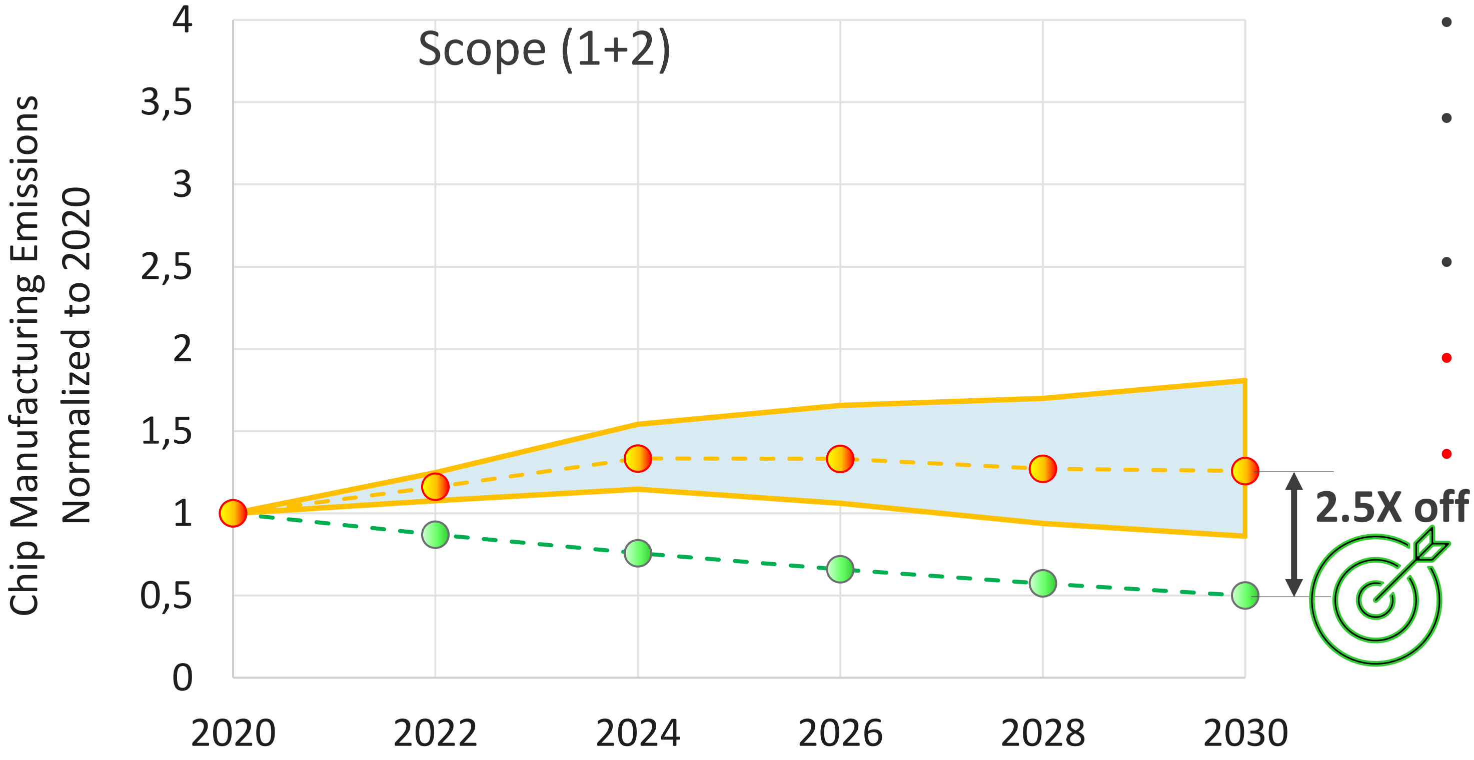
Projection includes:

- Evolution of technology mix
- Increase in technology complexity with CAGR ~7%
- ICT Market growth with CAGR 8% ± 4%

Electricity mix and abatement not evolving.

Constant electricity mix (0.49 kCO2eq/kWh), Tier 2C Abatement (2019 Refinement to the 2006 IPCC Guidelines for National Greenhouse Gas Inventories) and GHG global warming potential (IPCC AR6). Volume technology mix from IBS “Foundry Market Trends and Strategic Implications” Vol 30, N 12 , Dec 2021. Logic nodes only.

With Renewable Energy and State-of-the-Art GHG Abatement



Projection includes:

- Evolution of technology mix
- Increase in technology complexity with CAGR ~7%
- ICT Market growth with CAGR 8% ± 4%
- Renewable energy deployment
- State-of-art abatement from 2026 onwards

Adding to previous slide: Renewable Energy deployment according to IEA and abatement according to IPCC assumed for the years 2020-2024, State-of-the art Abatement from 2026.

Data enables Action across the industry ecosystem

Acknowledgments: The SSTS team and supporters

Many great colleagues across imec organization

- **SSTS Team**
  - Alexander Dockx, Andrea Firrincieli, Benjamin Vanhouche, Bertrand Parvais, Bram Vangestel, Emily Gallagher, Farrukh Yasin, Gioele Mirabelli, I-Yun Liu, Konstantina Filippidou, Laurent Van Winckel, Lizzie Boakes, Marie Garcia Bardon, Nora Maene and Lars-Åke Ragnarsson
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  - Alessio Spessot, Arnaud Furnémont, Frank Holsteyns, Hans Lebon, James Myers, Luca Di Piazza, Sri Samavedam, Tru Lefevere
  - The BD, Legal, ICT, APPM, CMT, FABENG, FAIN and LTE teams
- **SSTS Partners**

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