

Chips&Media's WAVE520 is one of the most advanced hardware video codec IP core supporting next generation High Efficiency Video Coding(HEVC) standard, also known as H.265.

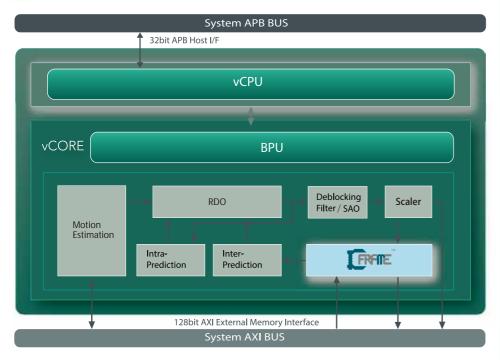
WAVE520 is Chips&Media's 2nd generation video IP, which achieves the best encoding quality at high resolution and frame rate - 4K(3840x2160) 60fps or similar. The required clock frequency for WAVE520 is significantly low, that 380MHz is necessary for decoding, and 500MHz is for encoding. For simultaneous decoding and encoding of 4K resolution, 30fps can be achieved with single IP core.

In addition to its superior high resolution(4K) capabilities, WAVE520 also provides maximum bandwidth efficiency and exceptionally low power consumption, which are today's most demanding requirements across all connected devices. With CFrame™ embedded frame buffer compression technology, memory access bandwidth reduction of 50~70% can be achieved.

WAVE520 is suitable for application across various industry segments including ultra high definition televisions(UHD TVs), UHD camcorders, VR-ARs, drones, automotives, set-top boxes, smartphones, tablets and any other applications or devices with super high resolution.



Block Diagram





Key Features

HEVC/H.265 Hardware Codec

- HEVC Main/Main10 Profile
- 4:2:0 (8-bit/10-bit)
- Brings 50% bitrate savings compared to H.264/AVC

On-the-fly pre/post-processing

- 3DNR for encoding
- Down scaler for decoding

Ideal Solution for Ultra HD Devices

- Enables Ultra HD(4Kx2K) video into home and even on hands
- Maximizes memory bandwidth efficiency by embedding its CFrame[™] technology

Applications

- Digital camcorders/cameras
- Smartphones
- Media tablet PCs
- Desktop & laptop PCs
- Digital TVs
- Digital set-top boxes(STBs)
- Video game consoles
- Blu-ray players
- Automotive infotainment
- VR·AR devices
- Drones

Product Brief WAVE520 I HEVC CODEC HARDWARE IP

Encoding Tools

- Fully Compatible with ISO/IEC 23008-2 HEVC(H.265)
 Main/Main10 Profile L5.1
- Up to 8192x4096 pixel resolution
- Configurable bit-depth of 8-bit/10-bit
- Rate Control
 - CBR and VBR focusing on subjective quality
- IP configurable at compile time
 - B-Frames, bit-depth, RDO complexity
- High performance CABAC engine
- High performance RDO
 - ME ¼-per accuracy with search range of ±128H, ±64V with adaptive search center
 - CU/TU split, transform skip
- Sample Adaptive Offset(SAO) filter
- De-blocking filter
- Mulit-core extension capability
- Low delay coding
- Temporal scalability
- Lossless coding
- 3-Dimensional Noise Reduction
- Smart background detection
- Motion-constrained tiles set support
- Weighted prediction

Decoding Tools

- Fully Compatible with ISO/IEC 23008-2 HEVC(H.265)
 Main/Main10 profile L5.1
- Up to 8192x4096 pixel resolution
- I/P/B picture decoding
- Configurable bit-depth of 8-bit/10-bit
- Coding Unit(CU) sizes from 8x8 to 64x64
- Prediction Unit(PU) sizes from 4x4 to 64x64
- Transform Unit(TU) sizes from 4x4 to 32x32
- Supports all intra prediction sizes and modes
- Supports all inter prediction sizes and modes

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+USA Office+ +Japan Office+

- Advanced motion vector prediction
- High performance CABAC engine
- De-blocking filter
- Sample Adaptive Offset(SAO) filter
- Multi-core extension capability

Performance

- Encoding
 1920x1080p 240fps @ 500MHz
 3840x2160p 60fps @ 500MHz
 3840x2160p 30fps x 2ch. @ 500MHz
- Decoding

 1920x1080p 240fps @ 380MHz
 3840x2160p 60fps @ 380MHz
 3840x2160p 30fps x 2ch. @ 380MHz
 * average clock w/ typical stream
 Required host CPU resource to run : < 1MIPS

CFrame™ for Bandwidth Evolution

- Chips&Media's proprietary technology for bandwidth savings
- Advanced frame buffer compression technology
- Smart 2D cache for motion estimation&compensation to reduce external memory accesses
- Achieves 50~70% bandwidth reduction

Deliverables

- Verilog RTL source code with synthesis scripts
- Testbench with reference C-model
- Detailed technical documents
- Software package
 - Firmware
 - API reference software
 - Android and Linux OpenMAX support for hardware codec

Interfaces

- 32-bit AMBA3 APB bus
- 128-bit AMBA3 AXI buses







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