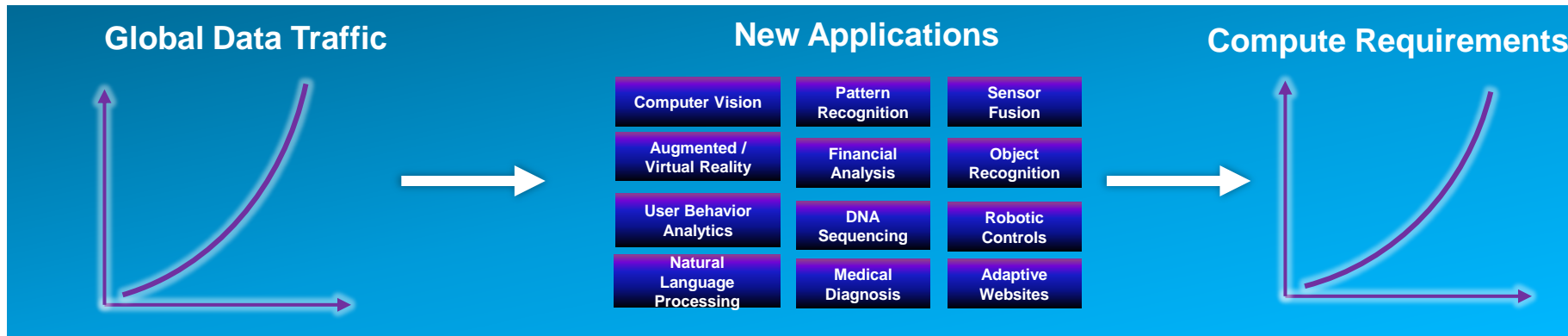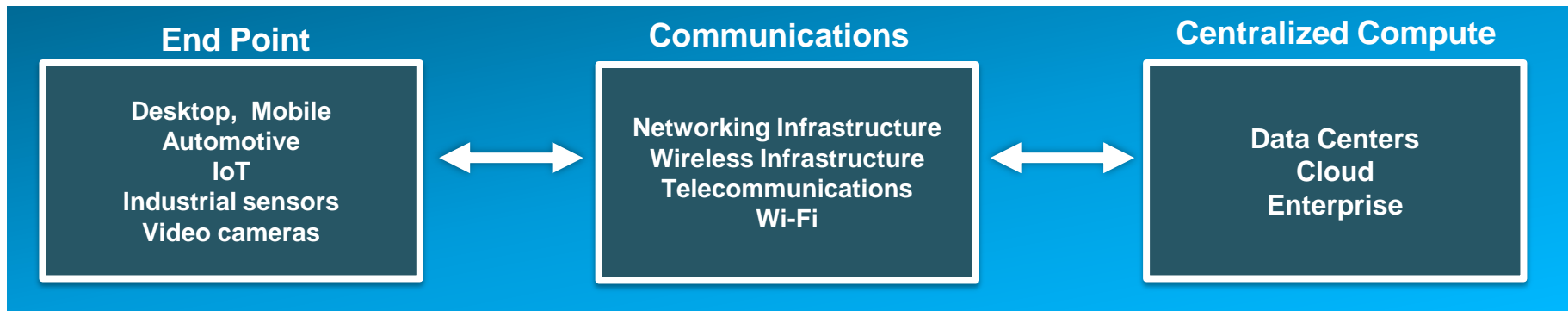# eFPGAs – Revolutionizing the High Performance Computing Landscape

**Eric Law**
**Director, Asia-Pacific Sales**
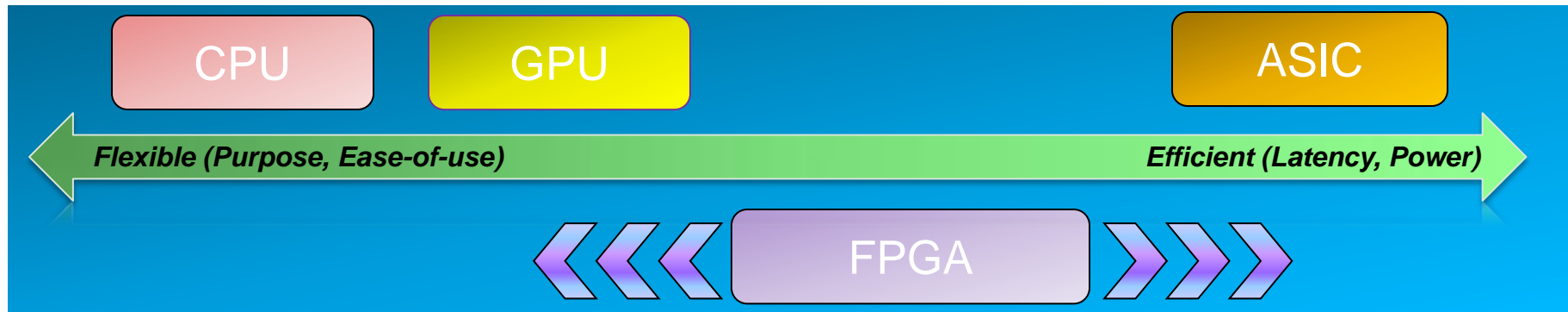**September 14th, 2017**

# Agenda

- The Compute Challenge and the Accelerator Spectrum

- eFPGA vs. FPGA for Hardware Acceleration

- Compute Acceleration with Speedcore eFPGA

- Standard Atomic Building Blocks

- ACE Design Tool

- Achronix Hardware Accelerator FPGA-Based Product Lines

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# The Compute Challenge

## End Point

**Desktop, Mobile**
**Automotive**
**IoT**
**Industrial sensors**
**Video cameras**

## Communications

**Networking Infrastructure**
**Wireless Infrastructure**
**Telecommunications**
**Wi-Fi**

## Centralized Compute

**Data Centers**
**Cloud**
**Enterprise**

## Global Data Traffic

## New Applications

| | | |
|---|---|---|
| Computer Vision | Pattern Recognition | Sensor Fusion |
| Augmented / Virtual Reality | Financial Analysis | Object Recognition |
| User Behavior Analytics | DNA Sequencing | Robotic Controls |
| Natural Language Processing | Medical Diagnosis | Adaptive Websites |

## Compute Requirements

# Accelerator Spectrum



- **CPU**
  - Lots of flexibility, easy to program
  - Slow compared to the other options
- **GPU**
  - Less flexible - can't run general purpose programs
  - Lots and lots of processors.
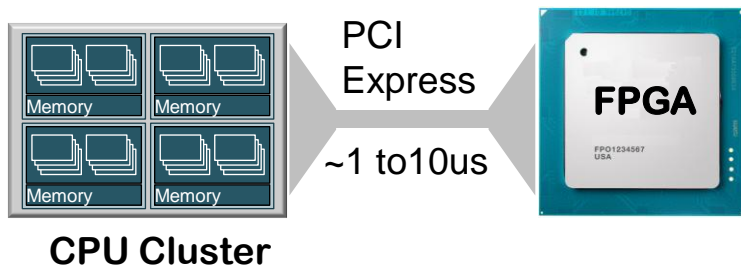  - Pretty flexible, very power hungry.
- **ASIC**
  - Burn algorithms into silicon.
  - No flexibility, but no wasted time or energy on anything superfluous.
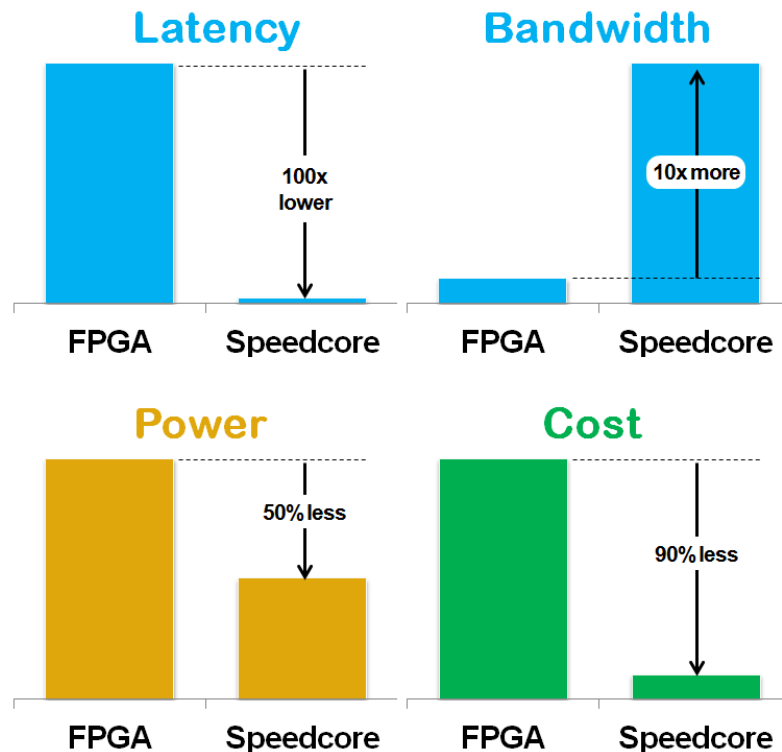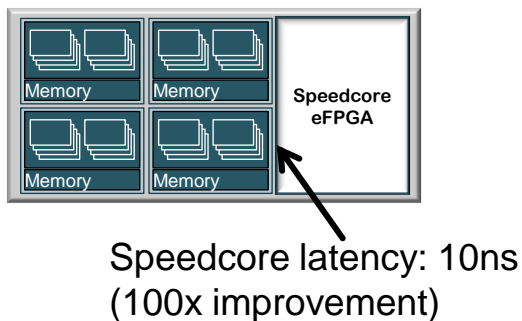
- **FPGA**
  - Flexibility of an CPU with ASIC-like efficiency and performance.
  - Very low power per operation vs. CPU or GPU
  - Reprogrammed to implement different algorithms in "hardware".
  - Made of Look-Up-Tables (LUTs) & Registers, SRAMS, DSPs, and other special purpose blocks.

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# eFPGA vs. FPGA for Hardware Acceleration

## FPGA Based Accelerator

Memory  Memory
Memory  Memory

**CPU Cluster**

PCI Express
~1 to10us

FPGA
FPO1234567
USA

## eFPGA Based Accelerator

Memory  Memory
Memory  Memory
Speedcore eFPGA

Speedcore latency: 10ns
(100x improvement)

### Latency
FPGA    Speedcore
100x lower

### Bandwidth
FPGA    Speedcore
10x more

### Power
FPGA    Speedcore
50% less

### Cost
FPGA    Speedcore
90% less

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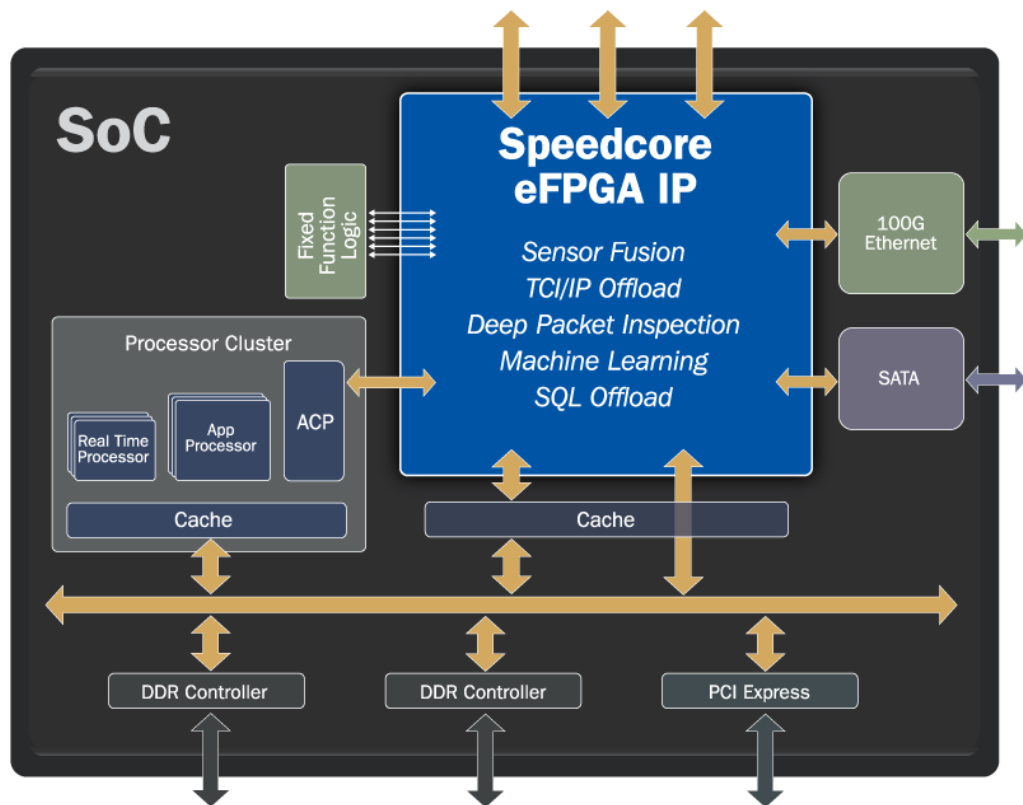
# Achronix Speedcore eFPGA IP

- Speedcore is an eFPGA IP for integration in ASIC / SoCs

- In production on TSMC 16nm
  - In development on TSMC 7nm

- Supported by Achronix ACE design tools

- Resource sizing defined by IP customer
  - Up to 1M LUTs
  - Speeds up to 500 MHz



SoC

Fixed Function Logic

**Speedcore eFPGA IP**

*Sensor Fusion*
*TCI/IP Offload*
*Deep Packet Inspection*
*Machine Learning*
*SQL Offload*

100G Ethernet

SATA

Processor Cluster

Real Time Processor

App Processor

ACP

Cache

Cache

DDR Controller

DDR Controller

PCI Express

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# Compute Acceleration with Speedcore

- **High throughput** **Programmable Acceleration**
  - 2x 128b interfaces @ 600 MHz: **_153 Gb/s_**
  - Any combination of masters and slaves.
  - As many interfaces as you need.
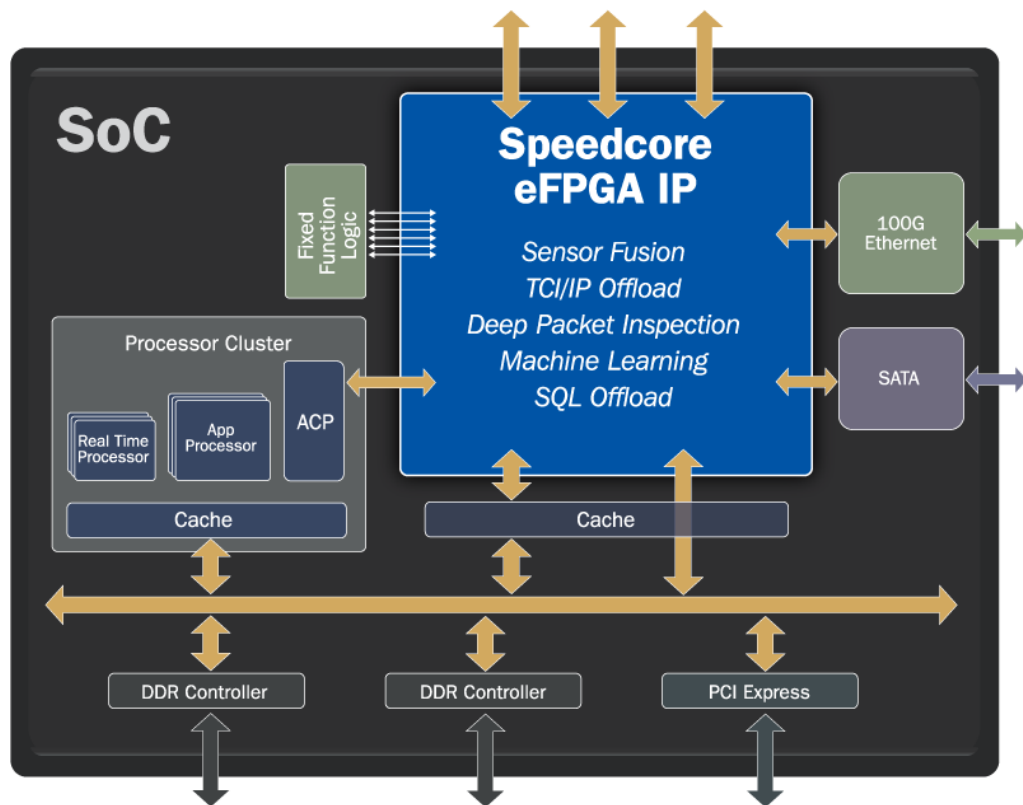
- **Low latency** **Programmable Acceleration**
  - Latency (round-trip) @ 600 MHz: ~**_10 ns_**.

- **Coherent** **Programmable Acceleration**
  - Simplified and safe software programming
  - Cache Stashing allows the FPGA to work with any layer of cache, from any CPU.

- **AXI/ACE-Lite Interfaces**
  - Integrates like any other SOC IP core.



**SoC**

**Speedcore eFPGA IP**

*Sensor Fusion*
*TCI/IP Offload*
*Deep Packet Inspection*
*Machine Learning*
*SQL Offload*

Fixed Function Logic

100G Ethernet

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Processor Cluster

Real Time Processor

App Processor

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Cache

Cache

DDR Controller

DDR Controller

PCI Express

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# Compute Acceleration with Speedcore

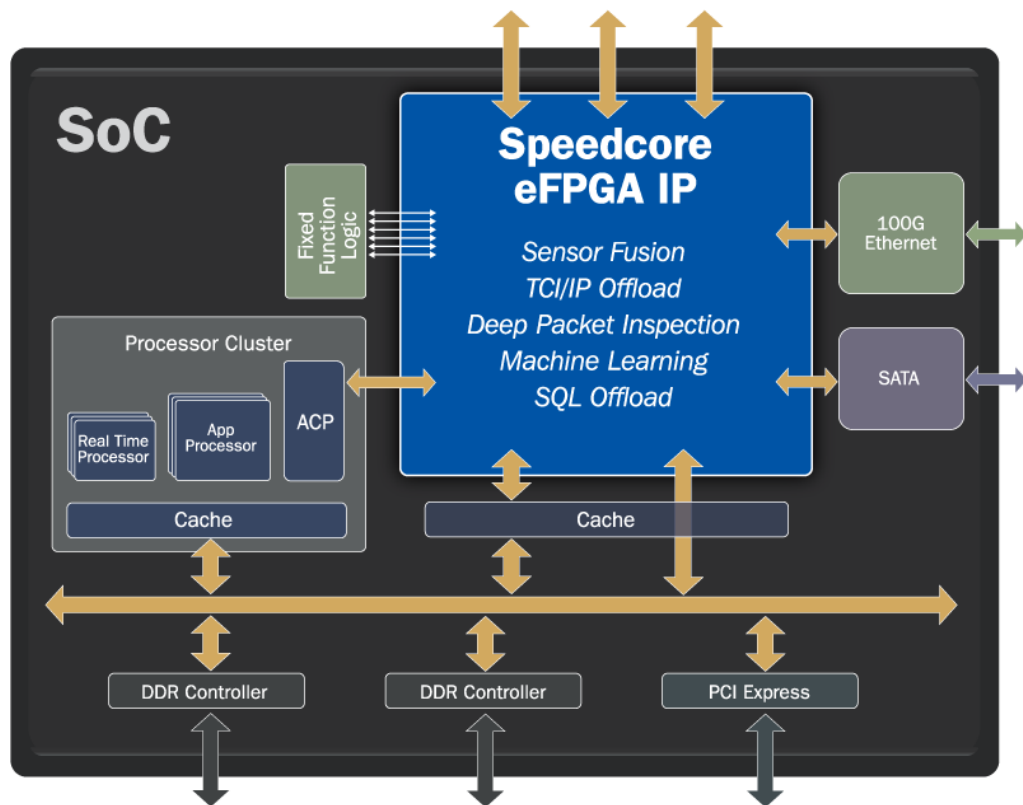- **Accelerator Coherency Port (ACP)**
  - The Speedcore Accelerator can access the system memory via L2 & L3 Cache.
  - Extremely low-latency:
    - Get inputs directly from CPU cache.
    - Returns results directly to CPU cache.

- **Configuration**
  - Speedcore internal half-DMA: pulls configuration from memory with minimal CPU involvement.
  - Extremely fast: **~2ms per 100k LUTs.**
  - On-die configuration is inherently more secure than interchip configuration.

- **Trustzone**
  - FPGA accesses memory (or other peripherals) via the Trustzone controller.
    - An untrusted configuration cannot see trusted data.



**SoC**

**Speedcore eFPGA IP**

*Sensor Fusion*
*TCI/IP Offload*
*Deep Packet Inspection*
*Machine Learning*
*SQL Offload*

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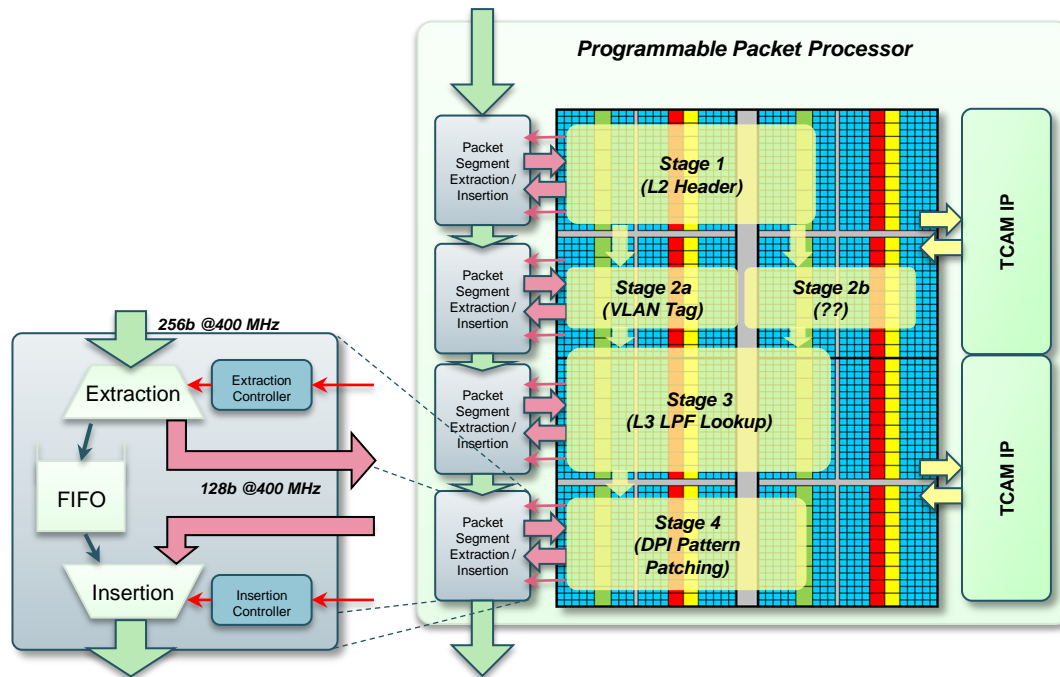
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# 100 Gbps Programmable Packet Processing

- Speedcore allows you to segment the design into hard vs. programmable blocks at a fine-grain level.
  - Increase performance while reducing area.

Example: 100 Gbps programmable packet processing

- FPGA Stage 1 tells extraction controller what to be extracted
  - E.g. L2 Header

- FPGA Stage 1 receives requested data via 128b interface

- FPGA Stage 1 Processes the packet header
  - E.g. MAC Address TCAM lookup

- FPGA Stage 1 Inserts sideband or inline data via 128b interface

- FPGA Stage 1 provides "insertion instruction".
  - Where to insert, drop, etc.

- FPGA Stage1 can forward control information directly to FPGA Stage 2
  - Within FPGA



**Programmable Packet Processor**

Packet Segment Extraction / Insertion

Stage 1 (L2 Header)

Stage 2a (VLAN Tag)  Stage 2b (??)

Stage 3 (L3 LPF Lookup)

Stage 4 (DPI Pattern Patching)

TCAM IP

TCAM IP

256b @400 MHz

Extraction

Extraction Controller

FIFO

128b @400 MHz

Insertion

Insertion Controller

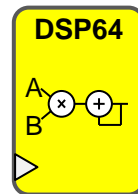achronix
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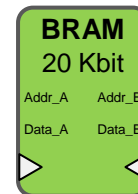
# Standard Atomic Building Blocks

- Standard FPGA blocks
  - Logic
  - DSP
  - Memory
- Structured in column based format
- Complete permutability for column locations

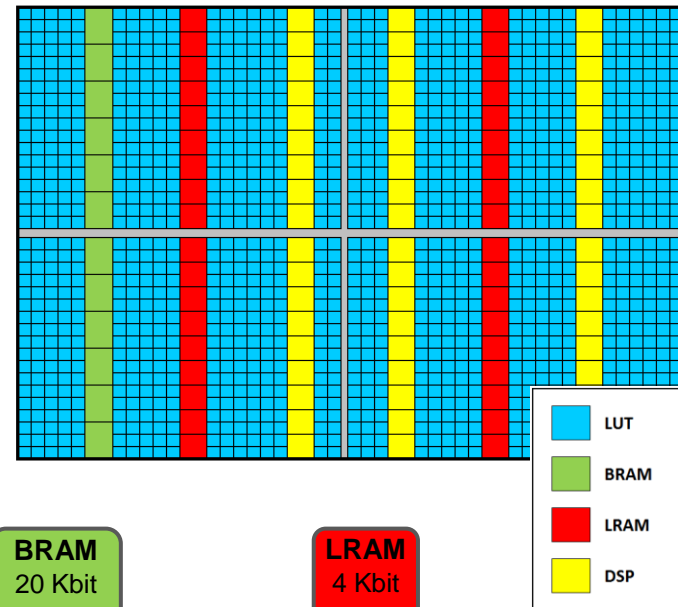**Logic**
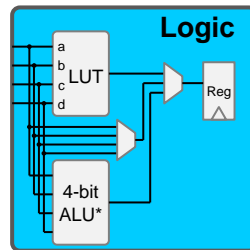
- 4-input LUT
- Dedicated wide muxes
- 4-bit ALU (per 4 LUTs)

**DSP64**

- 27x18
- 64-bit ACC

**BRAM**
**20 Kbit**

- 20 Kbit
- True dual-port

**LRAM**
**4 Kbit**

- 4 Kbit
- Simple dual-port

LUT
BRAM
LRAM
DSP

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# Achronix Speedcore eFPGA Compiler:
# Fast Development of Customer Specific Speedcore IP

## Inputs

## Deliverables



**IP Deliverables:**
- GDSII
- Simulation files
- SI and PI models
- Test models
- Timing characterization
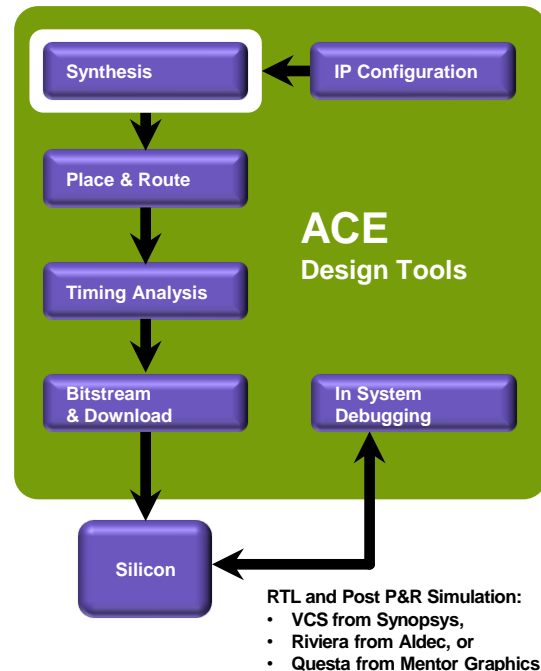- Documentation

**Full Support in ACE Design Tools**

# ACE Design Tools and Supported Features

ACE Design Tools loaded with features:

- Full RTL Verilog, SystemVerilog and RTL support
- Full-fledged STA supporting CRPR, OCV derating, multiple corners
- TCL command language
- GUI and command-line control
- Highly efficient integrated data model
- Supports all current simulators: Synopsys VCS, Mentor QuestaSim, Aldec Riviera, Cadence Incisive.
- Linux and Windows support
- Node locked and network licensing models
- Protected/encrypted IP support

*Production Version 6.0.4*
*Available Now*

**SYNOPSYS®**

**Synplify-Pro from Synopsys**
**Supplied by Achronix**

Synthesis ← IP Configuration

↓

Place & Route

↓

Timing Analysis

↓

Bitstream & Download

In System Debugging

**ACE**
**Design Tools**

Silicon

**RTL and Post P&R Simulation:**
- **VCS from Synopsys,**
- **Riviera from Aldec, or**
- **Questa from Mentor Graphics**

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# ACE Design Suite



**Project Setup & Compile**

**FPGA Program & Snapshot Debug**

**Floorplanning & Placement**
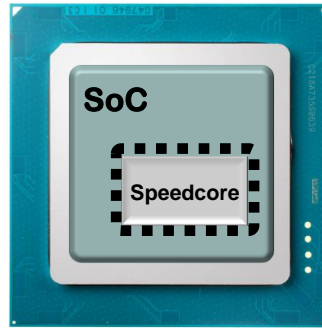
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# Achronix Hardware Accelerator FPGA-Based Product Lines
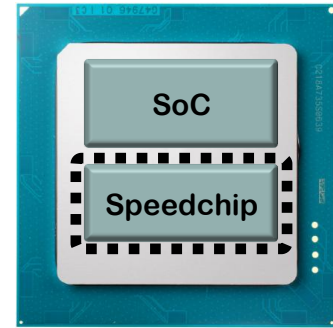
## Speedster



- Standalone FPGAs
- High-performance
- High-density
- For targeted applications

## Speedcore



- Embedded FPGA Cores
- High-performance
- Customized per application

## Speedchip



- FPGA Chiplets
- 2.5D or MCM integration
- Customized per application

## ACE Design Tools

**Synthesis – Verification – Timing – Programming – Debug**

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# Summary

- **Smaller, faster and programmable**
  - FPGAs are critical to meet tomorrow's compute requirements,

- **Embedding FPGA functionality no more a distant dream!**
  - Start exploiting the full functionality and benefits of an FPGA inside an SoC as a hard IP.

- **eFPGA IP has to be silicon-proven!**
  - Achronix Speedcore eFPGA based on the same high-performance architecture that is in Achronix's Speedster 22i FPGAs which have been shipping in production since 2013.
  - Speedcore eFPGA products are fully supported by Achronix's robust and proven ACE design tools.