Building flexible SoCs

Shanghai, China

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Flexible Trusted eFPGA

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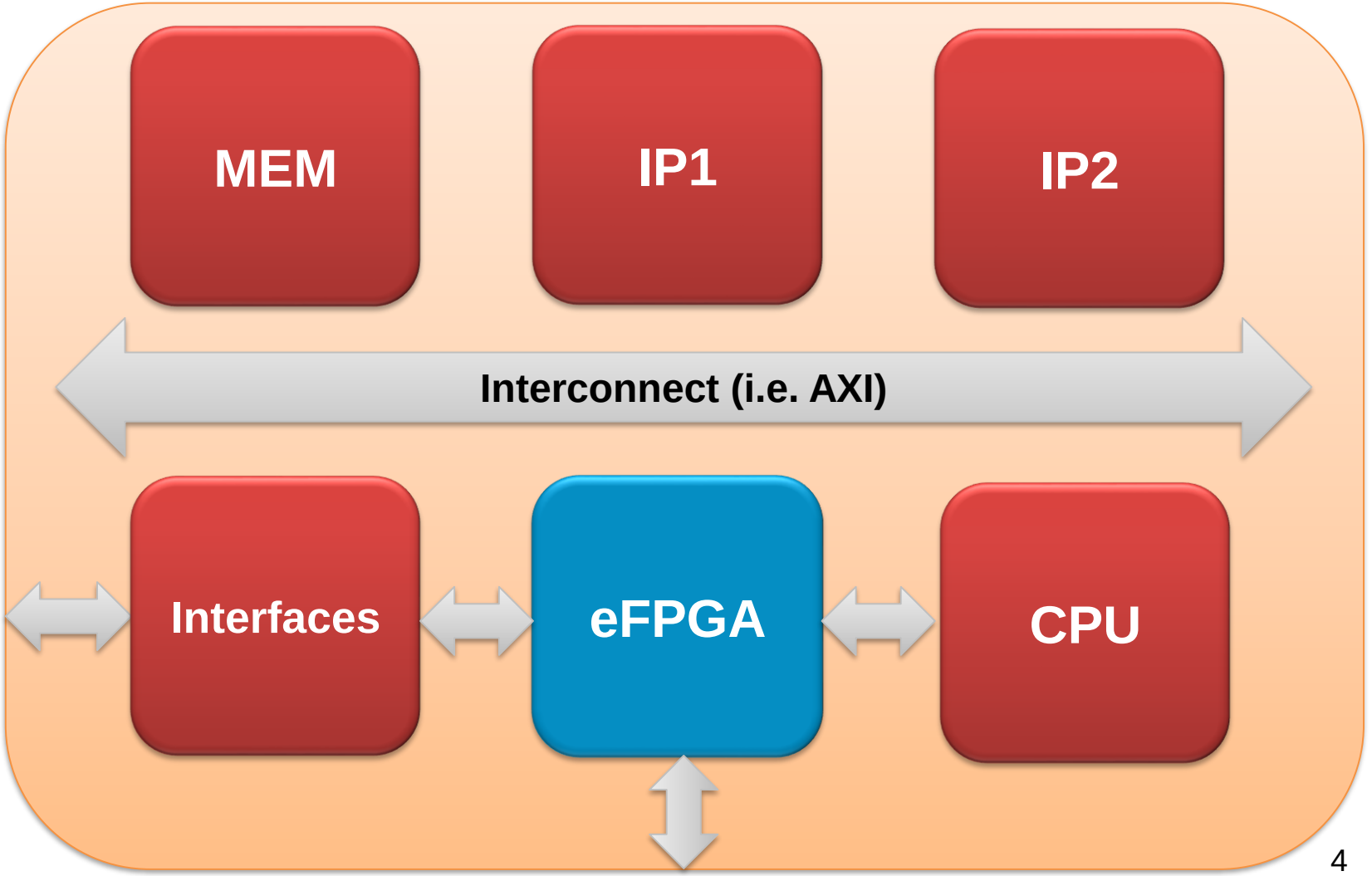
Technical Interface Director

Company

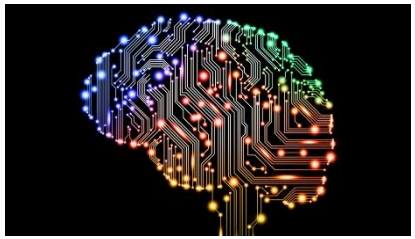
- HeadQuarter: France
- 10 years company
- Only focus on eFPGA
- Patented technology
- Silicon on different foundries and nodes
- Customers
- China commercial: Jiatao
- Staff of 15 people
  - Currently hiring (6 open positions)
- Capital: 7M$

System On Chip with eFPGA

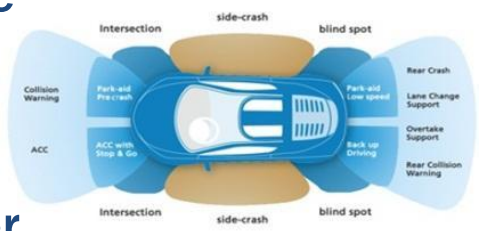


eFPGA application scenarios

- Co-processor:
  - AI

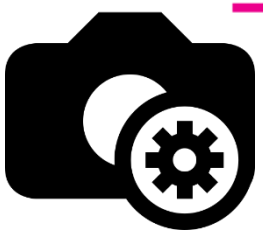


  - Automotive

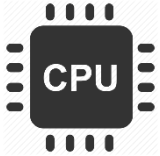


  - Data center

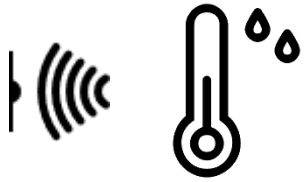
  - ISP



- MCU variants



- Sensor Hub

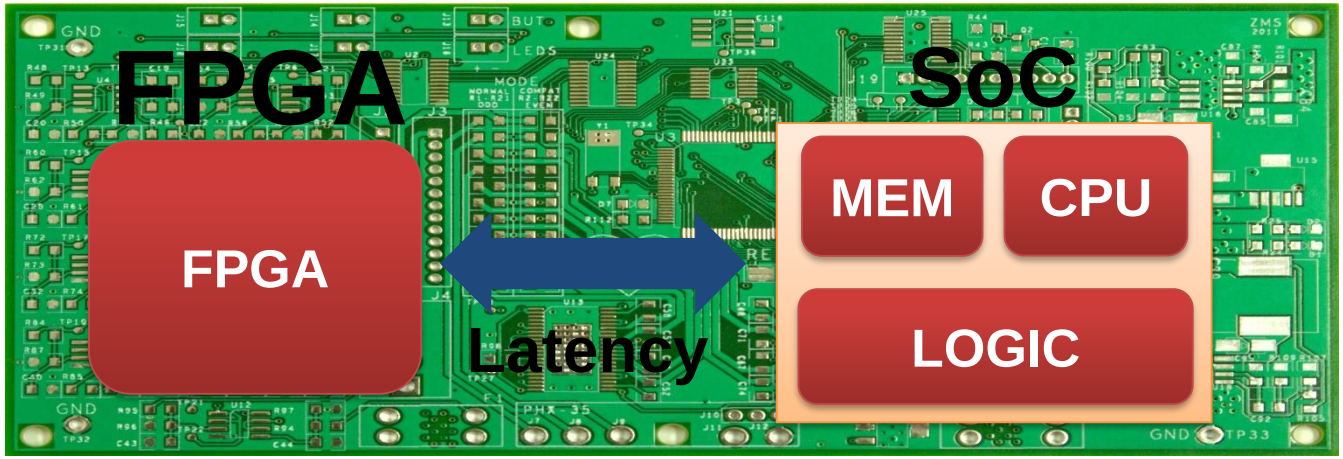


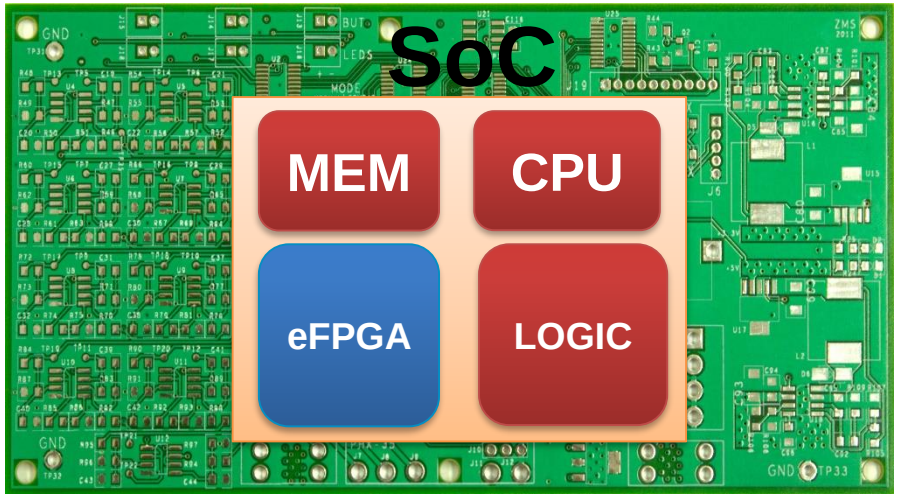
- Security / Cryptography

- Satellite payload

- Signal Processing

SOC + FPGA
vs
SOC with eFPGA



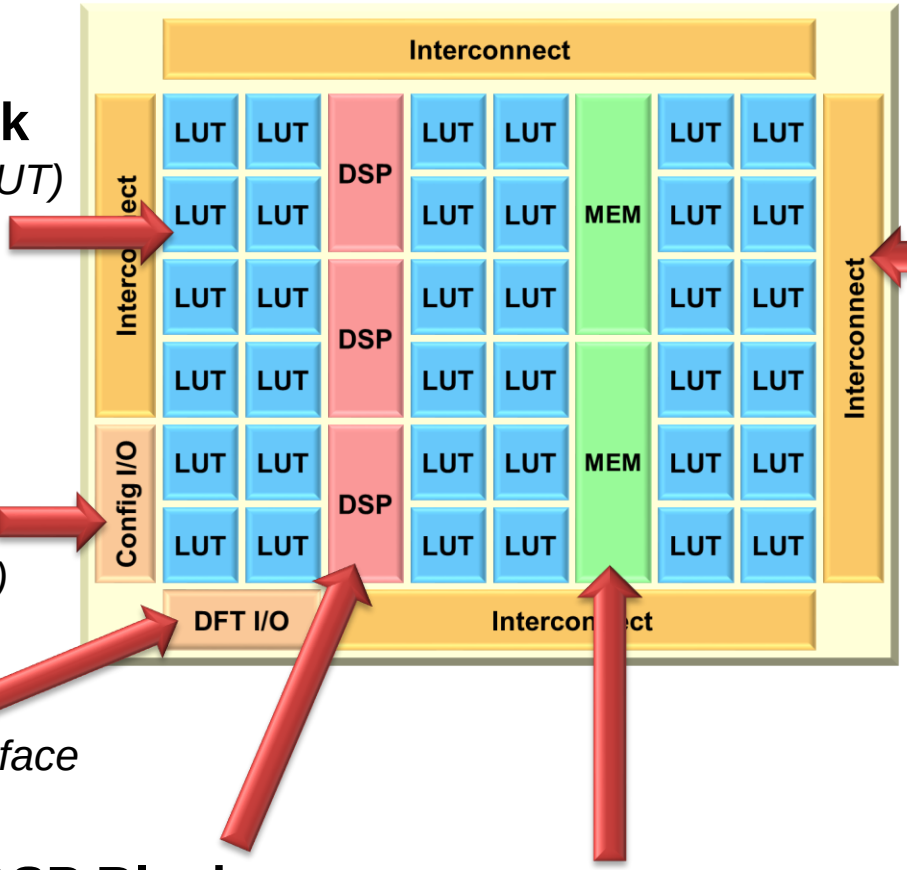


- Latency
- Power
- Cost

Menta 4th Generation eFPGA

embedded Logic Block

- *Menta Look Up Table (MLUT)*
- *Carry chain*
- *Patented technology*



IO pins

Define pins number

Configuration

- *Classical interface*
- *Optional soft IP (SPI/AHB)*

DFT

- *Standard scan chain interface*
- *Patented technology*

embedded DSP Block

- *MAC*
- *Complex DSP*
- *Customer/3rd Party DSP*

embedded Memory block

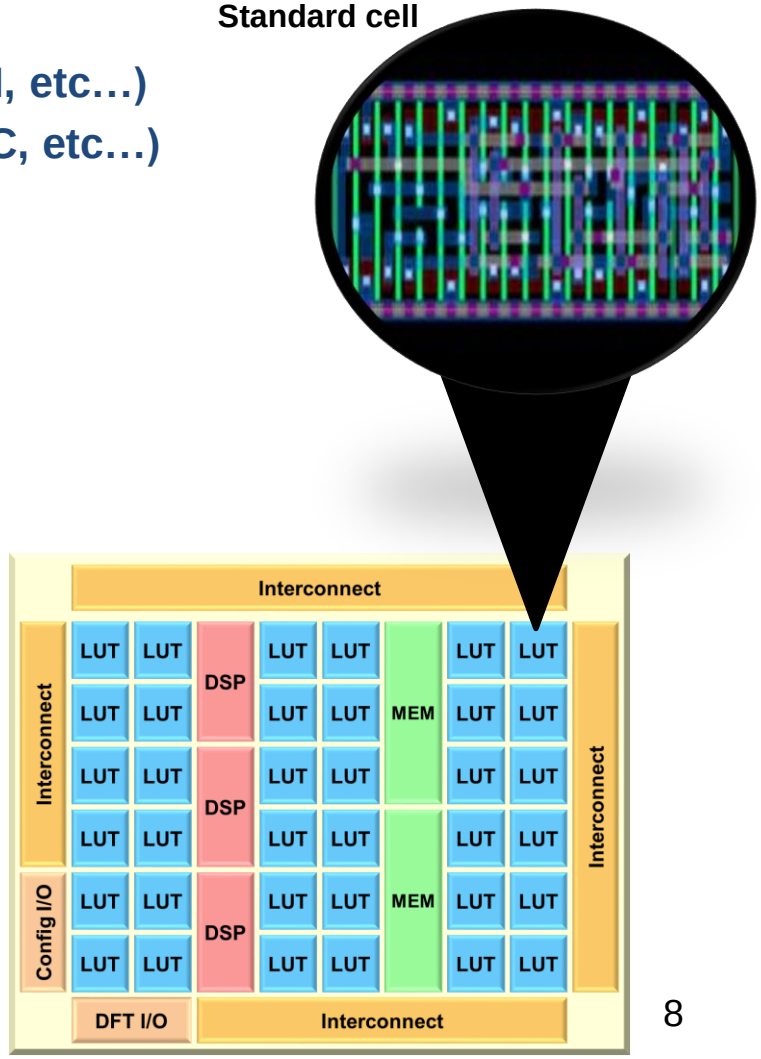
- *From Memory compiler (Foundry/Mem/Customer Provider)*
- *Type and size can be choosen*

100% Standard Cell Trusted eFPGA Hard-Macro

- **100% standard cell based**
  - From Std Cell provider library (Synopsys, ARM, etc…)
  - Or from Foundry library (TSMC, GF, SMIC, UMC, etc…)
  - Or from Customer library

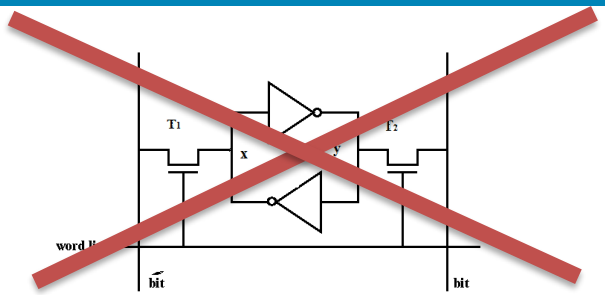
- **Standard EDA integration:**
  - No Blackbox
  - Full Gate Level netlist Simulation
  - STA + timings accuracy
  - Power accuracy
  - ATPG + vector files
  - Cadence/Synopsys/Mentor compatibility

Customer can verify every stage

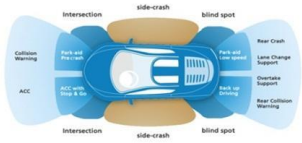


Trusted configuration
Not SRAM based

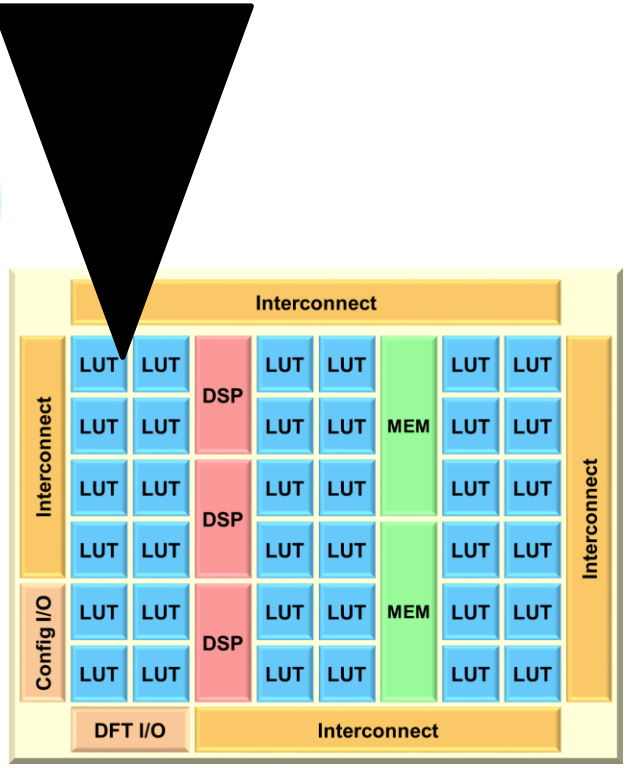
- **SRAM eFPGA # SRAM Compiler**



- **SRAM eFPGA**
  - **SRAM dedicated cell must be developed**
  - **DFT not standard => custom DFT**
  - **Characterization and testchip**



- **MENTA**
  - **Use Standard-Cell Register technology**
  - **Patented architecture**
  - **Standard DFT (managed by EDA tools): FC=99.9%**
  - **Very fast test time => low cost test**
  - **Standard verification**
  - **High Yield**
  - **Less prone to radiation errors (SEU)**
  - **Don't need characterization or testchip**



Trusted Standard Integration

eFPGA Hardware

eFPGA Hard Macro

GDS/NETLIST
STIL/SDF/LIB

SOC

SOC RTL

SOC design + verification

TAPEOUT

eFPGA software

RTL application

Origami Programmer

Bitstream

Bitstream

ASIC provider

Menta

flexible eFPGA

Up to 500k equivalent ASIC Gates

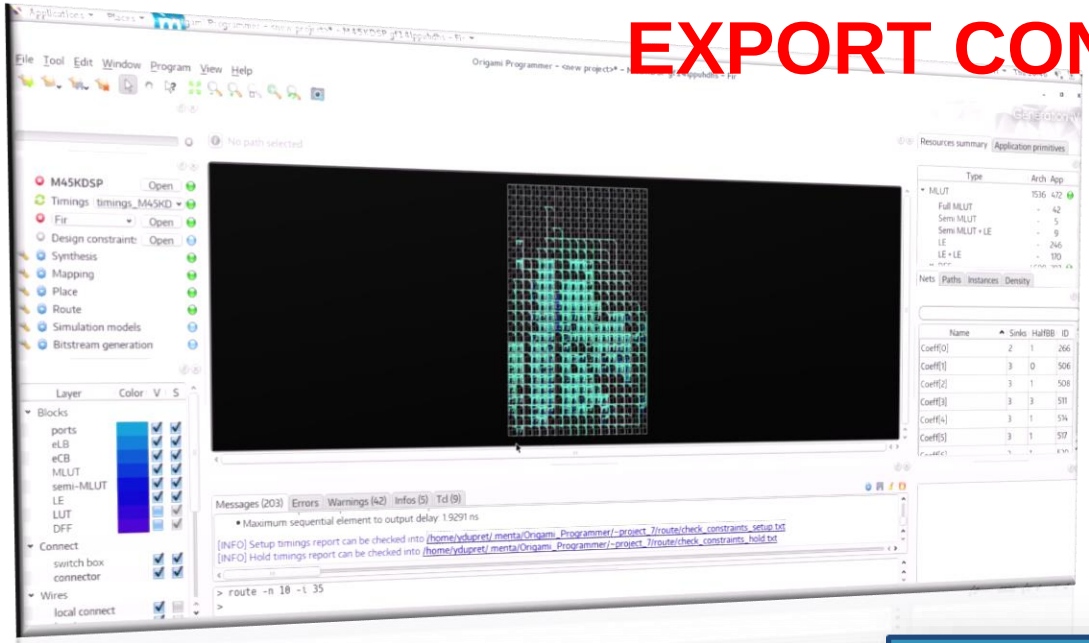
- **Foundry & node**
- **Standard cells provider**
- **Voltages**
- **VT flavors**
- **Metal stack**

Power and Speed Trade-off

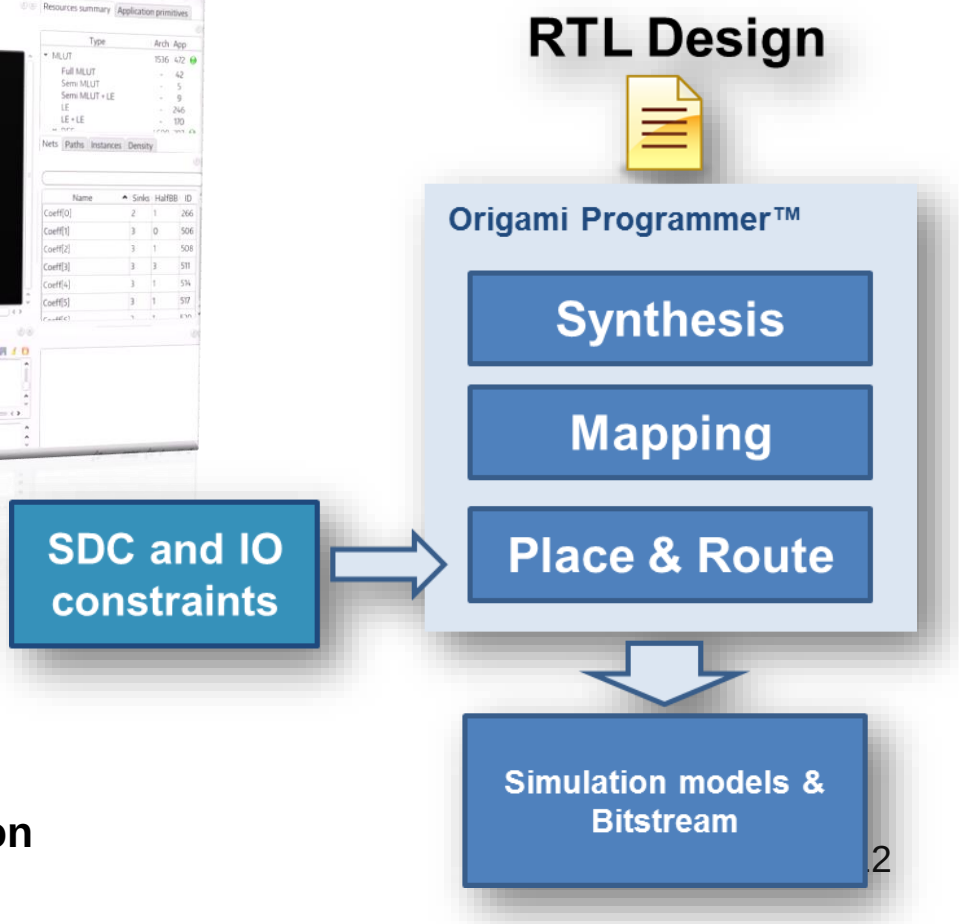
- **Form factor**
- **# IOs**
- **# LUTs**
- **DSP:**
  - **Menta 18bits MAC**
  - **Menta Complex DSP**
  - **Customer blocks**
- **Memory # & types**

Trusted Programming Software

EXPORT CONTROL ISSUES FREE



- IEEE VHDL/Verilog/SystemVerilog
- Routing congestion map
- LUT, FF, DSP resources
- Automatic DSP/MEM inferring
- Max Freq result
- STA
- Verilog model + SDF back-annotation
- Floorplanning



Menta offers

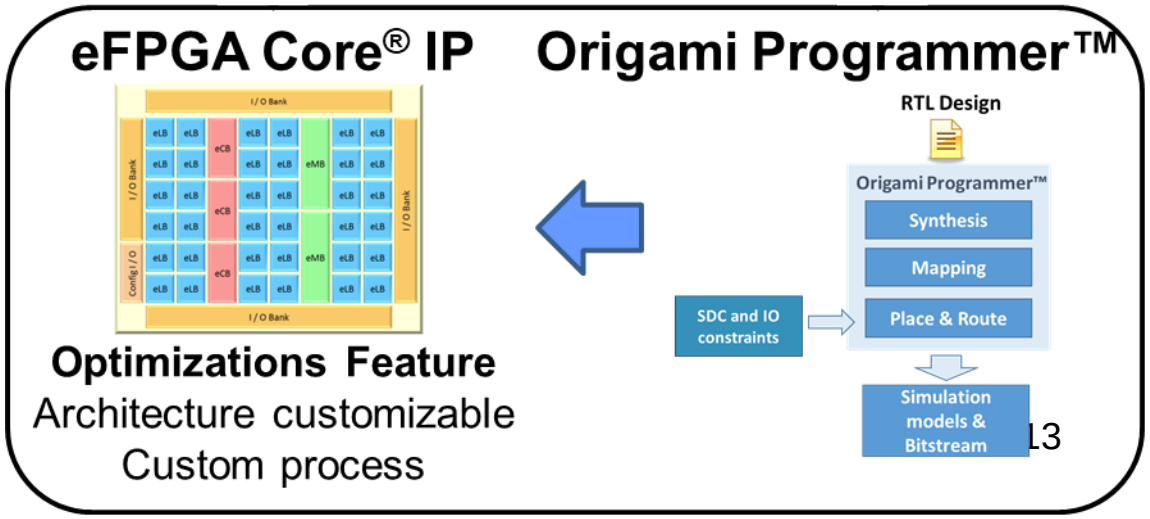
Pre-defined IP Menta (IPM)

Off-the-shelf eFPGA IP

Family of 5 optimized IPs

- From 7K to 60K equivalent ASIC gates
- Physical IP (GDSII)

Packaged with Origami Programmer



Menta offers

Dedicated eFPGA IP

eFPGA designed with Origami Designer and physically implemented by Menta

Menta deliverables:

- Up to 500K equivalent ASIC gates
- eFPGA dedicated array
- Physical Hard-Macro (GDSII)

Packaged with Origami Programmer

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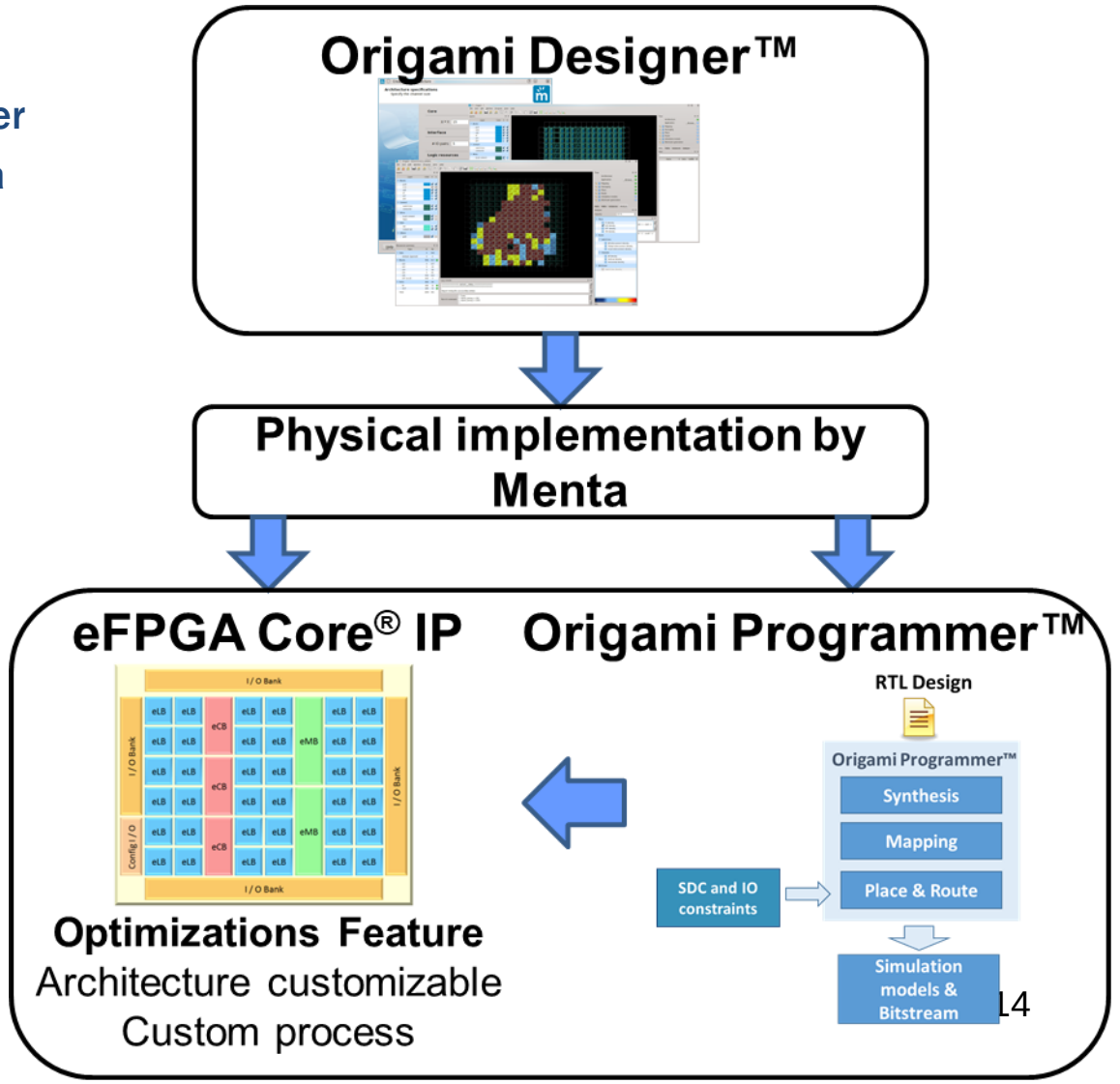

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Our partner in China

See us at our Booth

谢谢