D&R IP-SOC DAYS

Shanghai Event
September 14, 2017

Configuring DDR Interface IP to Enhance Speed and Minimize Design Footprint

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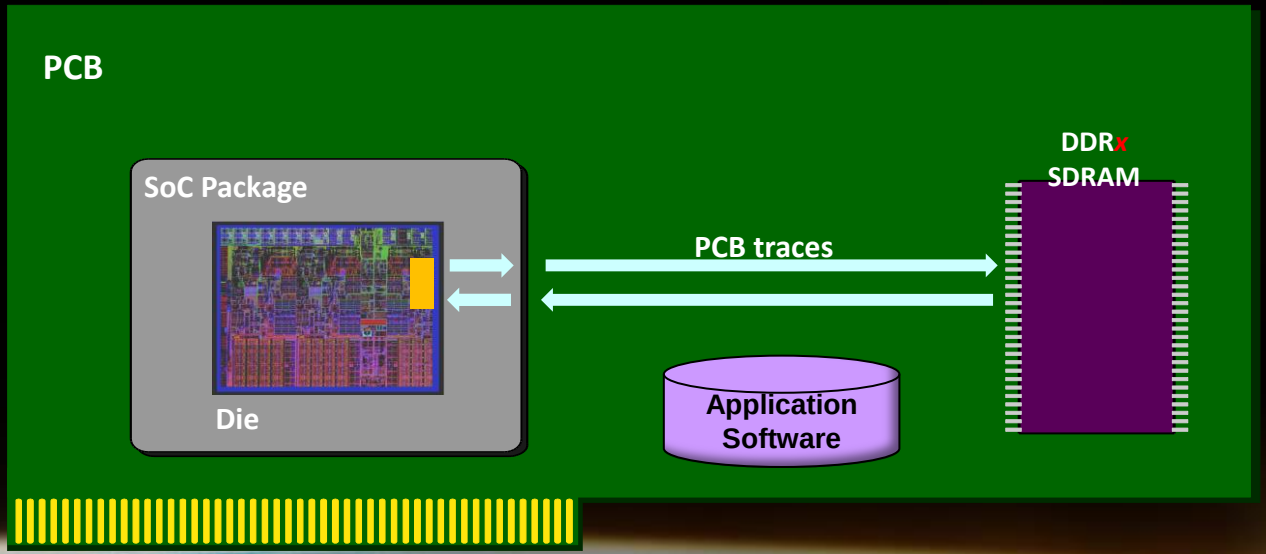
What Limits DDR Performance?



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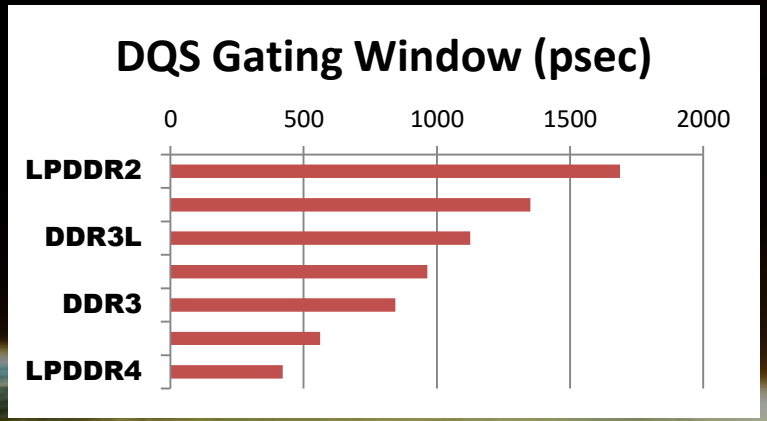
Timing Margins are Smaller

- LPDDR4 DQS gating window only 420 psec
- More sensitivity to Voltage and Temperature changes

DDR Type	Data Rate (Mbps)	Shortest Round Trip (ps)	Longest Round Trip (ps)	DQS Gating Window (ps)
LPDDR2	1066	2500	5500	1688
DDR3U	1333	255	400	1351
DDR3L	1600	225	400	1125
LPDDR3	1866	2500	5500	964
DDR3	2133	180	400	844
DDR4	3200	160	225	562
LPDDR4	4266	1500	3500	421



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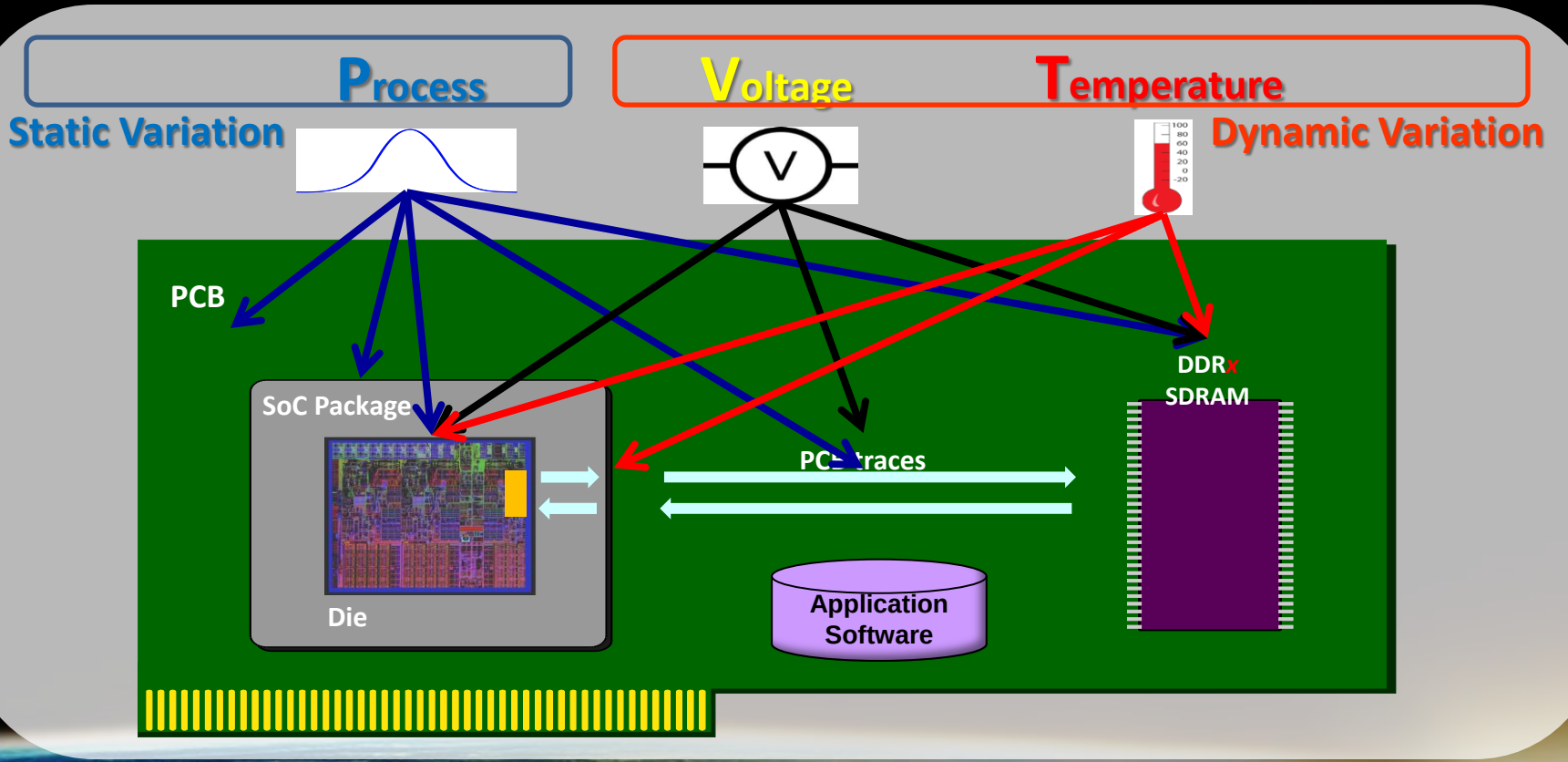
Static & Dynamic Variations

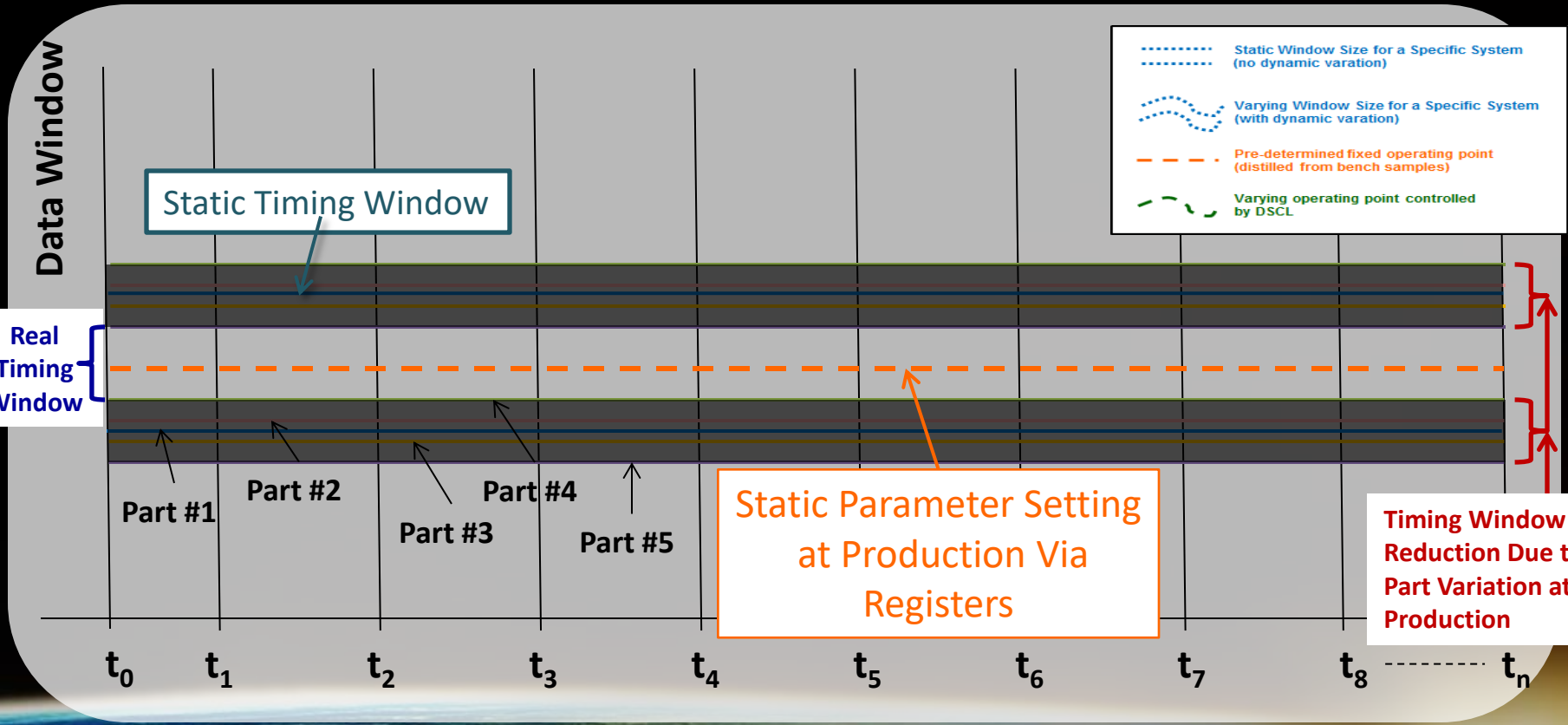


The Modeling Approach

Build the Best Model You Can

- With limited engineering samples, go through each chip and find the timing parameter that works
- Find the average of the timing window
- Set registers to accommodate most chips at production
- And WORRY!

Static vs. Dynamic Timing Window



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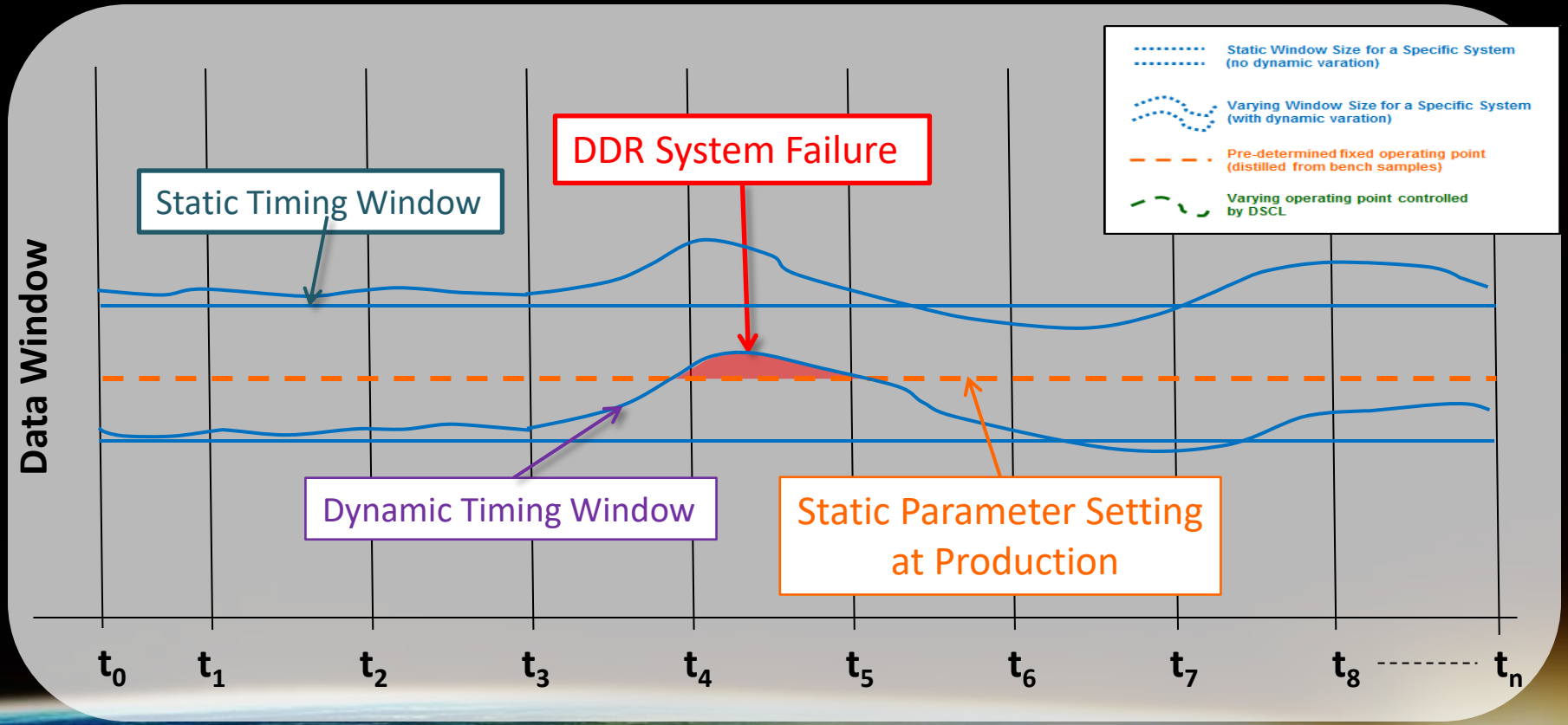
Static vs. Dynamic Timing Window



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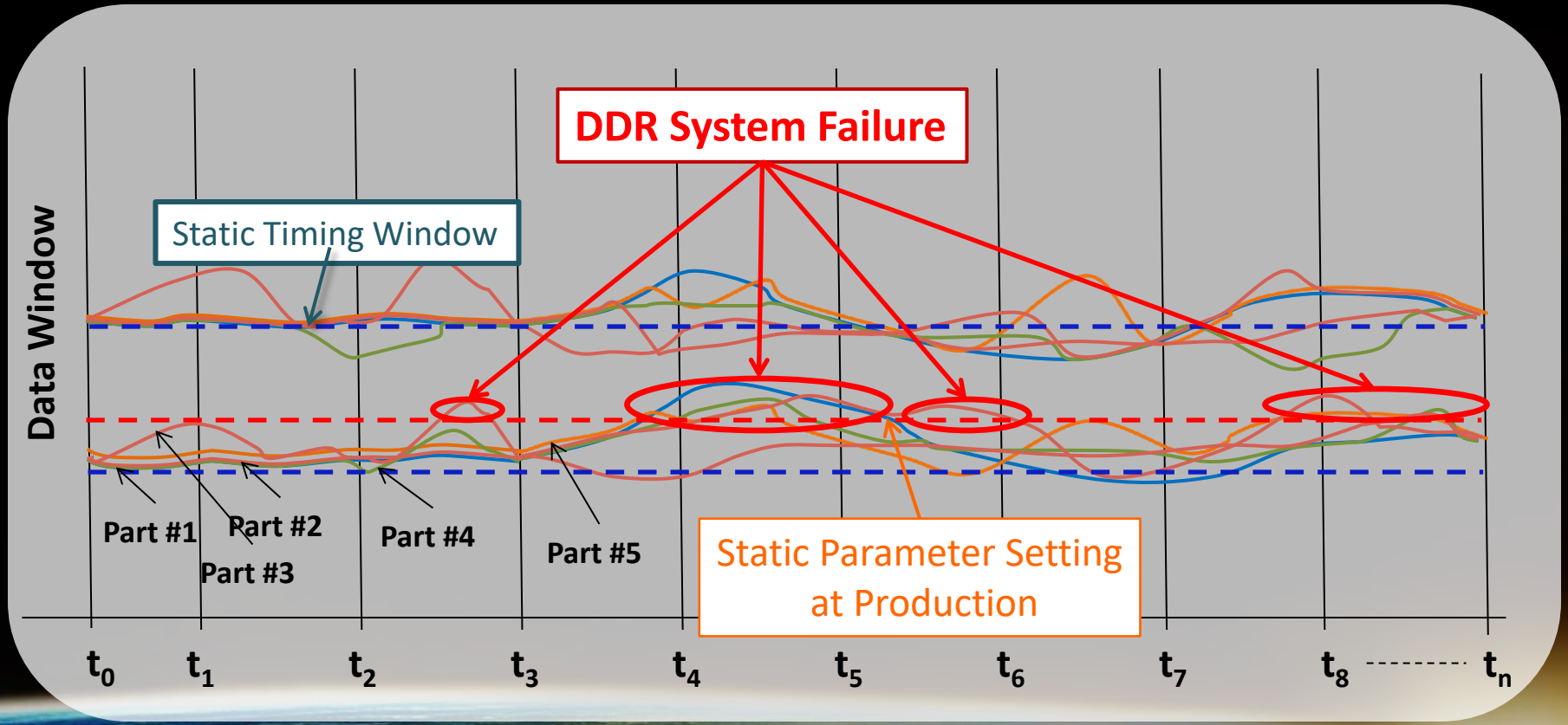
Dynamic Variation Between Production Parts



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The Solution:

Self-Calibrating Logic

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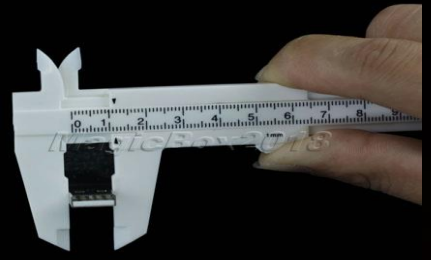
Precise Measurement

- No guessing with Self-Calibrating Logic (SCL)
- Accurately measure timing **in the system**
- Accommodates each unique system **at production**
- Relax! Your worry is over!



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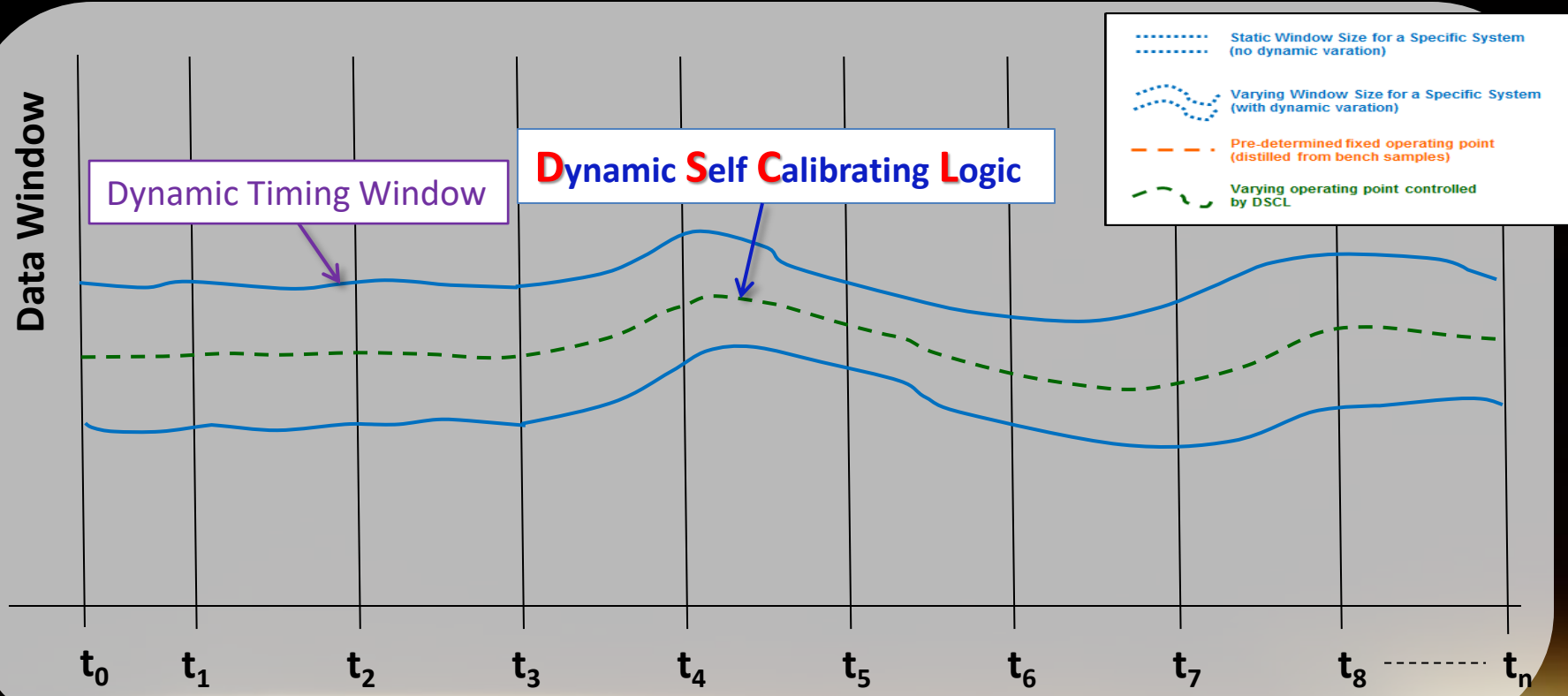
Dynamic SCL Ensures Maximum Data Rate



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The Fastest DDR SoC Interface IP

- Get the best performance for your system
- SCL measures **system timing** parameters: SoC + PKG + PCB
- Adjusts timing for **each system** at production
- Delivers fastest DDR data rate in all silicon nodes

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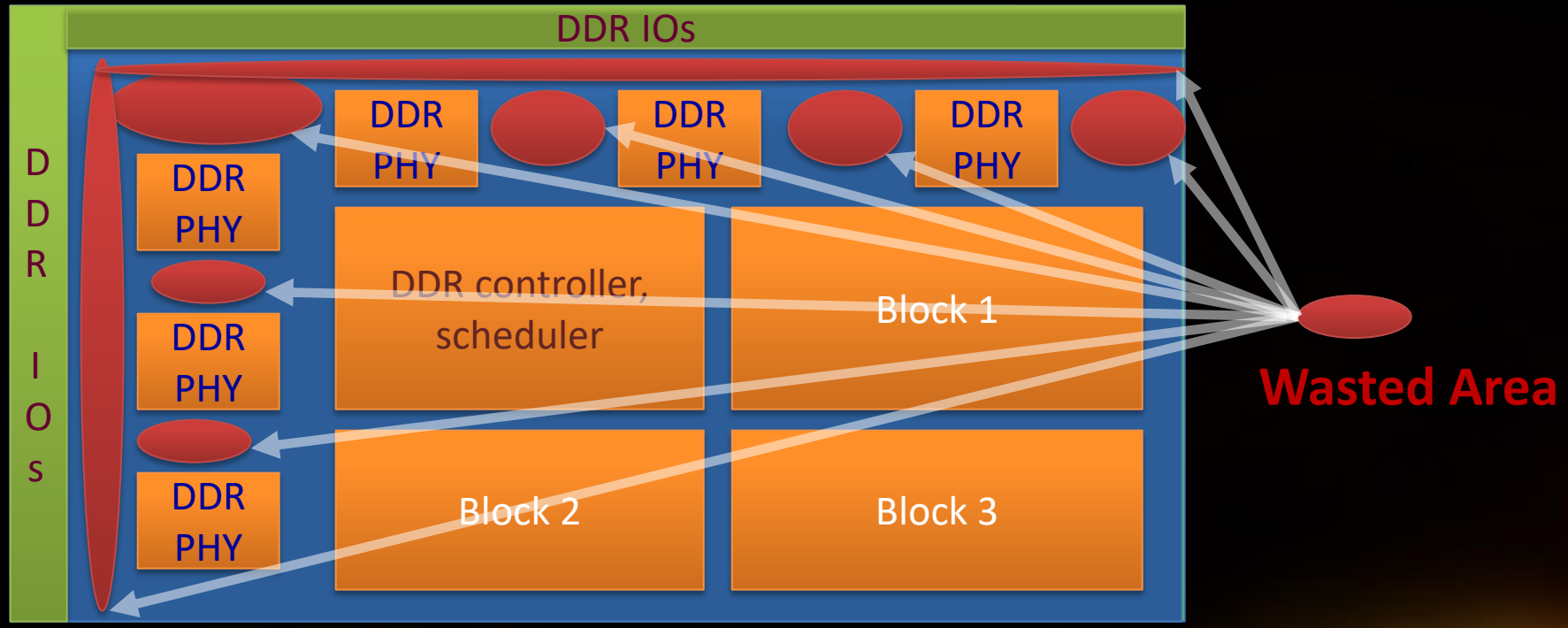
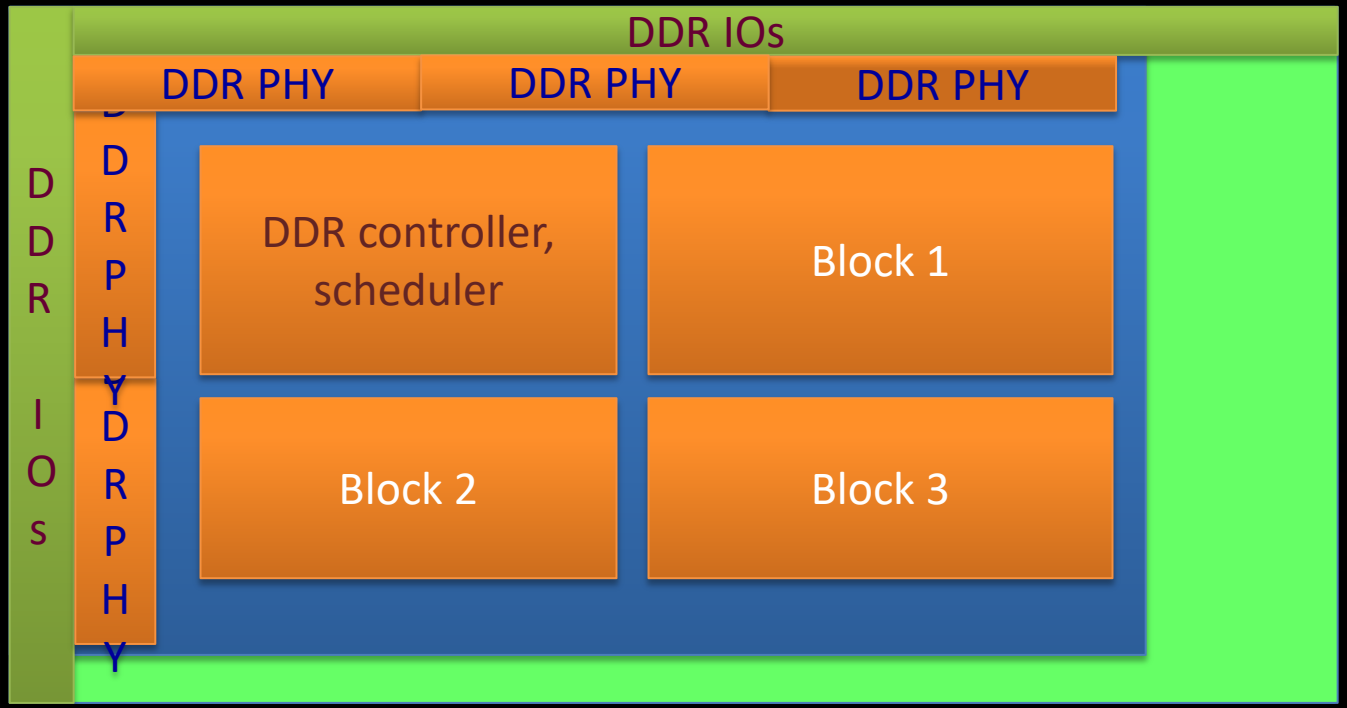
Improving Area and Reliability

Remove Wasted Area in Floorplan



Ultra-Low Area Footprint



- ✓ Customized PHY for any pad frame
- ✓ Only 2–3 weeks instead of months effort

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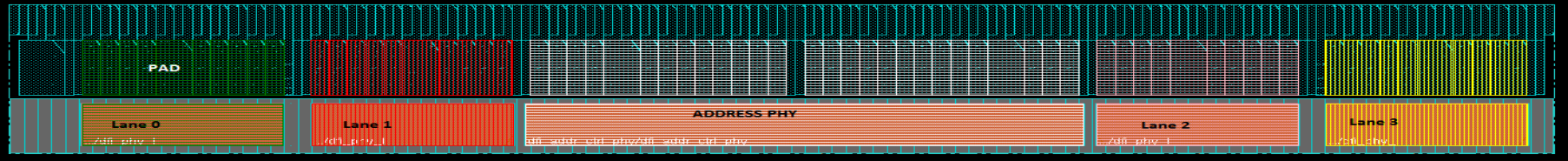
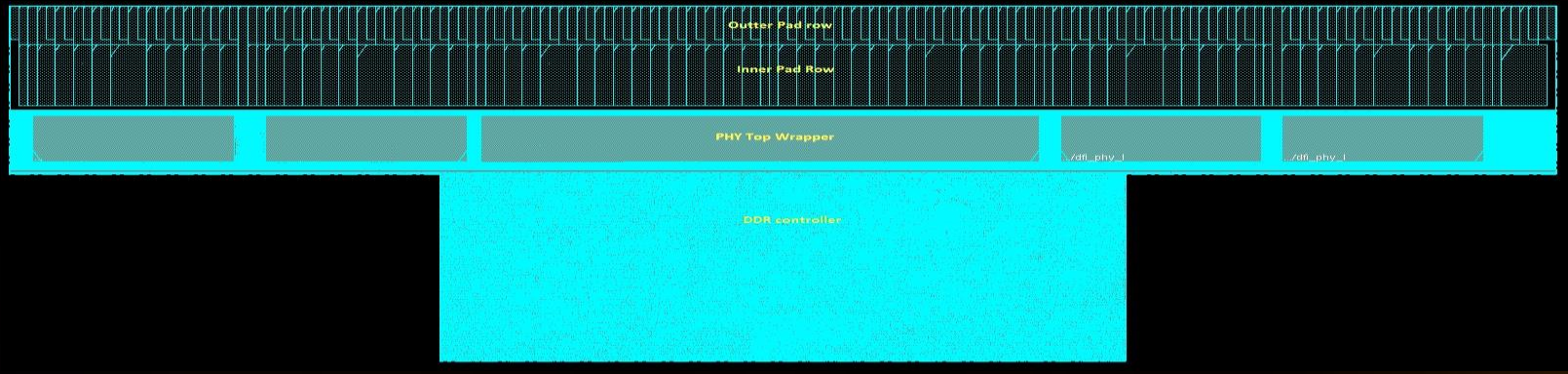
Optimal PHY & IO Integration

- PHY along side the IO pads
- Allows any pad ordering
- PHY height kept to a minimum

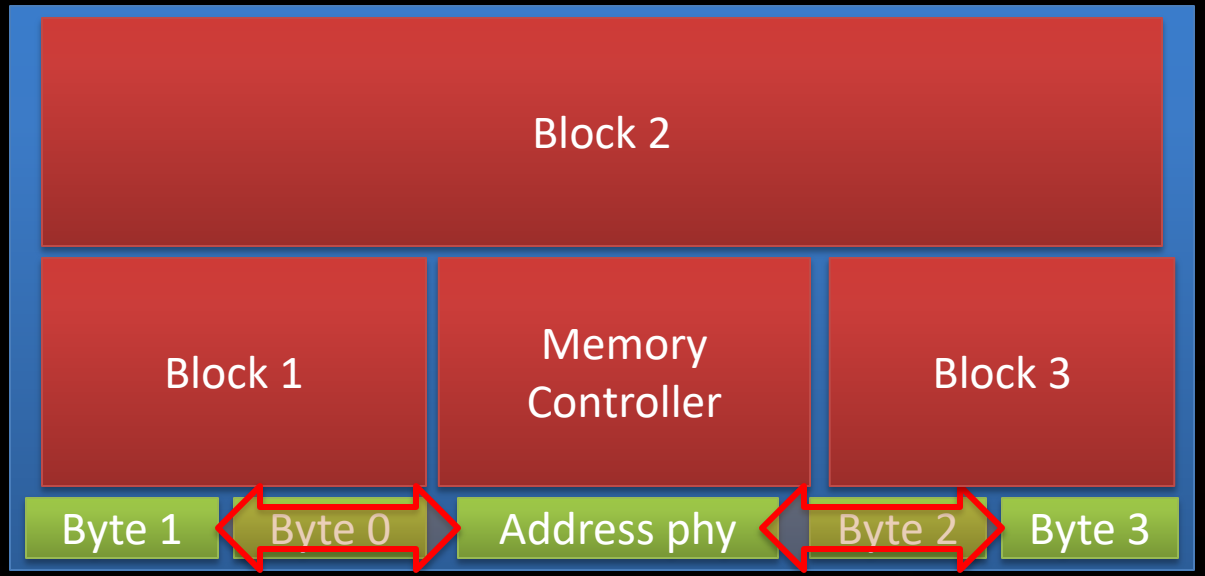


DDR Controller Integration Flexibility

- Integrate memory controller and close timing between controller and PHY



PHY Chaining Saves Top-level Routing



Allows extremely narrow channel next to PHYs in top level

- Training/config. signals routed between PHY edges
- Most top-level connections between memory controller and address PHY
- Tighter top level floorplan

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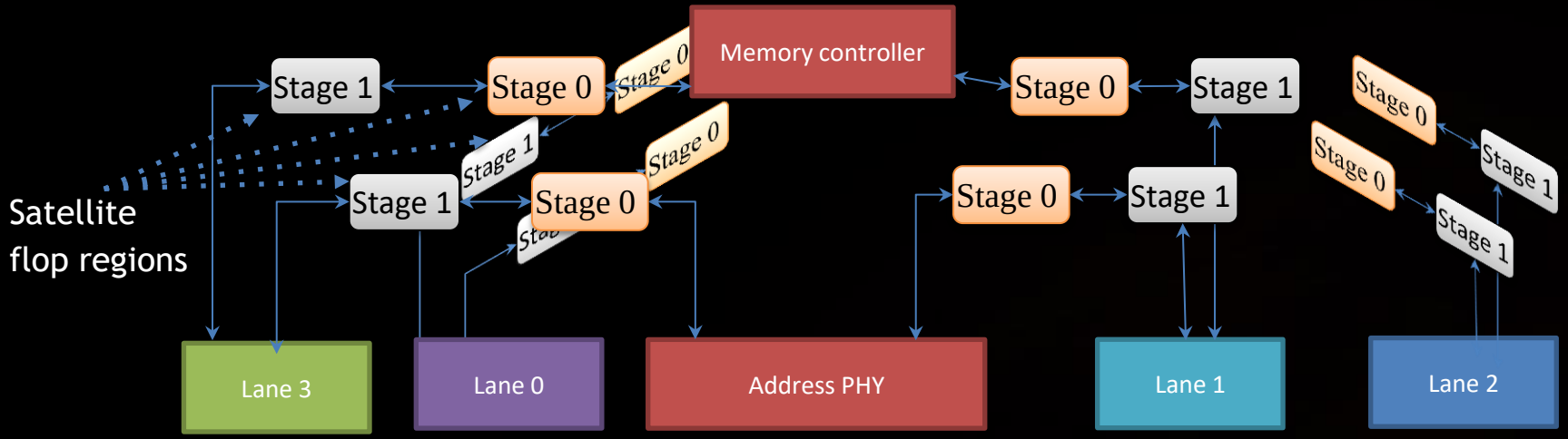
Satellite Flops Help Close Timing



- Helps meet timing on critical DFI paths from MC and address PHY to far flung data PHYs
- Ensures same clock cycle timing to all PHYs

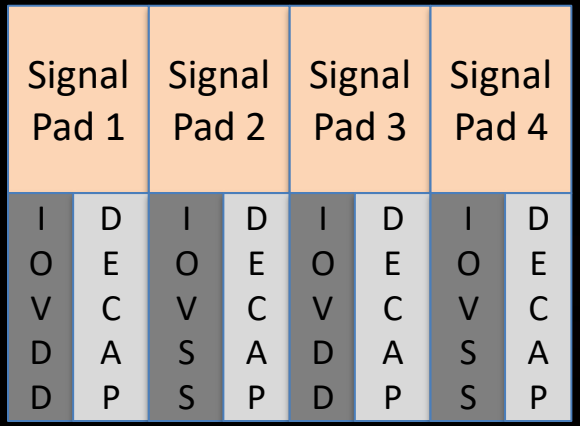
Satellite Flops Placed on the Top Level

- Area efficient
- Fewer signal routes, lower latency
- Convenient to close timing

DDR IOs Influence ASIC Floorplan

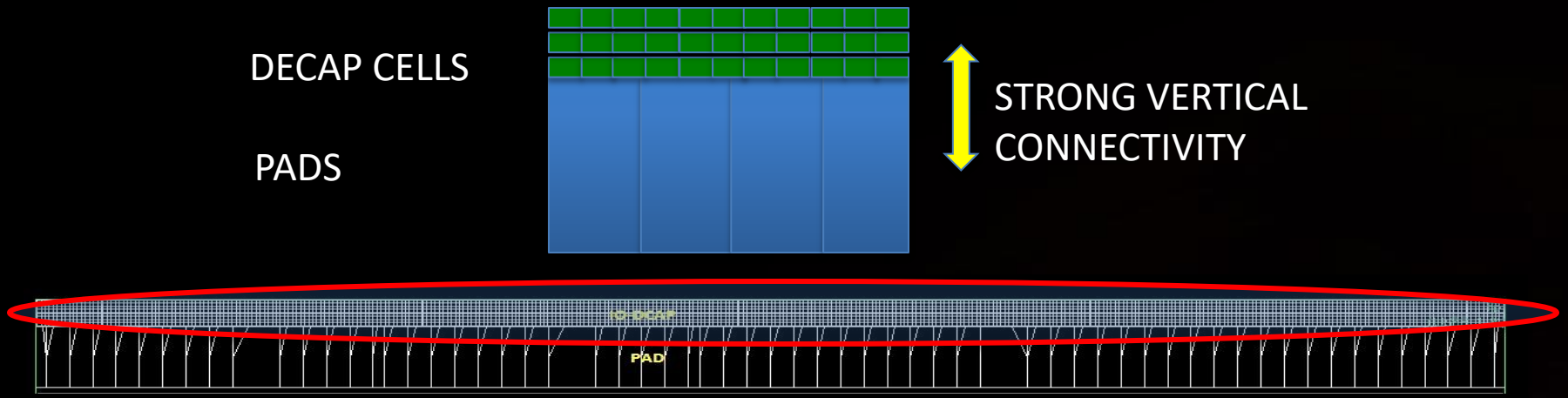
- Why is DDR IO span is so wide?
  - Need 1 VDDIO or VSSIO pad for every DDR signal IO (SSO ratio of 2:1) for high performance designs
  - Need decap for VDDIO/VSSIO power
- Shorter DDR IO pad frame saves area

Padframe Shortened by 50%



- Signal IOs on inner row
- Power/decap IOs on outer row
- Typical wirebond designs use 3 rows of bond pads

Flexible DECAP Scheme for Area



- Rows of decap cells are added incrementally beyond the outer IO row
- Right place, right amount!

Uniquify Combination DDR Interface IP

- Supports multiple different SoC applications
- LPDDR 4/3
- DDR 4/3
- DDR 4/3 + LPDDR 3
- DDR 4/3 + LPDDR 3/2

Foundry	Proven Silicon DDR Interface
GF	55LPe, 40LP, 28SLP/HPP, 22FDX
ICF	14FF
SMIC	55LL, 40LL, 28HK
Samsung	28LPP
TSMC	40G/LP, 29HPC/HPC+/HPM
UMC	28HLP

Thank You.

For more information, please contact

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