How to accelerate SoC Power Network Architecture Exploration

IP SoC Day – Grenoble – Martine FALHON – Product Marketing Manager

Not just a supplier of Technology, but provider of the Dolphin Integration know-how!
Since 1985

150 highly qualified design engineers for Mixed Signal development

> 200 Silicon IPs available across multiple nodes and foundries
  - Power Management
  - Standard Cell libraries
  - Memory Compilers
  - Audio CODECs/ADCs/DACs & Triggers
  - Oscillators

HQ in Grenoble, France
Subsidiaries in Canada & Israël

Renowned for
- Silicon IPs
- Design Methodology Software
- ASIC Design & Supply

> 500 customers worldwide
• Demanding markets (IoT, Autonomous vehicle, Mobile)
  ➔ Performance is not anymore the only constraint
  ➔ Power consumption has to be part of the equation
• New of smart and energy efficient SoC architectures based on stringent PPA
  ➔ meet end-users quest of compacity
  ➔ counterbalance manufacturing expenses
  ➔ maximized leadtime before battery recharge or replacement
• Manual processing is no more suitable
• SoC Architect, the BIG PICTURE owner

• Energy efficient SoC -> Focus on SoC Power Network
DEFINE your SoC architecture with PowerStudio™

BUILD a set of SoC architectures in PowerStudio

EXPLORE each candidate architecture with PowerArchitect

GENERATE formats of the winning architecture with PowerDesigner

SPEC from customer

EDA Solutions
• Core features
  ➤ To **BUILD** a set of candidate SoC power network architectures
  ➤ To **RUN** all required upcoming simulations

• Key features
  ➤ To **EXPLORE** architectures (PowerArchitect)
  ➤ To **GENERATE** optimized architecture related views (PowerDesigner)
BUILD a set of candidates of SoC power network architectures

- Project hierarchy
- Schematics based on a growing library of models
- Modes and transitions
- Build a set of similar synopses for further comparisons
• Early detect big inconsistencies in conception

• Control cross-block electrical specifications compatibility in each mode - input/output voltage, output current and impedance

• Check power supplies can provide the level of current expected by their respective associated loads
• Cost efficiency evaluation

• FOM configuration factors
  → Area (SoC components + Pads & Pins for bounding)
  → BOM (peripheral devices)
  → Power consumption (at component and mode levels)

• Sub score weighting / constraints

• Architectures ranking based on respective FOM score comparison

\[
\text{FOM score} = \text{Area} \times \% + \text{BOM} \times \% + \text{Power consumption} \times \%
\]

\(\text{Wa} + \text{Wb} + \text{Wp} = 100\%\)
Implementation quandary score (IQ)

- Risk evaluation of component implementation
- Early detection of power integrity issues
- IQ configuration factors
  - Potential noise level generated by aggressors (digital loads, regulators)
  - Noise tolerance level of potential victims (analog loads)
- Consolidated view of
  - Level of noise generated by power supply oscillations deterioring the SoC performance
  - Frequencies propagation path monitoring
  - Risk of side load aggression
- Architectures ranking based on respective IQ score comparison
• Compare both FOM and IQ score rankings
• Identify the best trade-off between cost-efficiency and risk of implementation
• From traditional SoC power network architectures to more innovative combinations
• From architecture to design stage
  ➔ Budget views
  ➔ Aligned UPF/RTL Top views
  ➔ Dolphin Power Management Unit (MAESTRO) configuration file

• Mirrors all the strategic data of your winning synoptic

• Forget tedious manual generation of views
**VALUE-ADDED FEATURES**

- Agile project management
- Ever-growing centralized library of IP models
- Wide scope of exploration criteria
- Noise propagation simulation
- Modes configuration interface
- User-friendly schematics
- Automatic views generation
- Results export

**BENEFITS FOR ARCHITECTS**

- Increasing range of PRNet architectures assessed
- Cost efficiency
- Risk limitation
- Faster PRNet architecture exploration
- Right-on-first pass PRNet architecture (no iteration loop)
- Smart bridge from Architecture to Design

**GLOBAL TTM REDUCTION**
• PowerStudio™ v1.0
  ➔ Includes PowerArchitect’s SoC power network architecture exploration key feature
  ➔ Available on January 7th, 2019

• Apply now to become a Beta Tester!
  ➔ Looking for Beta Testers to integrate the PowerStudio™ V1.0 Beta Test program
  ➔ Apply at contact@dolphin.fr
Thank You
Input

- **Key architecture components** and their distribution within Power Islands
- **Modes & Transitions**
- **Power, Area, BoM**-related specific information of each power islands
- **% of use of each mode**
- **Global weight** of Area, BoM & Power for candidate architectures’ FoM calculation

Output

- **Scoring/checks algorithms**
  - **IPCC**: Check of PRNet components compatibility (compatibility check)
  - **FoM**: Score consolidating weighted BoM, Area and Power consumption for a given architecture. The set of weights of a FoM reflects a specific use case constraints (cost efficiency optimization index)
  - **IQ**: Evaluates the noise resilience of a circuit in regards on the various levels of impact that frequency variations propagated through the candidate architecture may have on sensitive loads (power integrity index)

- **Results**
  - Comparison of the analysis results of a given set of architectures

- **Export**
  - to MS Excel
  - New export formats to come (PowerDesigner™): RTL top, UPF top, budgets, and other useful files related to the winning architecture